# **CW9253-125** Data sheet

## Four-channel14 Bit125MSPS ADC

## **1.0** overview

The CW9253-125 is a 4-channel, 14-bit, 125MSPS analog-to-digital converter (ADC) with built-in sample and hold circuitry, specifically designed for low cost, low power consumption, small size and ease of use. The product has a conversion rate of up to 125MSPS, excellent dynamic performance and low power consumption, and is suitable for small package applications.

The CW9253-125 is powered by a 1.8 V single power supply and an LVPECL/CMOS/LVDS compatible sample rate clock signal to maximize its performance. For most applications, no external reference power supply or driver device is required.

To obtain the appropriate LVDS serial data rate, the CW9253-125 automatically multiplies the sample rate clock. It provides a data clock output (DCO) for capturing data at the output, and a frame clock output (FCO) for sending a new output byte signal. It also supports each channel to enter the power-saving state independently; Typical power consumption less than 2.2 mW when all channels are closed

## **2.0** Applications

- Medical imaging and non-invasive ultrasound testing
- High-speed imaging
- Radio receiver
- Test equipment

## **3.0** peculiarity

- 1.8 V Power Supply
- Low power consumption: per channel170mW @ 125MSPS
- Signal-to-noise ratio(SNR)：76.5 dBFS @ 70MHz
- Differential nonlinearity(DNL)：± 0.7 LSB (Typical value)
- Integral nonlinearity(INL)：± 3.5 LSB (Typical value)
- Low power serialLVDS
- $2V_{P-P}$ Input voltage range
- QFN-48 Encapsulation7 mm × 7 mm

## **4.0** Performance indicators

- Full power bandwidth:650 MHz
- Static performance:DNL-1.0/+1.0 LSB，INL-5.0/+5.0 LSB
- Dynamic performance（$f_s$ =125MSps, input signal power-1 dBFS）

— $f_{in}$ = 9.7 MHz
ENOB = 11.7 Bit，SNDR = 72 dBFS，SNR = 72.5 dBFS

— $f_{in}$ = 70 MHz
ENOB = 11.2 Bit，SNDR = 69 dBFS，SNR = 69.5 dBFS

— $f_{in}$ = 128 MHz
ENOB = 10.5 Bit，SNDR = 64.7 dBFS，SNR =65.3 dBFS

— $f_{in}$ = 200 MHz
ENOB = 10 Bit，SNDR = 61.9 dBFS，SNR = 62.5 dBFS

## **5.0** Simplified block diagram

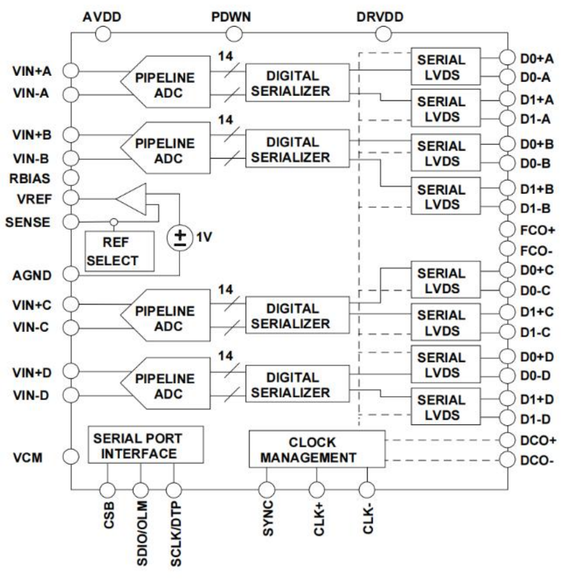


Figure5.1 CW9253-125 System block diagram

# **6.0** Typical performance

TABLE6-1 Conditions of use of chips

| parameter | Symbols | annotation | Numerical value | Units |
|---|---|---|---|---|
| Power supply voltage | $V_A$ | Analog circuit power supply | 1.8 | V |
| | $V_{DR}$ | Output drive circuit power supply | 1.8 | V |
| Power-on sequence | | No power-on sequence requirement | | |
| Ground | $GND_A$ | Analog circuit ground | 0 | V |
| | $GND_{DR}$ | Output drive circuit ground | 0 | V |
| Differential input analog signal amplitude(1) | $V_{INIP} - V_{ININ}$<br>$V_{INQP} - V_{INQN}$ | Differential amplitude of input signal | 2000 | mVpp |
| Logic input high | $V_{IH}$ | | $V_A$ | V |
| Logic input low | $V_{IL}$ | | GND | |
| Clock differential input signal swing | $V_{CLKP} - V_{CLKN}$ | | $200 \le V_{CLKP} - V_{CLKN} \le 3600$ | mVpp |
| Clock frequency | $f_{CLK}$ | | $f_{CLK} \le 1000$ | MHz |
| Conversion rate | $f_s$ | | 20-125 | MSPS |
| Operating temperature range | $T_A$ | | $-55 \le T_A \le 125$ | ℃ |

**NOTE:**
(1) Measurement conditions are input frequency, full-scale sine wave, load per output bit of approx5pF。

TABLE6-2 Electrical characteristics of power supply, inputs and outputs

Unless otherwise indicated,AVDD=1.8 V，DRVDD=1.8 V，−1.0 dBFS The full-scale differential input is2.0 V p-p；VREF=1.0V，DCS OFF.

| parameter | Symbols | Minimum | Typical value | Maximum | Units |
|---|---|---|---|---|---|
| Resolution | | | 14 | | Bit |
| Supply voltage: | | | | | |
| Analog circuit power supply | VA | 1.7 | 1.8 | 1.9 | V |
| Output drive circuit power supply | VDR | 1.7 | 1.8 | 1.9 | V |
| Supply Current: | | | | | |
| Analog circuit power supply | IA | | 310 | | mA |
| Output drive circuit power supply | IDR | | 70 | | mA |
| Analog input: | | | | | |
| Input differential analog signal amplitude | VINIP – VININ | 0.3 | 2 | VA | Vpp |
| Common mode voltage | VCM | | 0.9 | | V |
| Differential input resistance | RIN | | 2.6 | | kΩ |
| Clock input: | Differential sine wave | | | | |
| Logic compatibility | CMOS/LVDS/LVPECL | | | | |
| Input clock rate | *fMCLK* | 20 | | 1000 | MHz |
| Input differential swing | VCLKP –VCLKN | 200 | 900 | 3600 | mVpp |
| Input common mode voltage | VCM _ CLK | | 0.9 | | V |
| Clock differential input resistance | RCLK | | 15 | | kΩ |
| Internal reference voltage: | | | | | |
| Output voltage（1.0 V mode） | VREF | | 1 | | V |
| Input resistance | | | 7.5 | | kΩ |
| Power consumption: | | | | | |
| DC input power consumption | | | 620 | | mW |
| Sine wave input power consumption | | | 660 | | mW |
| Shutdown power consumption | PD | | 2.2 | | mW |

TABLE6-3 Static characteristics

| parameter | Symbols | Minimum | Typical value | Maximum | Units |
|---|---|---|---|---|---|
| Differential nonlinearity | DNL | -1.0 | 0.75 | 1.0 | LSB |
| Integral nonlinearity | INL | -5.0 | 3 | 5.0 | LSB |



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TABLE6-4 Dynamic characteristic(Reference）

Unless otherwise indicated,AVDD=1.8 V，DRVDD=1.8 V，−1.0 dBFS The full-scale differential input is2.0 V p-p；VREF=1.0 V，DCS OFF.

| parameter | Symbols | Minimum | Typical value | Maximum | Units |
|---|---|---|---|---|---|
| **$f_s$ = 125MSPS，$V_{in}$ = -1 dBFS** | | | | | |
| Significant digits | ENOB | 10.8 | | | |
| $f_{in}$ = 9.7 MHz（25°C） | | | 11.7 | | bit |
| $f_{in}$ = 15 MHz（25°C） | | | 11.65 | | bit |
| $f_{in}$ = 70 MHz（Full temperature | | | | | bit |
| $f_{in}$ = 128 MHz（25°C） | | | 10.51 | | bit |
| $f_{in}$ = 200 MHz（25°C） | | | 10.0 | | bit |
| Signal-to-noise ratio | SNR | 67.8 | | | |
| $f_{in}$ = 9.7 MHz（25°C） | | | 72.5 | | dBFS |
| $f_{in}$ = 15MHz（25°C） | | | 72.3 | | dBFS |
| $f_{in}$ = 70 MHz（Full temperature | | | | | dBFS |
| $f_{in}$ = 128 MHz（25°C） | | | 65.8 | | dBFS |
| $f_{in}$ = 200 MHz（25°C） | | | 62.5 | | dBFS |
| Signal ratio | SINAD | 67.2 | | | |
| $f_{in}$ = 9.7 MHz（25°C） | | | 72.1 | | dBFS |
| $f_{in}$ = 15MHz（25°C） | | | 71.9 | | dBFS |
| $f_{in}$ = 70 MHz（Full temperature | | | | | dBFS |
| $f_{in}$ = 128 MHz（25°C） | | | 65 | | dBFS |
| $f_{in}$ = 200 MHz（25°C） | | | 62.1 | | dBFS |
| Spur-free dynamic range | SFDR | 79.3 | | | |
| $f_{in}$ = 9.7 MHz（25°C） | | | 88.5 | | dBc |
| $f_{in}$ = 15MHz（25°C） | | | 85.3 | | dBc |
| $f_{in}$ = 70 MHz（Full temperature | | | | | dBc |
| $f_{in}$ = 128 MHz（25°C） | | | 77.5 | | dBc |
| $f_{in}$ = 200 MHz（25°C） | | | 71.4 | | dBc |
| Second harmonic | 2nd Harm | 80 | | | |
| $f_{in}$ = 9.7 MHz（25°C） | | | 97 | | dBc |
| $f_{in}$ = 15MHz（25°C） | | | 93 | | dBc |
| $f_{in}$ = 70 MHz（Full temperature | | | | | dBc |
| $f_{in}$ = 128 MHz（25°C） | | | 86 | | dBc |
| $f_{in}$ = 200 MHz（25°C） | | | 80 | | dBc |
| Crosstalk (Full temperature） | | | 90 | | dB |
| Analog input bandwidth （25°C） | | | 650 | | MHz |

Note: Measurement conditions of crosstalk: one channel input parameter is-1dBFS、70MHz Signal and no input signal on adjacent channels.



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# 7.0 Pin configuration and function description

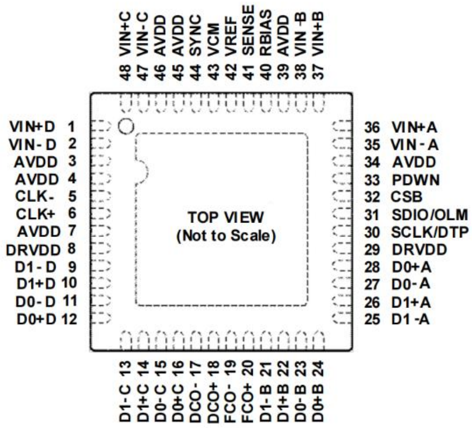


Figure7.1 CW9253-125 Pin arrangement（Top View）

TABLE7-1 Pin Function Description

| Balloon serial number | Symbols | functionality |
|---|---|---|
| 0 | AGND,<br>Exposed Pad | Analog ground with exposed pads. The bottom pad of the package provides analog ground for the chip. This exposed pad must be grounded for proper operation. |
| 1 | VIN + D | ChannelDAnalog input+ |
| 2 | VIN − D | ChannelDAnalog input- |
| 3, 4, 7, 34,39, 45, 46 | AVDD | Analog power supply,1.8 V |
| 5, 6 | CLK −, CLK + | Differential clock input |
| 8, 29 | DRVDD | A digital output drive voltage source,1.8 V |
| 9, 10 | D 1 − D, D1 + D | ChannelDDigital Output |
| 11, 12 | D0 − D, D0 + D | ChannelDDigital Output |
| 13, 14 | D 1 − C, D1 + C | ChannelCDigital Output |
| 15, 16 | D 0 − C, D0 + C | ChannelCDigital Output |
| 17, 18 | DCO −, DCO + | Data clock output |
| 19, 20 | FCO −, FCO + | Frame clock output |
| 21, 22 | D 1 − B, D1 + B | ChannelBDigital Output |
| 23, 24 | D0 − B, D0 + B | ChannelBDigital Output |
| 25, 26 | D 1 − A, D1 + A | ChannelADigital Output |
| 27, 28 | D 0 − A, D0 + A | ChannelADigital Output |
| 30 | SCLK/DTP | SPI Clock input/Digital test code |
| 31 | SDIO/OLM | SPI Data input and output/Output channel mode |
| 32 | CSB | SPI Chip selection signal, low enable operation,30 kΩ Internal pull-up |
| 33 | PDWN | Digital input,30kΩ Internal Drop Down<br>PDWN high=Switch-off device<br>PDWN low=Equipment operation, normal operation |
| 35 | VIN − A | ChannelAAnalog input- |
| 36 | VIN + A | ChannelAAnalog input+ |
| 37 | VIN + B | ChannelBAnalog input+ |
| 38 | VIN − B | ChannelBAnalog input- |
| 40 | RBIAS | Analog current bias, with10 kΩ (1%)Resistance grounding |
| 41 | SENSE | Reference voltage mode selection |
| 42 | VREF | Reference voltage input/Output |
| 43 | VCM | Analog input common mode voltage |
| 44 | SYNC | Digital input, frequency divider synchronous input |
| 47 | VIN − C | ChannelCAnalog input- |
| 48 | VIN + C | ChannelCAnalog input+ |



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# 8.0 Typical performance test curves (refer to）

Unless otherwise indicated,AVDD = 1.8 V、DRVDD = 1.8 V、VIN = − 1.0 dBFS Differential input,$f_S$ =125MSPS，$T_A$= 25 º C 1.0 V Internal reference voltage.

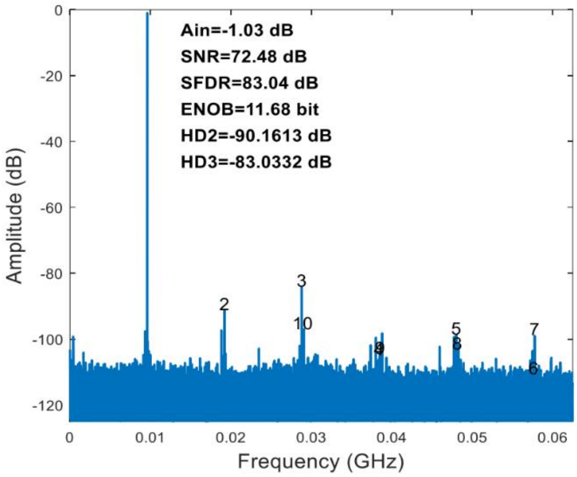


Figure 8.1 Single tone FFT (fin = 9.7 mhz @ 125MSPS)

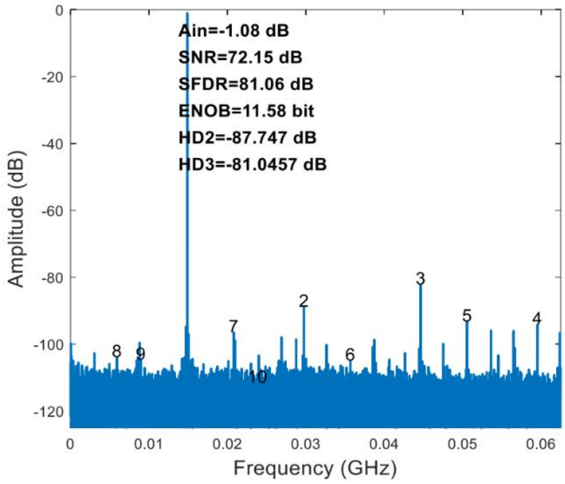


Figure 8.2 Single tone FFT (fin = 15MHz @ 125MSPS)

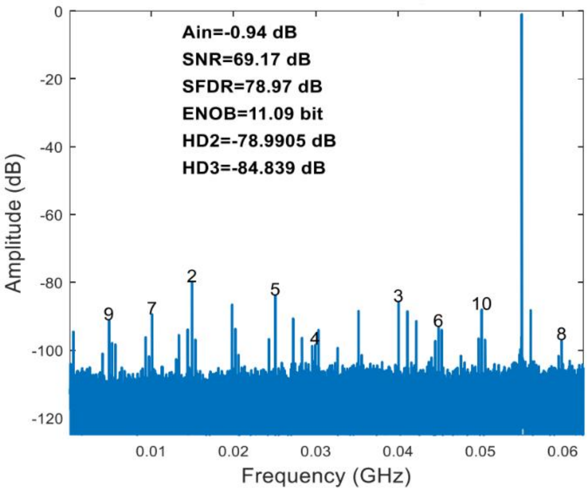


Figure 8.3 Single tone FFT (fin = 70MHz @ 125MSPS)

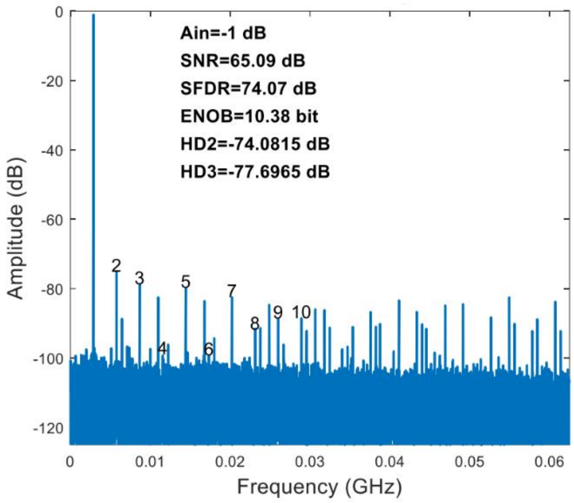


Figure 8.4 Single tone FFT (fin = 128MHz @ 125MSPS)

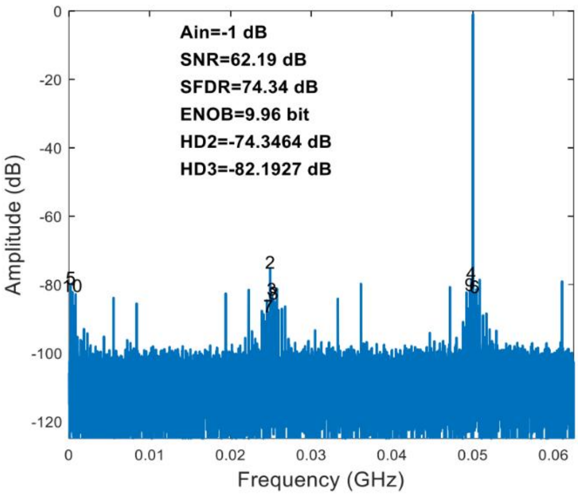


Figure 8.5 Single tone FFT (fin = 200MHz @ 125MSPS)

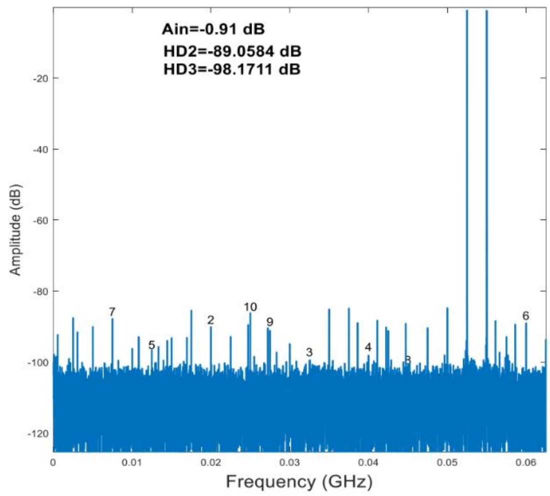


Figure 8.6 Double tone FFT (fin1 = 70.5 MHz and fin2 = 72.5 MHz @ 125MSPS)



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# 9.0 Timing diagram

## 9.1 Data timing

Unless otherwise indicated,AVDD = 1.8 V、DRVDD = 1.8 V、fs = 125MSPS、VIN = − 1.0 dBFS Differential input,1.0 V Internal reference voltage.

| parameter | Temperature | Minimum | Typical value | Maximum | Units |
|---|---|---|---|---|---|
| Clock input parameters | | | | | |
| Input clock rate | Full | 20 | | 1000 | MHz |
| Conversion rate | Full | 20 | | 125 | MHz |
| aperture | | | | | |
| Aperture delay（tA） | 25℃ | | 1 | | ns |
| shake | 25℃ | | 135 | | fs rms |
| Out-of-range recovery time | 25℃ | | 1 | | tcycle |
| Data output parameters | | | | | |
| Transmission delaytPD | | | 3 | | ns |
| FCO Propagation delaytFCO | Full | 1.5 | 2.3 | 3.1 | ns |
| DCO Propagation delaytCPD | Full | | tFCO+( tSAMPLE/16) | | ns |
| DCO To data delaytDATA | Full | ( tSAMPLE/16)-300 | (tSAMPLE/16) | ( tSAMPLE /16)+300 | ps |
| DCOToFCO DelaytRAME | Full | ( tSAMPLE/16)-300 | (tSAMPLE/16) | ( tSAMPLE /16)+300 | ps |
| Channel delaytLD | | | 90 | | ps |
| Wakeup time（await the opportune moment） | 25℃ | | 250 | | ns |
| Wakeup time（Power saving mode） | 25℃ | | 375 | | us |
| Pipeline delay | Full | | 16 | | tcycle |

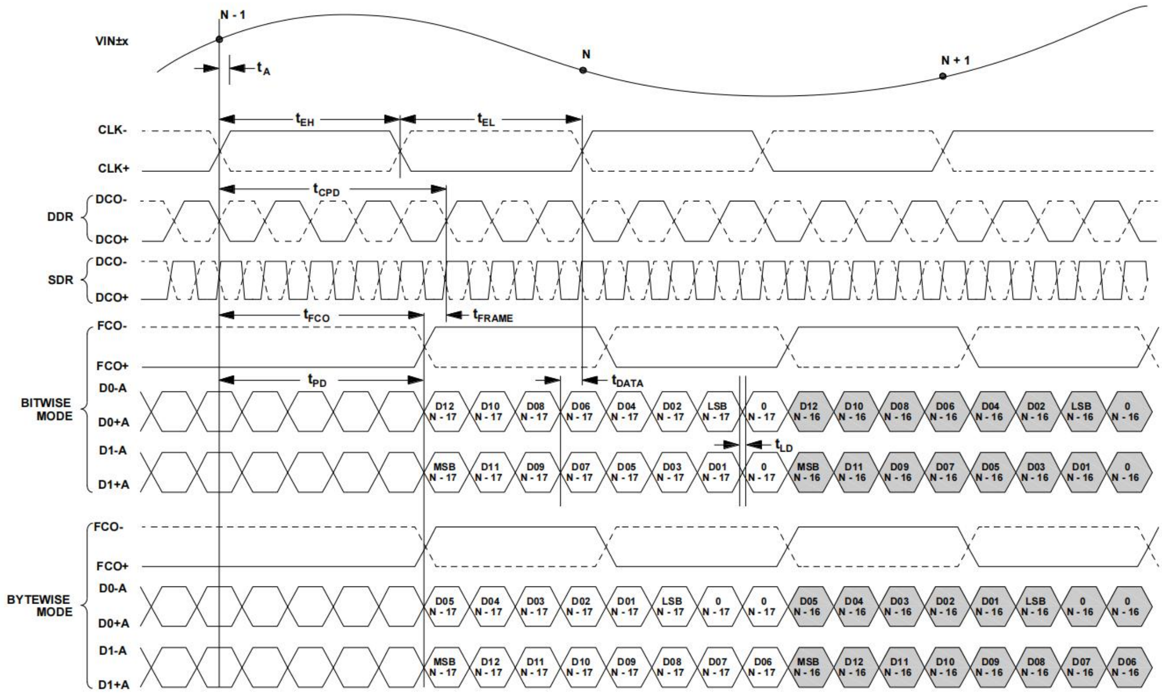


Figure9.1 16-Bit DDR/SDR, Two-Lane, 1×Frame(Default)Working sequence diagram



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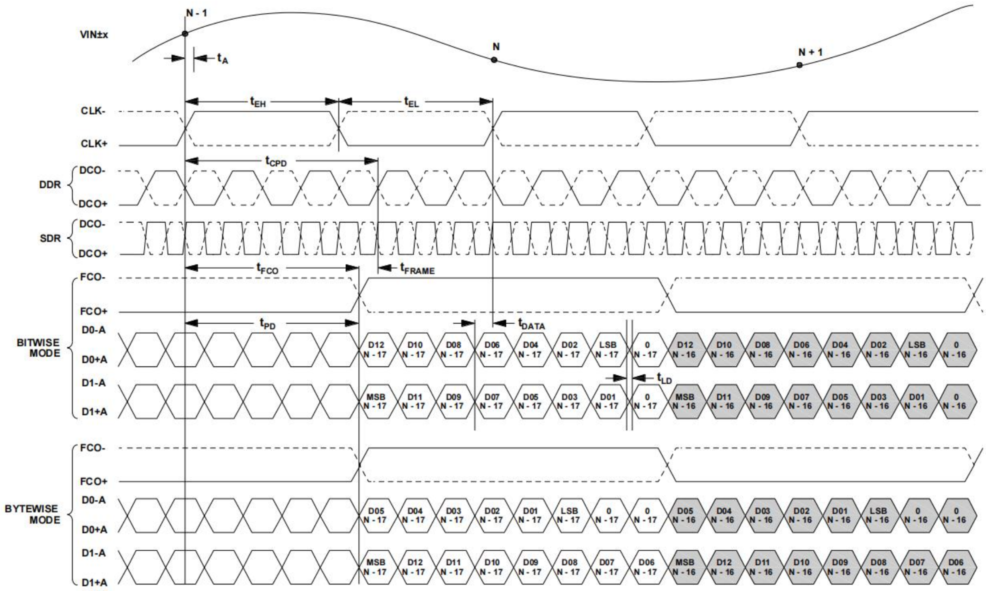


Figure9.2 16-Bit DDR/SDR, Two-Lane, 2×Frame Working sequence diagram

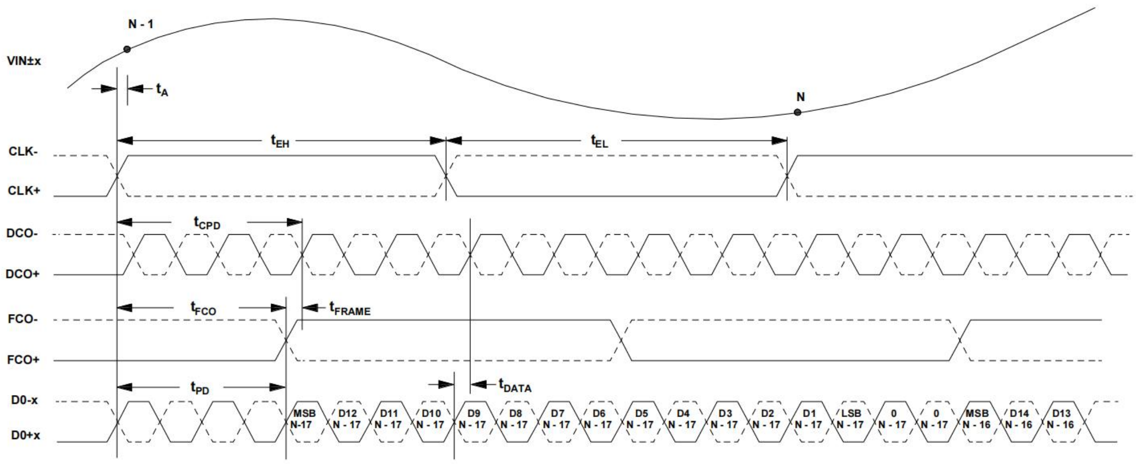


Figure9.3 16-Bit DDR, One-Lane,1×Frame Working sequence diagram



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## 9.2 SPI Interface timing

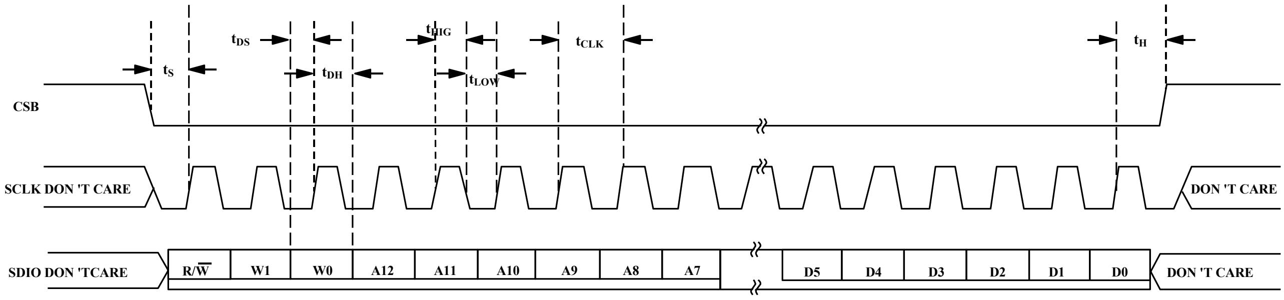


Figure9.4 Serial port interface timing

TABLE9.2 SPI Timing parameters

| parameter | condition | Limits |
|---|---|---|
| $t_{DS}$ | Data withSCLK Settling time between rising edges | 2ns, minimum |
| $t_{DH}$ | Data withSCLK Hold time between rising edges | 2ns, minimum |
| $t_{CLK}$ | SCLK cycle | 40ns, minimum |
| $t_{S}$ | CSB WithSCLK Establishment time between | 2ns, minimum |
| $t_{H}$ | CSB WithSCLK Hold time between | 2ns, minimum |
| $t_{HIG}$ | SCLK High-level pulse width | 10ns, minimum |
| $t_{LOW}$ | SCLK Low-level pulse width | 10ns, minimum |




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## 10.0 Working Principle

CW9253-125 It is a multi-stage, pipeline typeADC, each level provides sufficient overlap to correct the upper levelFlash Error. The quantized outputs of each stage are combined in oneIn the digital correction logic, a14 Bit conversion result. Serializer starts with14 The bit output format sends this converted data. The pipelined architecture allows the first stage to handle newThe sample is entered while the other stages continue to process the previous sample. Sampling takes place on the rising edge of the clock. Except for the last stage, each stage of the pipeline consists of a low-resolutionFlashTypeADCA switched capacitor connected theretoDAC And an interstage margin amplifier(Such as multiplicative digital-to-analog converter(MDAC)Composition. Amplification and reconstruction of margin amplifierDAC Output withFlash Type input difference to be supplied to the next stage of the pipeline. In order to helpFlash The error is digitally corrected, and the redundancy amount of one bit is set for each stage. The last level consists only ofoneFlash TypeADC Composition. The output stage module can realize data alignment, error correction, and transmit data to the output buffer. The data is then serialized and aligned with the frame and data clock.

## 10.1 Analog input network

ADCThe best performance of is achieved by differentially driving analog inputs. Using a differential dual-balun configuration to driveCW9253-125, providing excellent performance andFlexibleADC Interface（See figure10.1）。 When the input frequency is in the second or higher Nyquist region, the noise performance of most amplifiers cannot meet the requirements to achieve CW9253-125 GenuineSNR Performance, differential transformer coupling is the recommended input configuration（See figure10.2）。 Regardless of configuration, shunt capacitorsC1 The value of depends on the input frequency and may need to be reduced or removed.

Use VIN-to connect the common mode voltage and VIN + to connect the input signal to the input network mode. This input mode will cause the chip SNR to deteriorate, so it is not recommended to single-ended drive the CW9253-125 input

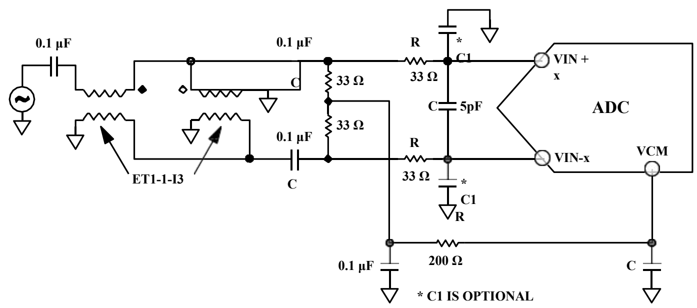


Figure10.1 Differential dual balun input configuration

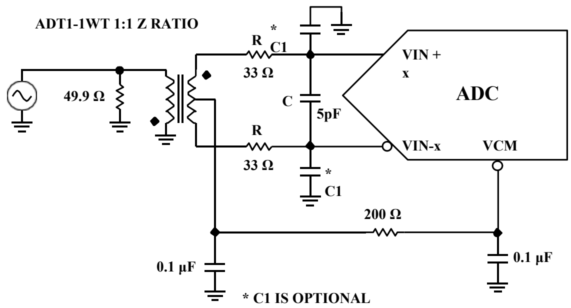


Figure10.2 Coupling input configuration of differential transformer

**10.2** Clock input network

To give full play to the performance of the chip, a differential signal should be used asCW9253-125 Sampling clock input（CLK +/-）The clock signal. The input clock pin has internal biasNo external bias is required. It is recommended to sample the RF transformer configuration, as shown in Figure10.3 Shown in. A back-to-back Schottky diode connected across the transformer may provide input toCW9253-125 MiddleThe clock signal is limited to about the differential0. 8V Peak-to-Peak. In this way, the large voltage swing of the clock can be prevented from being fed through to other parts, and the rapid rise and fall of the signal can be preservedThis is very important for low jitter performance.

CW9253-125 Has a flexible clock input structure.CMOS、LVDS、LVPECL Or a sine wave signal can be used as its clock input signal. Regardless of which signal is used, clock source jitter must be taken into account(See Jitter Considerations section for description)。 Figure10.2 ForCW9253-125 Preferred Method of Providing Clock Signals(The clock rate before internal clock division can reach1GHz)。 The single-ended signal of a low-jitter clock source can be converted into a differential signal using an RF transformer or RF balun. For125 MHzTo1 GHz Clock frequency, recommendedRF balun configuration; For20MHzTo200 MHz Clock frequency, it is recommended to use RF transformer configuration. Cross-connected to transformer/Back-to-back Schottky Two on Balun Secondary WindingThe pole tube can input toCW9253-125 The clock signal in is limited to approximately differential0.8 V Peak-to-Peak. In this way, it is possible to prevent the large voltage swing of the clock from feeding through toCW9253-125 OfIn other parts, the fast rise and fall time of the signal can also be preserved, which is very important to achieve low jitter performance. However, when the frequency is higher than500 MHzTime, the two poles



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The tube capacitance makes a difference. Care must be taken to select the appropriate signal limiting diode.

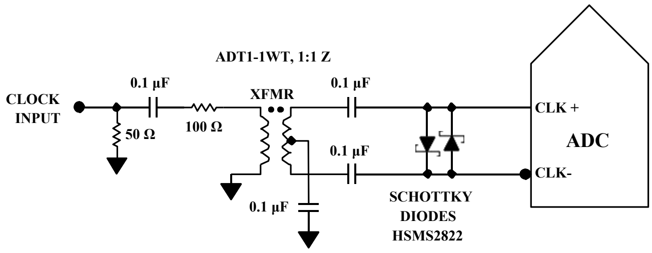

Figure10.3 Clock input configuration

## 10.3 Baseline configuration method

The CW9253-125 has a built-in stable, accurate voltage reference. The VREF can be configured with an internal 1.0 V reference voltage, an externally applied 1.0 V to 1.3 V reference voltage, or an external resistor applied to the internal reference voltage to produce a reference voltage according to the user's choice. For a summary of the various reference modes, see the Internal Reference Connection section and the External Reference Configuration section. The VREF pin shall be bypassed to ground by an external parallel combination of a low ESR 0.1 uF ceramic capacitor and a low ESR 1.0 uF capacitor

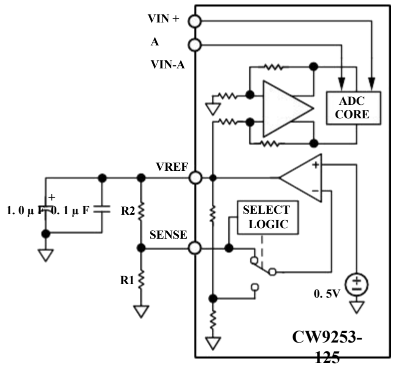

Figure10.4 Programmable internal reference configuration

TABLE10.1 Reference Voltage Configuration Summary

| Selected mode | SENSE Voltage | Corresponding$V_{REF}$（V） | Corresponding scoring range（Vpp） |
|---|---|---|---|
| Fixed internal reference voltage | AVDD To0.2 | 1.0, internal | 2 |
| Programmable internal voltage reference | External resistor configuration | 0.5×（1 + R2/R1） | 2 × $V_{REF}$ |
| Fixed external reference voltage | AGND to 0.2 | 1.0 To1.3, by external$V_{REF}$ Pin offers | 2.0~2.6 |

10.4 Digital output format

The CW9253-125 output driver is an LVDS interface, and the timing is shown in Figure 9.1. The output driver should be able to provide sufficient output current to drive various logic circuits, and the driving force can be adjusted by registers. However, large drive currents may lead to glitch pulses in the power supply signal, affecting the performance of the converter. Therefore, external buffers or latches may be required in applications that require an ADC to drive large capacitive loads or large fan-outs. The format of the output data defaults to binary complement. See Table 10.2 for an example of the output encoding format. To change the output data format to offset binary code, please refer to the "Memory Mapping" section.

In DDR mode, data from each ADC is serialized and provided through different channels. The data rate of each serial stream is equal to 14 bits times the sampling clock rate, and the maximum value is 500 Mbps per channel [(16 bits × 125 MSPS)/(2 × 2) = 500 Mbps/channel]. The typical minimum conversion rate is 20 MSPS. For more information on using this feature, see the "Memory Mapping" section.

To help capture data from the CW9253-125, the device provides two output clocks. The DCO is used to timing the output data. In the default operation mode, it is equal to 4 times the sampling clock (CLK) rate. Data is output from CW9253-125 one by one and must be captured on the rising and falling edges of the DCO; DCO supports double data rate (DDR) capture.

The FCO is used to indicate the start of a new output byte, and in 1 × frame mode, it is equal to the sampling clock rate. See the Timing Diagram section for more information

| Input（V） | condition | Offset binary mode | Binary complement pattern |
|---|---|---|---|
| VIN + - VIN- | <-VREF – 0.5 LSB | 0000 0000 0000 0000 | 1000 0000 0000 0000 |
| VIN + - VIN- | =-VREF | 0000 0000 0000 0000 | 1000 0000 0000 0000 |
| VIN + - VIN- | =0 | 1000 0000 0000 0000 | 0000 0000 0000 0000 |
| VIN + - VIN- | = + VREF – 1LSB | 1111 1111 1111 1100 | 0111 1111 1111 1111 |
| VIN + - VIN- | > + VREF- 0.5 LSB | 1111 1111 1111 1100 | 0111 1111 1111 1111 |

When using SPI, the DCO phase can be adjusted in 60 ° increments with respect to one data period (30 ° with respect to one DCO period). This enables users to optimize system timing margins as needed. As shown in Figure 9.1, the default DCO ± output data edge timing is 180 ° relative to a data cycle (90 ° relative to a DCO cycle).

In the default mode, as shown in Figure 9.1, the MSB is first in the data output serial stream. This can be reversed by using SPI so that the LSB is in the first place in the data output serial stream.

**10.5 Output Test Mode**

The Output Test options are described in Table 10.3 and are controlled by the Output Test Mode bit at address 0x0D. When the output test mode is enabled, the analog part of the ADC is disconnected from the digital back-end block and the test mode runs through the output format block. Some test modes are constrained by the output format, others are not. The PN generator in the PN sequence test can be reset by setting bit 4 or bit 5 of register 0x0D. These tests can be performed on an analog signal (which is ignored if present) but requires a clock signal.

Table 10.3 Flexible output test modes

| Output measurement Trial mode Bit sequence | Schema Name | Digital output word1 | Digital output word2 | Accept data format selection | annotation |
|---|---|---|---|---|---|
| 0 | Off (default) | N/A | N/A | N/A | |
| 1 | Intermediate level short code | 1000 0000 0000 0000(16-bit) | N/A | Yes | Offset binary code |
| 10 | Positive full scale | 1111 1111 1111 1111(16-bit) | N/A | Yes | Offset binary code |
| 11 | Negative full scale | 0000 0000 0000 0000(16-bit) | N/A | Yes | Offset binary code |
| 100 | Checkerboard form | 1010 1010 1010 1010(16-bit) | 0101 0101 0101 0101(16-bit) | No | |
| 101 | PNCode length sequence | N/A | N/A | Yes | PN23 ITU 0.150 $X^{23}+ X^{18}+1$ |
| 110 | PNCode short sequence | N/A | N/A | Yes | PN9 ITU 0.150$X^{9}+ X^{5}+1$ |
| 111 | 1/0 Word flip | 111 1111 1111 1111(16-bit) | 0000 0000 0000 0000(16-bit) | No | |
| 1000 | User input | Register 0x19 to Register 0x1A | Register 0x1B to Register 0x1C | No | |
| 1001 | 1/0 bitFlip | 1010 1010 1010 1010(16-bit) | N/A | No | |
| 1010 | 1 × sync | 0000 0001 1111 1111(16-bit) | N/A | No | |
| 1011 | 1Bit high level | 1000 0000 0000 0000(16-bit) | N/A | No | Test code associated with external pins |
| 1100 | Mixing frequency | 1010 0001 1001 1100(16-bit) | N/A | No | |

TABLE10.4 PN Sequence

| Sequence | Initial value | The first three output samples（MSB Prioritize） Binary complement |
|---|---|---|
| PNCode short sequence | 0x7F83 | 0x5F17，0xB209，0xCED1 |
| PNCode length sequence | 0x7FFF | 0x7E00，0x807C，0x801F |

For information on how to change these additional digital output timing characteristics via SPI, see the Register List.

**10.6 CSB Pin**

For applications that do not require SPI mode operation, the CSB pin should be connected to the AVDD. By setting CSB to high, all SCLK and SDIO information will be ignored.

When the CSB pin is connected to the AVDD, the CW9253-125, DCS is turned on by default and remains on until the device enters SPI mode and is controlled by SPI.

**10.7 RBIAS Pin**

The CW9253-125 requires the user to place a 10 kΩ resistor between the RBIAS pin and ground. The series resistor is used to set the main reference current of the ADC core, and the resistor tolerance is at least 1%.

**10.8 Serial Port Interface (SPI)**

The CW9253-125 Serial Port Interface (SPI) allows users to configure the corresponding function registers within the ADC to meet the needs of specific functions and operations. Through the serial port, the address space can be accessed and read and written to the address space. The SPI of this ADC consists of three parts: the SCLK pin, the SDIO pin and the CSB pin. The SCLK (serial clock) pin is used to synchronize the read and write data of the ADC; The SDIO (Serial Data Input/Output) dual function pin allows data to be sent to or read from internal registers; The CSB (Chip Select Signal) pin is a low-level active control pin, which enables or disables read and write cycles.

The timing requirements are shown in Figure 9.4



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## 11.0 Application Information

### 11.1 Power and Grounding Recommendations

It is recommended to use two separate 1.8 V power supplies to power the CW9253-125: one for the analog side AVDD and one for the digital output side DRVDD. For AVDD and DRVDD, multiple different decoupling capacitors should be used to support high and low frequencies. Decoupling capacitors should be placed close to the PCB entry point and close to the device pins, with as short trace length as possible.

The CW9253-125 requires only one PCB ground plane. Reasonable decoupling and clever separation of PCB analog, digital and clock modules makes it easy to achieve optimal performance.

### 11.2 Recommendations for exposed pad heat sinks

For optimal electrical and thermal performance, the exposed pads at the bottom of the ADC must be connected to the analog ground AGND. The exposed continuous copper plane on the PCB should match the exposed pads of the CW9253-125. There should be multiple vias on the copper plane in order to obtain the lowest possible thermal resistance path for heat dissipation through the bottom of the PCB. These vias should be filled or plugged to prevent tin infiltration of the vias and affecting the connection performance. In order to maximize the coverage and connection between the ADC and the PCB, a silk screen layer should be covered on the PCB to divide the continuous plane on the PCB into multiple equal parts. In this way, multiple connection points can be provided between the ADC and the PCB during the reflow soldering process. A continuous, undivided plane can only guarantee a connection point between the ADC and the PCB.

### 11.3 VCM

The VCM pin should be decoupled to ground through a 0.1 uF capacitor.

### 11.4 Voltage reference decoupling

The VREF pin should be decoupled to ground by an external parallel connection of a low ESR 0.1 uF ceramic capacitor and a low ESR 1.0 uF capacitor.

### 11.5 SPI Port

The SPI port should be disabled when the converter is required to give full play to its full dynamic performance. Typically the SCLK signal, CSB signal, and SDIO signal are asynchronous with the ADC clock, so the noise in these signals can degrade converter performance. If other devices use the on-board SPI bus, a buffer may need to be connected between this bus and the CW9253-125 to prevent these signals from changing at the input of the converter during the critical sampling period.



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## 12.0 Register List

Register mapping is broadly divided into the following parts: chip configuration registers, device index registers, and transfer registers, and globalADC Function registers including settings,Control and test functions.

| ADDR（HEX） | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0（LSB） | Default (HEX) | annotation |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Chip configuration register | | | | | | | | | | | |
| 0x00 | SPIPort configuration | 0 = SDO Effective | LSB Prioritize | Soft ComplexBit | 1 = 16-bit address | 1 = 16-bit address | Soft ComplexBit | LSB Prioritize | 0 = SDO Effective | 0x18 | The ADC default is 16-bit mode |
| 0x01 | ChipID | | | | | | | | | 0xB5 | ChipID, read-only |
| 0x02 | Chip grade | disable | Chip speed rating | | | disable | disable | disable | disable | | Chip speed rating, read-only |
| Device index and transfer register | | | | | | | | | | | |
| 0x04 | Device Index | disable | disable | | | | | | | | |
| 0x05 | Device Index | disable | disable | Clock channel DCO | Clock channel FCO | DatacomTao D | Data Channel C | Data channels B | Data ChannelA | 0x3F | Determining which channel on the chip receives the next write command; The default value is all channels on chip |
| 0xFF | transmission | disable | disable | disable | disable | disable | disable | disable | cover | 0x00 | Set sampling rate override |
| overall situation**ADC**Function register | | | | | | | | | | | |
| 0x08 | Power consumption mode (FullBureau | disable | disable | External power down pin function 0=FinishDrop it allElectricity1=To wait Machine | disable | disable | disable | Power consumption mode 00=Work normally 01=Complete power loss 10=await the opportune moment 11=restoration | | 0x00 | Determine the general operating mode of the chipFormula |
| 0x09 | Clock (global） | disable | disable | disable | disable | disable | disable | disable | Duty cycle stabilization 0=Open 1=Close | 0x01 | Duty cycle stabilizer (Difference from imports） |
| 0x0B | Clock division (FullBureau） | disable | disable | disable | disable | disable | Clock division ratio[2:0] 000=1 Frequency division 001=2 Frequency division 010=3 Frequency division 011=4 Frequency division 100=5 Frequency division 101=6 Frequency division 110=7 Frequency division 111=8 Frequency division | | | 0x00 | |
| 0x0D | Test Mode (local） | User input test mode | | restoration PN Long sequence Column | restoration PN Short sequence Column | Output test mode[3:0]（Local） 0000=Closed (Default） 0001=Intermediate level short sequence 0010=Positive full scale 0011=Negative full scale 0100=Alternating checkerboard form 0101 = PN 23 Sequence 0110 = PN 9 Sequence 0111=1/0 Word inversion 1000=User Defined 1001=1×synchronization 1011=1 Bit high level 1100=Mixing frequency （Specific output format reference table11.3） | | | | 0x00 | Test mode enabled, not subject to modeInfluence of pseudo-input signal |
| 0x10 | Offset adjustment (BureauDepartment） | 8 Bit device offset adjustment, bit[7:0] Offset adjustment toLSB, from+127 To-128（Binary complement） | | | | | | | | 0x00 | Device offset adjustment |
| 0x14 | Output Mode | disable | 0 = LVD S-ANSI 1 = LVD S-IEEE LVDS Output swing | disable | disable | disable | Output Reverse direction（） | disable | Output Format 0 = Offset Binary 1 = binary complement (global) | 0x01 | Configure output and data formats |
| 0x15 | Output adjustment | disable | Output driver termination 00=without 01 = 200 Ω 10 = 100 Ω 11 = 100 Ω | | disable | disable | disable | | Output drive 0=1×Drive 1=2×Drive | 0x00 | LVDS Output configuration |
| 0x16 | Output phase | disable | Input clock phase adjustment [6: 4] (input whose value is phase delay Number of clock cycles) | | | Output clock phase adjustment[3:0] (0000 To1011) | | | | 0x03 | On devices that utilize global clock division, it is decided which phase of the divider output is used to provide the output clock. Internal latches are not affected. |



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| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x18 | VREF Adjustment | disable | disable | disable | disable | disable | VREF Adjustment scheme[2:0]<br>000 = 1.0 Vpp（1.3 Vpp）<br>001 = 1.14 Vpp（1.48 Vpp）<br>010 = 1.33 Vpp（1.73 Vpp）<br>011 = 1.6 Vpp（2.08 Vpp）<br>100 = 2.0 Vpp（2.6 Vpp） | | | 0x04 | Adjust the interiorVREF Value |
| 0x19 | User _ PATT 1 _ LSBoverall situation) | | | | | | | | | | User-defined tests1LSB |
| 0x1A | User _ PATT 1 _ MSBoverall situation) | | | | | | | | | | User-defined tests1MSB |
| 0x1B | User _ PATT 2 _ LSBoverall situation) | | | | | | | | | | User-defined tests2LSB |
| 0x1C | User _ PATT 2 _ MSBoverall situation) | | | | | | | | | | User-defined tests2MSB |
| 0x21 | Serial output datacontrol(overall situation) | LVDS Output LSB Excellent First | SDR/DDR Single/Dual-channel, one-by-oneBit/Byte by byte[6:4]<br>000=SDR Dual-channel, bit-wise<br>001=SDR Dual-channel, byte-by-byte<br>010=DDR Dual-channel, bit-wise<br>011=DDR Dual-channel, verbatimSection<br>100=DDR Single channel, verbatim | | | disable | Select 2X Frame | Serial output bits<br>00=16 Bit | | 0x30 | Serial Stream Control. Defaults to<br>MSB Priority, |
| 0x22 | Serial channel status (local） | disable | disable | disable | disable | disable | disable | Channel output reset | Channel power down | 0x00 | Used to turn off each of the convertersPart |
| 0x100 | Sampling rate coverage | disable | Operate to makecan | 0 | 0 | disable | Sampling rate<br>000 = 20 MSPS<br>001 = 40MSPS<br>010 = 50 MSPS<br>011 = 65MSPS<br>100 = 80 MSPS<br>101 = 105 MSPS<br>110 = 125 MSPS | | | 0x00 | Sampling rate coverage |
| 0x109 | synchronization | disable | disable | disable | disable | disable | disable | Synchronous pulse with next onlysynchronization | Enable synchronization | 0x00 | |



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## 13.0 Encapsulation information

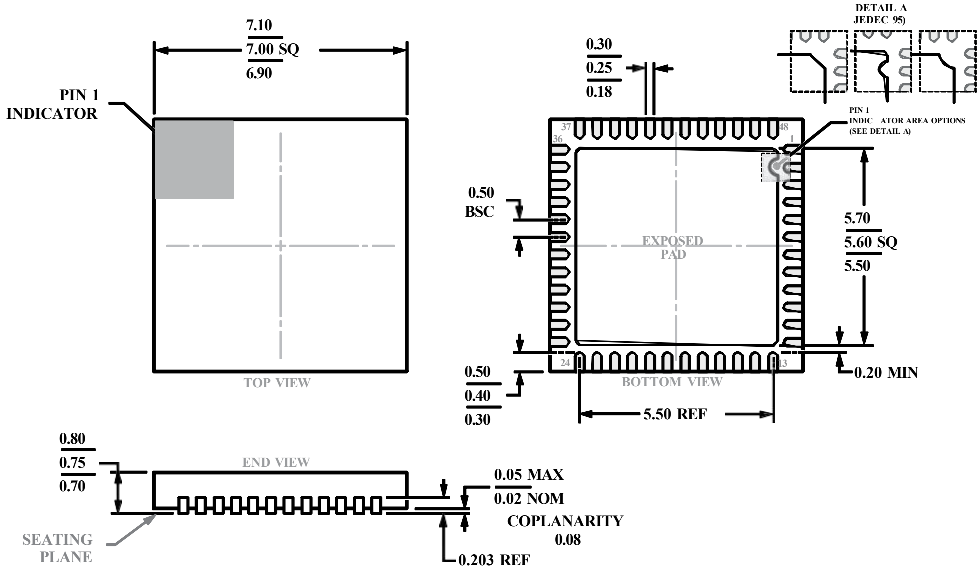


Figure13.1 CW9253-125 Package profile

### 13.1Order information

| Order model | Operating temperature | Encapsulation form | Execution Standard（Quality grade） |
|---|---|---|---|
| CW9253-125E | -55℃~+125℃ | QFN-48 | Military warm level |




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