CW7606 Data sheet
Eight-channel16-Bit，200kSPS Synchronous samplingADC

1.0 Overview

CW7606 has eight built-in 16Bit fast, low-power successive approximation ADCs.

Supports 8 channels of synchronous sampling. The conversion rate of each channel ADC of this ADC

Up to 200kSPS.

The CW7606 supports conversion between ± 10 V and ± 5 V using only 5V power supply

The true bipolar input signal of.

In order to simplify the PCB design of the data acquisition system, CW7606 has built-in

1MΩ input impedance input buffer and anti-aliasing filter for direct acquisition

Set analog signals. CW7606 integrates flexibly configurable, high-precision voltage reference

Generators and buffers.

CW7606 supports parallel mode or serial mode through different connections of hardware pins

Connect mode to configure. This function is the interface between the device and the microprocessor or DSP

Connection creates a variety of connection conditions.

The CW7606 is available in a 64-pin LQFP package.

2.0 Application

Power line monitoring and protection system

Multiphase motor control

Instrumentation and control systems

Multi-axis positioning system

Data acquisition system

3.0 Features

8 independent ADCs

True bipolar analog input

Input signal range: ± 10 V, ± 5 V

Conversion rate: 200kSPS

Low power consumption: 108mW (internal reference, 200kSPS, 5V power supply)

On-chip voltage reference and buffer

Parallel and serial interface modes

High-speed serial interface compatible with SPI interface protocol

64-pin LQFP package and 64-pin CQFP package

4.0 Main Performance Indicators

ENOB: 14.5 Bit (typical value)

SNR: 90 dB (typical value)

SINAD: 89 dB (typical value)

SFDR:-105 dB (typical value)

INL: ± 1 LSB (typical value)

DNL: ± 0. 5 LSB (typical value)

Operating power consumption: 108mW (internal benchmark)

Operating temperature:-55 ℃ ~ + 125 ℃

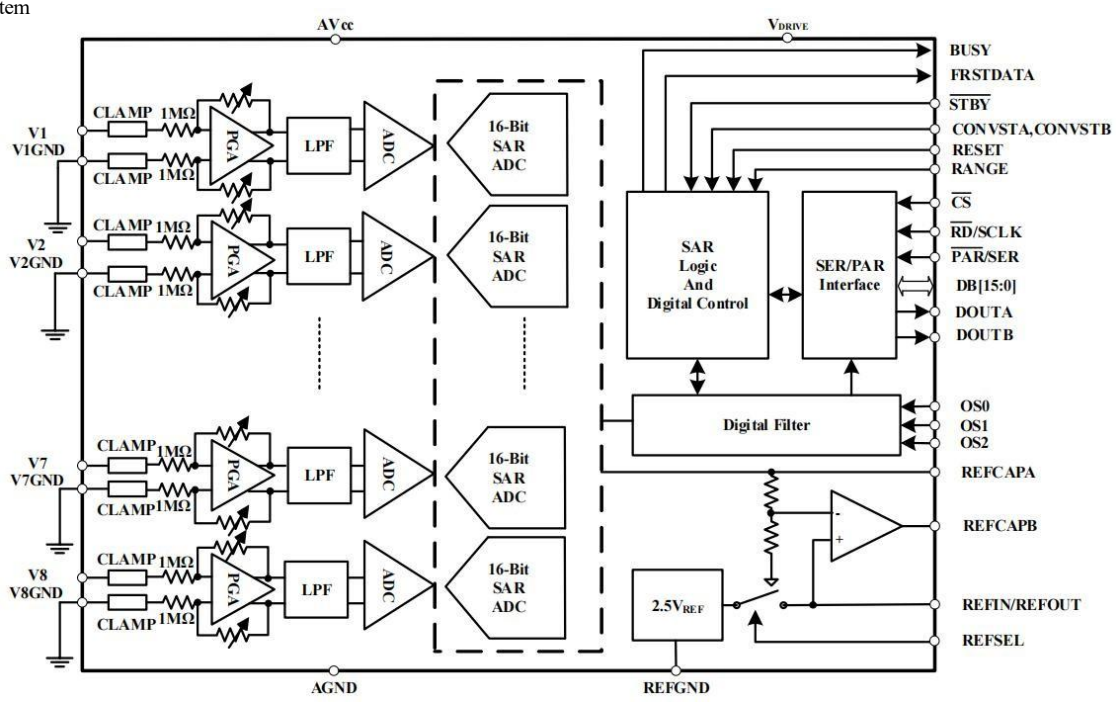

Figure 1. CW7606 System Block Diagram

6.0 Technical specifications

Unless otherwise stated, internal/The external reference voltages areVREF= 2.5 V，AVCC= 4.75 VTo5.25 V，VDRIVE= 2.5 VTo5.25 V，*f*SAMPLE= 200kSPS。

TABLE1

parameter	Test conditions/annotation	Minimum	Typical value	Maximum	Units
Dynamic performance	f_{in}= 1.1 kHz Sine wave, unless otherwise stated				
Signal ratio（SINAD）	No oversampling,± 10 V scope		87 90		dB
	No oversampling,± 5 V scope		86.5 89		dB
Signal-to-noise ratio（SNR）	No oversampling,± 10 V scope		88 90		dB
	No oversampling,± 5 V scope		87.5 89		dB
	Oversampling, see table**5**				
Total harmonic distortion（THD）	No oversampling,± 10 V scope		-100		dB
	No oversampling,± 5 V scope		-100		dB
Peak harmonic or spurious noise	No oversampling,± 10 V scope		-105		dB
（SFDR）	No oversampling,± 5 V scope		-105		dB
Full power bandwidth	-3 dB，± 10 V scope		22		kHz
	-3 dB，± 5 V scope		15		kHz
Channel isolation	Unselected channelsf_{in} Up to160kHz		-100		dB
DC accuracy					
Resolution			16		Bit
No missing code			16		Bit
Integral nonlinearity（INL）			±1	±2	LSB
Differential nonlinearity（DNL）			±0.5	±0.99	LSB
Bipolar zero level error			±2	±6	LSB
Positive full scale error	± 10 V scope		±8	±32	LSB
	± 5 V scope		±10	±32	LSB
Positive full scale error drift	± 10 Vscope/Internal benchmark		±5		ppm/℃
	± 5 V scope/Internal benchmark		±5		ppm/℃
Positive full-scale error matching	± 10 V scope		5	32	LSB
	± 5 V scope		10	40	LSB
Negative full-scale error	± 10 V scope		±8	±32	LSB
	± 5 V scope		±10	±32	LSB
Negative full-scale error drift	± 10 Vscope/Internal benchmark		±5		ppm/℃
	± 5 V scope/Internal benchmark		±5		ppm/℃
Negative full-scale error matching	± 10 V scope		5	32	LSB
	± 5 V scope		10	40	LSB
Analog input					
Input voltage range	RANGE = 1	−10		10	V
	RANGE = 0	−5		5	V
Input capacitance			5		pF
Analog input current		−10		10	μA
Input impedance			1		MΩ
Reference voltage input/Output Range					
Reference output voltage			2.5		V
Voltage reference temperature coefficient			±5	±12	ppm/℃
Logic input					
Input high voltage（V_{INH}） Input low voltage（V_{INL}）		0.7 * V_{DRIVE}		0.1 * V_{DRIVE}	V V
Logic output					
Output high voltage（V_{OH}） Output low voltage（V_{OL}）	I_{SOURCE}= 100 μA I_{SINK}= 100 μA	V_{DRIVE}-0.2		0.2	V V

TABLE1-Continued

parameter	Test conditions/annotation	Minimum	Typical value	Maximum	Units
Dynamic performance	f_{in}= 1.1 kHz Sine wave, unless otherwise stated				
Signal ratio（SINAD）	No oversampling,± 10 V scope		87 90		dB
	No oversampling,± 5 V scope		86.5 89		dB
Signal-to-noise ratio（SNR）	No oversampling,± 10 V scope		88 90		dB
	No oversampling,± 5 V scope		87.5 89		dB
	Oversampling, see table**5**				
Total harmonic distortion（THD）	No oversampling,± 10 V scope		-100		dB
	No oversampling,± 5 V scope		-100		dB
Peak harmonic or spurious noise	No oversampling,± 10 V scope		-105		dB
（SFDR）	No oversampling,± 5 V scope		-105		dB
Full power bandwidth	-3 dB，± 10 V scope		22		kHz
	-3 dB，± 5 V scope		15		kHz
Channel isolation	Unselected channelsf_{in} Up to160kHz		-100		dB
DC accuracy					
Resolution			16		Bit
No missing code			16		Bit
Integral nonlinearity（INL）			±1	±2	LSB
Differential nonlinearity（DNL）			±0.5	±0.99	LSB
Bipolar zero level error			±2	±6	LSB
Positive full scale error	± 10 V scope		±8	±32	LSB
	± 5 V scope		±10	±32	LSB
Positive full scale error drift	± 10 Vscope/Internal benchmark		±5		ppm/℃
	± 5 V scope/Internal benchmark		±5		ppm/℃
Positive full-scale error matching	± 10 V scope		5	32	LSB
	± 5 V scope		10	40	LSB
Negative full-scale error	± 10 V scope		±8	±32	LSB
	± 5 V scope		±10	±32	LSB
Negative full-scale error drift	± 10 Vscope/Internal benchmark		±5		ppm/℃
	± 5 V scope/Internal benchmark		±5		ppm/℃
Negative full-scale error matching	± 10 V scope		5	32	LSB
	± 5 V scope		10	40	LSB
Analog input					
Input voltage range	RANGE = 1	−10		10	V
	RANGE = 0	−5		5	V
Input capacitance			5		pF
Analog input current		−10		10	μA
Input impedance			1		MΩ
Reference voltage input/Output Range					
Reference output voltage			2.5		V
Voltage reference temperature coefficient			±5	±12	ppm/℃
Logic input					
Input high voltage（V_{INH}）Input low voltage（V_{INL}）		0.7 * V_{DRIVE}		0.1 * V_{DRIVE}	V V
Logic output					
Output high voltage（V_{OH}）Output low voltage（V_{OL}）	I_{SOURCE}= 100 μA I_{SINK}= 100 μA	V_{DRIVE}-0.2		0.2	V V

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7.0 Timing specification

Unless otherwise stated, internal/The external reference voltages areVREF= 2.5 V，AVCC= 4.75 V To5.25 V，VDRIVE=2.5 V To5.25 V。

TABLE2

parameter	Description	Minimum	Typical value	Maximum	Units
tCYCLE	Throughput rate			5	μs
tCONV	Transition time	3.45	4	4.15	μs
tRESET	RESET High-level pulse width	50			ns
tOS _ SETUP	BUSY ToOS x Pin setting time	20			ns
tOS _ HOLD	BUSY ToOS x Pin hold time	20			ns
t1	CONVST x High toBUSY High Level			40	ns
t2	ShortestCONVST x Low level pulse	25			ns
t3	ShortestCONVST x High-level pulse	25			ns
t4	BUSYFalling edge toCSFalling edge setting time	0			ns
t5	CONVSTA/CONVSTB Maximum allowable delay between rising edges Interval			0.5	ms
t6	bestCSRising edge vsBUSY Maximum time between falling edges			25	ns
t7	RESET Low toCONVST x Shortest delay between high levels Late time	1			ms
t8	CSToRDSet time	0			ns
t9	CSToRDHold time	0			ns
t10	RDLow-level pulse width				
	VDRIVE Above4.75 V	16			ns
	VDRIVE Above3.3 V	21			ns
	VDRIVE Above2.7 V	25			ns
	VDRIVE Above2.5 V	32			ns
t11	RDHigh-level pulse width	15			ns
t12	CSHigh-level pulse width	22			ns
t13	FromCSUntilDB [15: 0]Delay time for tri-state disabling				
	VDRIVE Above4.75 V			16	ns
	VDRIVE Above3.3 V			20	ns
	VDRIVE Above2.7 V			25	ns
	VDRIVE Above2.5 V			30	ns
t14	RDData access time after falling edge				
	VDRIVE Above4.75 V			16	ns
	VDRIVE Above3.3 V			21	ns
	VDRIVE Above2.7 V			25	ns
	VDRIVE Above2.5 V			32	ns
t15	RDData retention time after falling edge	6			ns
t16	CSToDB [15: 0]Hold time	6			ns
t17	FromCSRising edge toDB [15: 0]Delay time of three-state enablement			22	ns
t18	FromCSToDOUTA/DOUTB Delay time for tri-state disabling/ FromCSToMSB Effective delay time				
	VDRIVE Above4.75 V			15	ns
	VDRIVE Above3.3 V			20	ns
	VDRIVE= 2.5 V To2.7 V			30	ns

TABLE2-Continued

parameter	Description	Minimum	Typical value	Maximum	Units
t_{19}	SCLK Data access time after rising edge				
	V_{DRIVE} Above4.75 V		17		ns
	V_{DRIVE} Above3.3 V		23		ns
	V_{DRIVE} Above2.7 V		27		ns
	V_{DRIVE} Above2.5 V		34		ns
t_{20}	SCLK Low-level pulse width	0.4 t_{SCLK}			ns
t_{21}	SCLK High-level pulse width	0.4 t_{SCLK}			ns
t_{22}	SCLK Rising edge to $D_{OUTA/D_{OUTB}}$ Effective hold time	7			ns
t_{23}	CSRising edge $D_{OUTA/D_{OUTB}}$ Tri-state enabling		22		ns
t_{24}	FromCSFalling edge untilFRSTDATA Delay time for tri-state disabling				
	V_{DRIVE} Above4.75 V		15		ns
	V_{DRIVE} Above3.3 V		20		ns
	V_{DRIVE} Above2.7 V		25		ns
	V_{DRIVE} Above2.5 V		30		ns
t_{25}	FromCSFalling edge untilFRSTDATA Delay time of high level, Serial mode				
	V_{DRIVE} Above4.75 V		15		ns
	V_{DRIVE} Above3.3 V		20		ns
	V_{DRIVE} Above2.7 V		25		ns
	V_{DRIVE} Above2.5 V		30		ns
t_{26}	FromRDFalling edge untilFRSTDATA Delay time at high level				
	V_{DRIVE} Above4.75 V		16		ns
	V_{DRIVE} Above3.3 V		20		ns
	V_{DRIVE} Above2.7 V		25		ns
	V_{DRIVE} Above2.5 V		30		ns
t_{27}	FromRDFalling edge untilFRSTDATA Delay time at low level				
	V_{DRIVE}= 3.3 V To5.25 V		19		ns
	V_{DRIVE}= 2.5 V To2.7 V		24		ns
t_{28}	From16 1SCLK Falling edge toFRSTDATALow-level delay Late time				
	V_{DRIVE}= 3.3 V To5.25 V		17		ns
	V_{DRIVE}= 2.5 V To2.7 V		22		ns
t_{29}	FromCSRising edge untilFRSTDATA Delay time of three-state enablement		24		ns
f_{SCLK}	Serial read clock frequency		20		MHz

8.0 Pin diagram

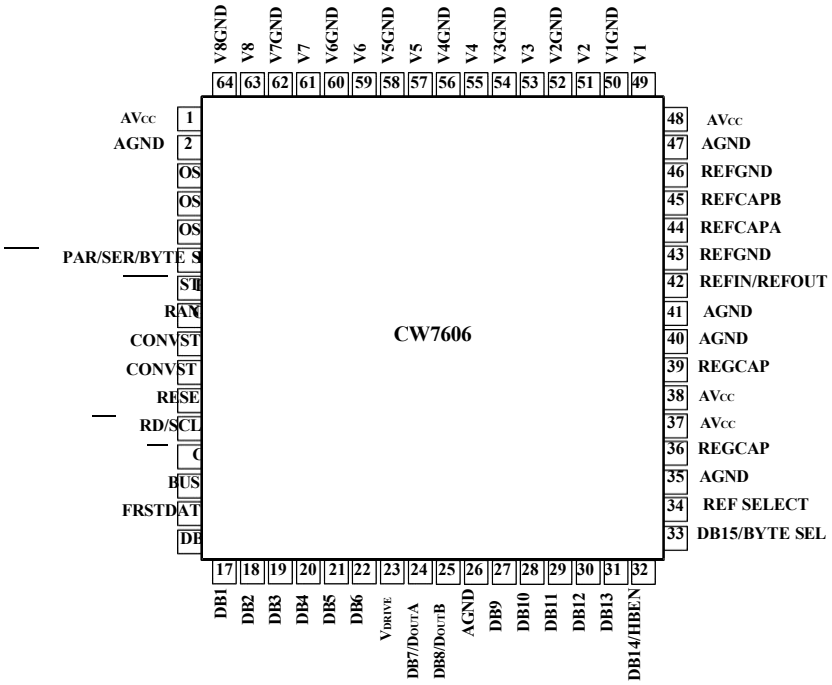

Figure2. CW7606 Pin diagram

TABLE**3**

Pin number	Pin Name	Description
1, 37, 38 ,48	AV_{CC}	Analog supply voltage, 4.75 V to 5.25 V. This is the supply voltage for the internal front-end amplifier and ADC core. These power pins should be decoupled to the AGND, and the 10μF and 100nF decoupling capacitors should be connected to the AVCC pins.
2, 26, 35, 40, 41, 47,	AGND	Analogically. These pins are the ground reference points for all analog circuits on the ADC. All analog input signals and external reference signals should be referenced to these pins. All 6 AGND pins should be connected to the AGND plane of the system.
5, 4, 3	OS[2:0]	Oversampling mode pin. Logic input. These pins are used to select the oversampling magnification. OS2 is the MSB control bit, and OS0 is the LSB control bit.
6	PAR/SER/BYTE SEL	Parallel/serial interface select input. Logic input. If this pin is connected to a logic low level, the parallel interface is selected. If this pin is connected to high, select the serial interface. If this pin is logically high and DB15/BYTE SEL is logically high, parallel byte interface mode is selected. In serial mode, the RD/SCLK pin is used as the serial clock input. DB7/DOUTA pins and The DB8/DOUTB pin is used as a serial data output. When selecting a serial interface, this pin should be DB [15: 9] and DB [6: 0] are grounded. In byte mode, DB 15 selects the parallel byte operation mode together with PAR/SER/BYTE SEL. The DB14 is used as the HBEN pin. DB [7: 0] transmits the 16-bit conversion result through 2 RD operations, and DB0 is the LSB of data transmission.
7	STBY	Standby mode input. This pin is used to put the ADC into one of two power-saving modes: standby mode or OFF mode. The power saving mode to enter depends on the status of the RANGE pin. In standby mode, all circuits except the on-chip reference voltage, regulator, and regulator buffer are turned off. In off mode, all circuits are turned off.
8	RANGE	Analog input range selection. Logic input. The polarity of this pin determines the input range of the analog input channel Circumference. If this pin is connected to a logic high level, the analog input range for all channels is ± 10 V. If this pin is connected to a logic low level, the analog input range for all channels is ± 5 V. This quote Changes in the logical state of the foot immediately affect the analog input range. For fast throughput applications, conversion Do not change the logical state of this pin during.
9, 10	CONVSTA CONVSTB	Transition start input A and Transition start input B. Logic input. These logic inputs are used to initiate analog input channel transitions. To sample all channels simultaneously, you can short CONVSTA and CONVSTB together and apply a transition start signal. Alternatively, synchronous sampling of V1, V2, V3, and V4 channels can be initiated with CONVSTA and V5, V6, V7, and V8 channels can be initiated with CONVSTB, only if oversampling is not turned on. When the CONVSTA and CONVSTB pins change from low to high, the front-end sample-and-hold circuit of the corresponding analog input is set to hold.

Pin number	Pin Name	Description
11	RESET	Reset input. When set to logic high, the RESET rising edge resets the ADC. The device should receive a RESET pulse after power-up. The RESET high pulse width is typically 50ns. If a RESET pulse is applied during the transition, the transition will be interrupted. If a RESET pulse is applied during a read, the contents of the output register are RESET to all zeros.
12	RD/SCLK	Parallel data read control input (RD) when parallel interface is selected/serial when serial interface is selected Clock input (SCLK). In parallel mode, if both CS and RD are logic low, the output bus is enabled. In serial mode, this pin is used as the serial clock input for data transfer. The falling edge of CS makes the data output lines DOUTA and DOUTB out of the three states, and outputs the MSB of the conversion result one by one. The SCLK rising edge sends all subsequent data bits to the serial data outputs DOUTA and DOUTB one by one.
13	CS	Film selection. This low active logic input enables data frame transmission. In parallel mode, if both CS and RD are logic low, the output bus DB [15: 0] is enabled, causing the conversion result to be output on the parallel data bus. In serial mode, CS is used to enable serial data frame transmission, and the most significant bits (MSB) of serial data are output one by one.
14	BUSY	Output busy. After both CONVSTA and CONVSTB reach the rising edge, this pin goes to a logical high level, indicating that the conversion process has begun. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of BUSY indicates that the conversion data is being latched to the output data register and is available for reading after the elapse of time t4. Data read operations performed when BUSY is high should be completed before the falling edge of BUSY. When the BUSY signal is high, the rising edges of CONVSTA and CONVSTB do not work.
15	FRSTDATA	Digital outputs. The FRSTDATA output signal indicates when to read back the first channel V1 on a parallel, byte, or serial interface. When the CS input is high, the FRSTDATA output pin is in tri-state. The CS falling edge takes FRSTDATA out of the three-state. In parallel mode, the RD falling edge corresponding to the V1 result then sets the FRSTDATA pin high, indicating that the output data bus can provide the V1 result. After the next falling edge of RD, the FRSTDATA output resumes a logic low level. In serial mode, FRSTDATA goes high on the CS falling edge. Because the MSB of V1 will be output on DOUTA at this time. At the 16th SCLK falling edge after the CS falling edge, it returns to low level.
22 To16	DB [6:0]	Data bits DB6 to DB0 are output in parallel. These pins act as tri-state parallel digital input/output pins when PAR/SER/BYTE SEL = 0. When both CS and RD are low, these pins are used to output the conversion results to DB6 to DB0. These pins should be connected to AGND when PAR/SER/BYTE SEL = 1.
23	V_{DRIVE}	Logic power input. The supply voltage of this pin (2.3 V to 5.25 V) determines the operating voltage of the logic interface. The nominal power of this pin is the same as the host interface power. This pin should be decoupled to the DGND, and the 10μF and 100nF decoupling capacitors should be connected to the VDRIVE pin.
24	DB7/D_{OUT}A	Parallel output data bit 7 (DB7)/serial interface data output pin (DOUTA). This pin acts as a tri-state parallel digital input/output pin when PAR/SER/BYTE SEL = 0. When both CS and RD are at low levels, this pin is used to output the conversion result DB7. When PAR/SER/BYTE SEL = 1, this pin serves as a DOUTA and outputs serially converted data. When working in parallel byte mode, DB7 is the MSB of this byte.
25	DB8/D_{OUT}B	Parallel output data bit 8 (DB8)/serial interface data output pin (DOUTB). This pin acts as a tri-state parallel digital input/output pin when PAR/SER/BYTE SEL = 0. When both CS and RD are at low levels, this pin is used to output the conversion result DB8. When PAR/SER/BYTE SEL = 1, this pin serves as a DOUTB and outputs serially converted data.
31 To27	DB [13:9]	The data bits DB 13 to DB 9 are output in parallel. These pins act as tri-state parallel digital input/output pins when PAR/SER/BYTE SEL = 0. When both CS and RD are at low levels, this pin is used to output the conversion results DB 13 to DB 9. These pins should be connected to AGND when PAR/SER/BYTE SEL = 1.
32	DB14/HBEN	Parallel output data bit 14 (DB14)/high byte enable (HBEN). When PAR/SER/BYTE SEL = 0, this pin acts as a tri-state parallel digital output pin. When both CS and RD are at low levels, this pin is used to output the conversion result DB 14. Works in parallel byte interface mode when PAR/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1. In parallel byte mode, the HBEN pin is used to select whether to output the high byte (MSB) or low byte (LSB) of the conversion result first. When HBEN = 1, the MSB is output first, and then the LSB is output. When HBEN = 0, the LSB is output first, and then the MSB is output.

Pin number	Pin Name	Description
33	DB15/BYTE SEL	Parallel output data bit 15 (DB15)/parallel byte mode selection (BYTE SEL). When PAR/SER = 0, this pin acts as a tri-state parallel digital output pin. When both CS and RD are at low levels, this pin is used to output the conversion result DB 15. When PAR/SER/BYTE SEL = 1, the BYTE SEL pin is used to select between serial interface mode and parallel byte interface mode. Operates in serial interface mode when PAR/SER/BYTE SEL = 1 and DB15/BYTE SEL = 0. Works in parallel byte interface mode when PAR/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1.
34	REFSELECT	Internal/external reference voltage select input. Logic input. If this pin is set to logic high, the internal reference mode is selected and enabled. If this pin is set to logic low, the internal reference voltage is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
36,39	REGCAP	Decoupling capacitor pin for internal regulator voltage output. Each of these pins should be decoupled to the AGND through a 1 μF capacitor. The voltage on these pins is in the range of 2.5 V to 2.7 V.
42	REFIN/REFOUT	Voltage reference input/output. If the REF SELECT pin is set to logic high, this pin provides a 2.5 V on-chip reference for external use. Alternatively, you can set the REF SELECT pin to logic low to disable the internal reference and apply a 2.5 V external reference to this input. This pin needs to be decoupled whether an internal or external reference voltage is used. A 10μF capacitor should be connected between this pin and ground near the REFGND pin.
43,46	REFGND	Voltage reference ground pin. These pins should be connected toAGND。
44,45	REFCAPA, REFCAPB	Reference buffer output force/detect pin. These pins must be connected together and decoupled to the AGND by a low ESR 10μF ceramic capacitor. The voltage on these pins is typically 4.0 V.
49	V1	Analog input 1. This pin is a single-ended analog input. The analog input RANGE for this channel is determined by the RANGE pin.
50	V1GND	Analog input ground pin. These pins correspond to analog input pins V1 through V8. All analog input AGND pins should be connected to the AGND plane of the system.
51	V2	Analog input2。
52	V2GND	Analog input2 Ground pin.
53	V3	Analog input3。
54	V3GND	Analog input3 Ground pin.
55	V4	Analog input4。
56	V4GND	Analog input4 Ground pin.
57	V5	Analog input5。
58	V5GND	Analog input5 Ground pin.
59	V6	Analog input6。
60	V6GND	Analog input6 Ground pin.
61	V7	Analog input7。
62	V7GND	Analog input7 Ground pin.
63	V8	Analog input8。
64	V8GND	Analog input8 Ground pin.

9.0 Typical performance parameters

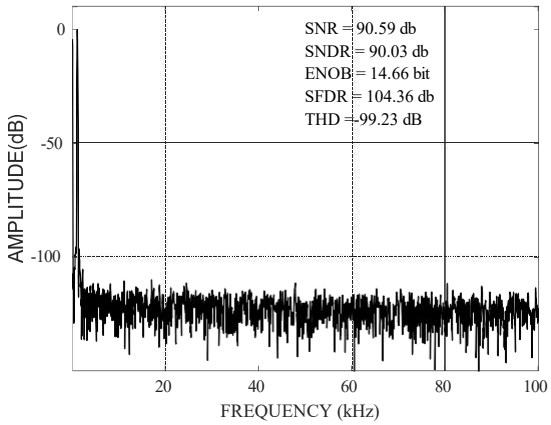

Figure3. CW7606 typicalFFT，± 10 VRange,

Parallelf_S= 200 kHz，f_{in}= 1.1 kHz，V_{IN} = ±9.5 V

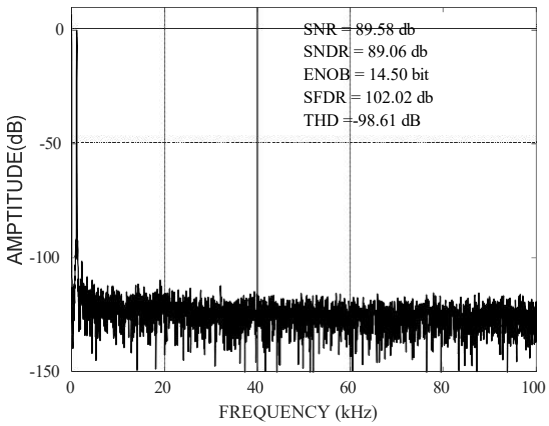

Figure4. CW7606 typicalFFT，± 5 VRange,

Parallelf_S= 200 kHz，f_{in}= 1.1 kHz，V_{IN} = ±4.8 V

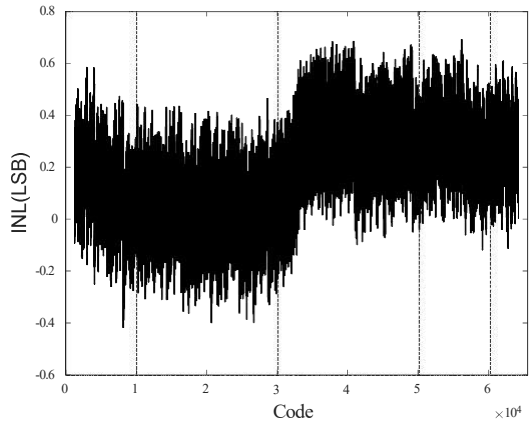

Figure5. CW7606 typicalINL，± 10 V Range,V_{IN} = ±9.8 V

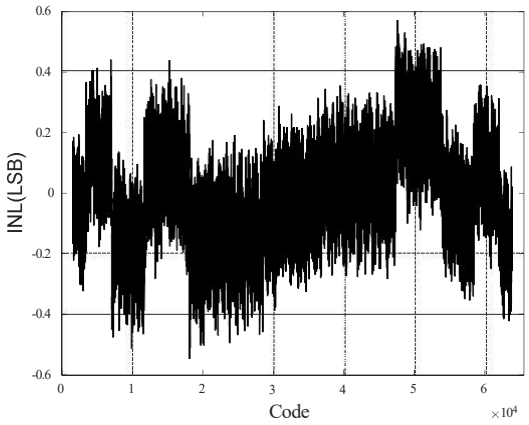

Figure6. CW7606 typicalINL，± 5 V Range,V_{IN} = ±4.8 V

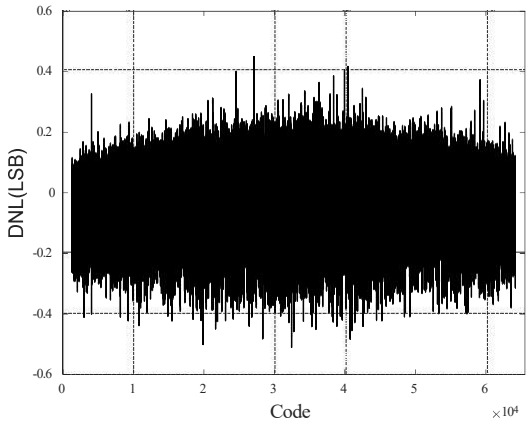

Figure7. CW7606 typicalDNL，± 10 VRange,V_{IN} = ±9.8 V

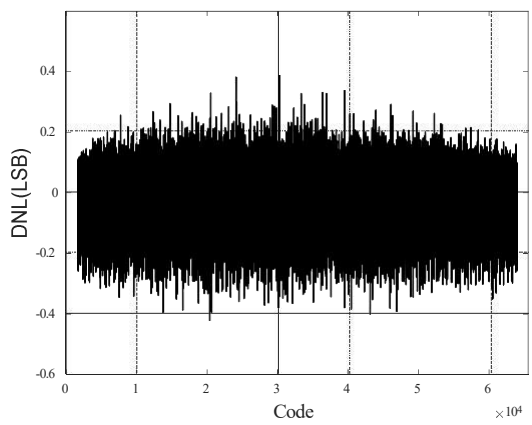

Figure8. CW7606 typicalDNL，± 5 V Range,V_{IN} = ±4.8 V

10.0Working Principle

10.1 Detailed explanation of converter

CW7606 is a data acquisition system using high-speed, low-power, charge redistribution successive approximation analog-to-digital converter (ADC), which can simultaneously sample 8 analog input channels. Its analog input can accept true bipolar input signals. The input RANGE of ± 10 V or ± 5 V can be selected using the RANGE pin. The CW7606 is powered by a 5V single power supply.

The CW7606 has built-in input clamp protection, input signal scaling amplifier, second-order anti-aliasing filter, sample and hold amplifier, on-chip reference, reference buffer, high-speed ADC, digital filter, and high-speed parallel and serial interfaces. The sampling of CW7606 is controlled by the CONVST signal.

10.2 Analog Inputs

Analog input range

The CW7606 handles true bipolar, single-ended input voltages. The logic level on the RANGE pin determines the analog input RANGE for all analog input channels. If this pin is connected to a logic high level, the analog input range for all channels is ± 10 V. If this pin is connected to a logic low level, the analog input range for all channels is ± 5 V. Changes in the logic state of this pin immediately affect the simulation

Enter the range. However, in addition to the normal acquisition time requirement, there is a setup time requirement with a typical value of about 80 μs. Establish the input RANGE based on the system signal, and set the RANGE pin by hardwiring.

Analog input impedance

The analog input impedance of the CW7606 is 1MΩ. This is a fixed input impedance and does not vary with the ADC sampling frequency. The high analog input impedance eliminates the need for a driver amplifier at the front end of the ADC, allowing it to be directly connected to a signal source or sensor. Because there is no need to drive the amplifier, the bipolar power supply in the signal chain (which is usually the noise source in the system) can be removed.

Analog input clamping protection

The figure below shows the analog input structure of the CW7606. Each analog input contains a clamp protection circuit. Although powered by a single 5V power supply, this analog input clamp protection allows input overvoltages to reach ± 22 V.

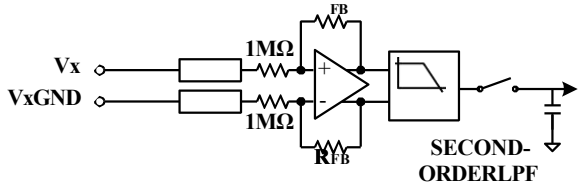

Fig. 9 Analog input circuit

When the input voltage does not exceed ± 22 V, there is no current in the clamp circuit. When the input voltage exceeds ± 22 V, the clamp circuit is turned on.

A series resistor should be placed on the analog input channel to limit the current to less than ± 10 mA when the input voltage exceeds ± 16. 5 V. If there is a series resistor on the analog input channel Vx, an equivalent resistor is also required on the analog input GND channel VxGND (see figure below). If there is no corresponding resistor on the VxGND channel, the channel will have an offset error.

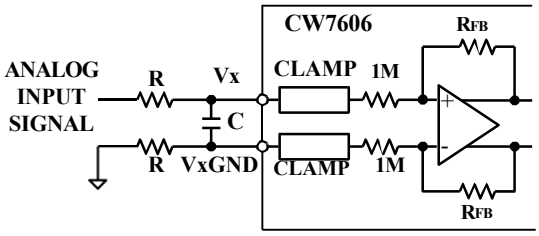

Figure 10 Input resistance matching on analog input

10.3 Internal/External Voltage Reference

The CW7606 has a built-in 2.5 V on-chip bandgap voltage reference. The REFIN/REFOUT pin can either use this 2.5 V reference voltage to internally generate a 4.0 V on-chip reference voltage or allow a 2.5 V external reference voltage to be applied. The applied 2.5 V external reference voltage is also amplified to 4.0 V by the internal buffer. This 4.0 V buffered reference voltage is the reference voltage used by the SAR ADC.

The REF SELECT pin is a logic input pin that allows the user to select an internal or external reference voltage. If this pin is set to logic high, the internal reference mode is selected and enabled. If this pin is set to logic low, the internal reference voltage is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After reset, the CW7606 operates in the reference voltage mode selected by the REF SELECT pin. The REFIN/REFOUT pin needs to be decoupled whether an internal or external reference voltage is used. The REFIN/REFOUT pin requires a 10μF ceramic decoupling capacitor.

10.4 Typical connection diagram

The diagram below shows a typical connection diagram for CW7606. The device has four AVCC power pins. Each of these four power pins should use a 100nF decoupling capacitor. A 10 μF capacitor is used for decoupling on the power side. The CW7606 operates with both an internal reference and an externally applied reference. In the configuration shown below, the CW7606 is configured to operate at an internal reference voltage. The REFCAPA and REFCAPB pins are short-circuited together and decoupled by a 10μF ceramic capacitor. The VDRIVE power supply is connected to the same power supply that powers the processor. The VDRIVE voltage controls the voltage value of the output logic signal.

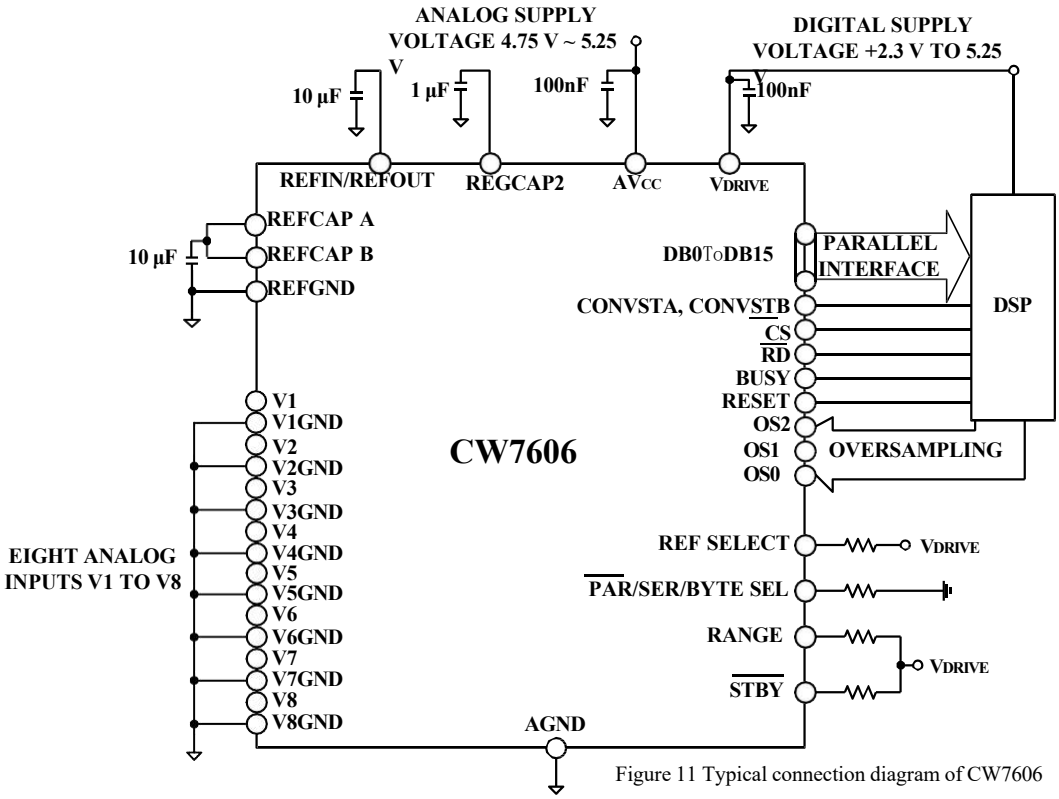

Figure 11 Typical connection diagram of CW7606

10.5 Transition Control

All analog input channels are sampled simultaneously

The CW7606 can simultaneously sample all analog input channels. When two CONVST pins (CONVSTA good CONVSTB) are connected together, all channels are sampled synchronously. Two CONVST x inputs can be controlled using one CONVST signal. The rising edge of this common CONVST signal initiates synchronous sampling of all analog input channels.

The CW7606 has a built-in on-chip oscillator for conversion. Conversion time tCONV for all ADC channels. The BUSY signal informs the user that a transition is taking place, so when the CONVST rising edge is applied, BUSY goes to a logical high level and goes to a low level at the end of the entire transition process. The BUSY signal drop is used to return all eight sample and hold amplifiers to track mode. The BUSY falling edge also indicates that new data can now be read from the parallel bus DB [15: 0], DOUTA/DOUTB serial data lines.

After the RESET signal becomes low, it needs to be delayed for at least 1ms before the CONVST signal can be sent. See t7 in the timing diagram for details.

Synchronous sampling of two sets of channels

The CW7606 also allows simultaneous sampling of analog input channels in two sets. The two CONVST pins are activated independently by pulses, and this sampling method can only be achieved when oversampling is not used. CONVSTA is used to initiate synchronous sampling for the first set of channels (V1 to V4), and CONVSTB is used to initiate synchronous sampling for the second set of channels (V5 to V8), as shown in Figure 12 below.

At the rising edge of CONVSTA, the sample and hold amplifiers of the first set of channels enter hold mode. At the rising edge of CONVSTB, the sample and hold amplifiers of the second group enter the hold mode. The conversion process begins when both CONVST x have reached the rising edge, so BUSY goes high at the rising edge of the latter CONVST x signal. When two independent CONVST x signals are used, the data reading process is unchanged. Connect all unused analog input channels to the AGND. The results of not using channels are still included in the data read, because all channels are always converted.

10.6 Interface Part

The CW7606 offers three interface options: parallel interface, high-speed serial interface, and parallel byte interface. The required interface mode can be selected via the PAR/SER/BYTE SEL and DB15/BYTE SEL pins.

Table 4. Interface mode selection

PAR/SER/BYTE SEL	DB15	Interface Mode
0	0	Parallel interface mode
1	0	Serial interface mode
1	1	Parallel byte interface mode

Parallel interface (PAR/SER/BYTE SEL = 0)

Data can be read from the CW7606 via a parallel data bus with standard CS and RD signals. When reading data through the parallel bus, you need to connect the PAR/SER/BYTE SEL pin to the low level. Through the CS and RD input signals, the conversion result can be output to the data bus. When CS and RD are at the logic low level at the same time, the data lines DB 15 to DB 0 are no longer in the high impedance state. The rising edge of the CS input signal makes the bus enter three states, and its falling edge makes the bus out of the high impedance state. CS is the control signal that enables the data line. Using this function, multiple ADC devices can share the same parallel data bus. The CS signal can be permanently connected to the low level, while the RD signal can be used to obtain the conversion result, as shown in Figure 13. After the BUSY signal goes low, new data can be read (see Figure 13);

Alternatively, when BUSY is high, the data from the previous conversion can be read (see Figure 14). The RD pin is used to read data from the output conversion result register. Applying an RD pulse sequence to the ADC chip pins can cause the conversion results of each channel to be output to the parallel bus DB one by one in ascending order [15: 0]. After BUSY becomes low, the first RD falling edge outputs the conversion result of channel V1, and the next RD falling edge updates the bus with the V2 conversion result, and so on. On CW7606, the eighth falling edge of RD outputs the conversion result of channel V8. When the RD signal is logic low, the data conversion results of each channel can be transmitted to the digital host (DSP, FPGA).

When there is only one ADC chip on the system board and it does not share a parallel bus, only one control signal of the digital host can be used to read data. The CS and RD signals may be connected together, as shown in FIG. 16. In this case, the data bus goes out of tri-state at the falling edge of the CS/RD. Using the CS and RD combined signals, data can be output from the CW7606 and read by the digital master. In this case, the CS is used to enable data frame transmission for each data channel.

Parallel byte (PAR/SER/BYTE SEL = 1, DB15 = 1)

The working principle of parallel byte interface mode is very similar to that of parallel interface mode, except that the conversion result of each channel is read out in two 8-bit transmissions. Therefore, it takes 16 RD pulses to read the conversion results of all eight channels of the CW7606, as shown in Figure 17. When the CW7606 is configured in parallel byte mode, the PAR/SER/BYTE SEL and DB15/BYTE SEL pins should be connected to logic high (see Table 4). In parallel byte mode, DB [7: 0] is used to transmit data to the digital host. DB0 is the LSB for data transmission, and DB7 is the MSB for data transmission. The DB14 acts as the HBEN pin. When DB14/HBEN is connected to the logic high level, the high byte of the conversion result is output first, and then the low byte is output; When the DB14/HBEN is connected to a logic low level, the low byte is output first, and then the high byte is output. The FRSTDATA pin will remain high until the CW7606 reads the full 16-bit conversion result of V1.

Serial interface (PAR/SER/BYTE SEL = 1, DB15 = 0)

To read back data from the CW7606 via the serial interface, the PAR/SER/BYTE SEL pin must be connected to high and the DB15 to low. The CS and SCLK signals are used to transmit the data of the CW7606. The CW7606 has two serial data output pins: DOUTA and DOUTB. Data can be read back from the CW7606 via single or dual DOUT lines. The results of the conversion of channels V1 to V4 appear first on DOUTA and the results of the conversion of channels V5 to V8 appear first on DOUTB. The falling edge of CS enables the data output lines DOUTA and DOUTB to break out of the three states, and outputs the MSB of the conversion result one by one. The SCLK rising edge sends all subsequent data bits to the serial data outputs DOUTA and DOUTB one by one. The CS input can be kept low throughout the serial read operation, or it can be activated by pulse to enable 16 SCLK cycle frame reads for each channel. When the dual DOUT line is used to read eight synchronous conversion results on the CW7606, 64 SCLK transmissions are required to access the data of the CW7606, and the CS is kept low to enable all 64 SCLK periodic frames. You can also use only one DOUT line to output data one by one; In this case, it is recommended to access all transformed data with DOUTA, because the channel data is output in ascending order. For the CW7606, a total of 128 SCLK cycles are required when accessing all eight conversion results over a single DOUT line. These 128 SCLK periodic frames may be enabled by one CS signal, or 16 SCLK periodic frames of each group may be independently enabled by the CS signal. The disadvantage of using only one DOUT line is that if you read after conversion, the throughput rate will decrease. In serial mode, unused DOUT cables should remain disconnected. For CW7606, if DOUTB is used as a DOUT line, the channel results will be output in the order of V5, V6, V7, V8, V1, V2, V3, V4; However, after reading V5 on DOUTB, the FRSTDATA indication returns to low.

Figure 18 shows a timing diagram of reading a channel of data (frame transmission enabled by CS signal) from CW7606 in serial mode. The SCLK input signal provides a clock source for serial read operations. CS goes low to access data from CW7606. The CS falling edge takes the bus out of tri-state and outputs the MSB of the 16-bit conversion result one by one. This MSB is valid at the first SCLK falling edge after the CS falling edge. The subsequent 15 data bits are output one by one at the rising edge of the SCLK. The data is valid at the falling edge of SCLK. 16 clock cycles must be provided to the CW7606 to obtain the conversion result of one channel. The FRSTDATA output signal indicates when to read back the first channel V1. When the input is high, the FRSTDATA output pin is in tri-state. In serial mode, the CS falling edge takes FRSTDATA out of tri-state and sets the FRSTDATA pin to high, indicating that the DOUTA output data line can provide the result of V1. After the 16th SCLK falling edge, the FRSTDATA output resumes a logic low level. If all channels are read on DOUTB, the FRSTDATA output does not go high when V1 is output to this serial data output pin. It only goes high when DOUTA provides a V1 result (at which point DOUTB provides a V5 result).

Read during transition

When BUSY is high, the conversion is in progress, and data can also be read from the CW7606. This hardly affects the performance of the converter, and can achieve faster throughput. Parallel, parallel byte, or serial reads can be performed during conversion, with or without oversampling. Figure 14 shows the timing diagram of the read operation when BUSY is high in parallel or serial mode. Reads are performed during conversion so that the highest throughput can be achieved even when the serial interface is used and the VDRIVE is higher than 4.75 V.

Oversampling control

When the oversampling function is turned on, the magnification of oversampling is controlled by the oversampling pin OS [2: 0] (see Table 5). OS2 is the MSB control bit and OS0 is the LSB control bit. Table 5 provides the oversampled bit decoding used to select different oversampling magnifications. The OS pin is latched on the falling edge of BUSY to set the oversampling magnification for the next conversion (see Figure 19). When oversampling is turned on, the CONVST A and CONVST B pins need to be connected together to drive, and the time for BUSY to remain high during the conversion process will be extended. The actual time that BUSY stays high depends on the chosen oversampling magnification; The higher the oversampling rate, the BUSY stays high

The longer the flat time or total conversion time.

Timing diagram

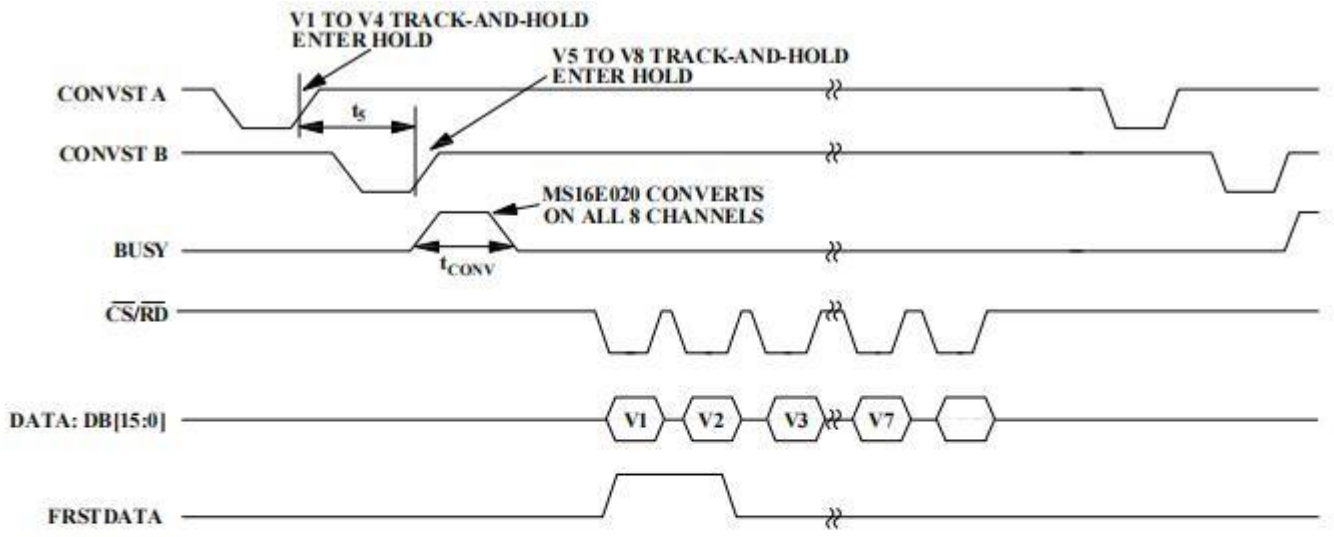

Figure12 Synchronous sampling is performed in two sets of channels, using independentCONVST A AndCONVST B time series-Parallel mode

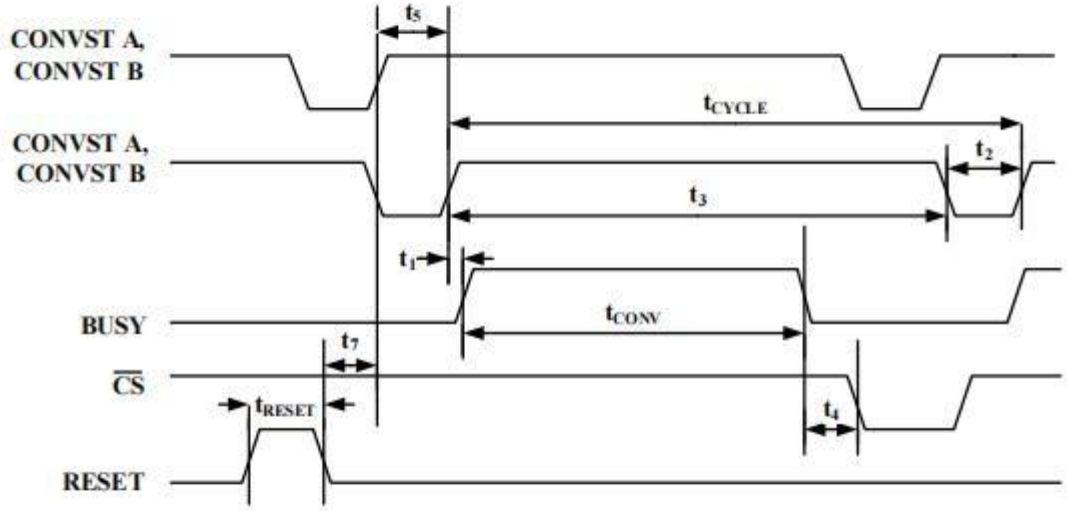

Figure13 CONVST Timing-Read after conversion

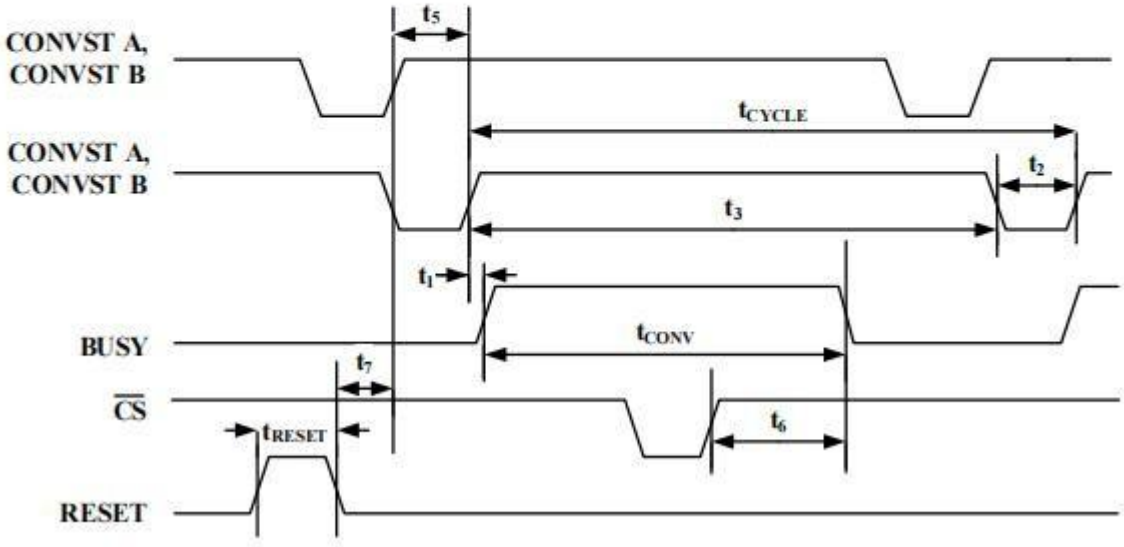

Figure14 CONVST Timing-Read during transition

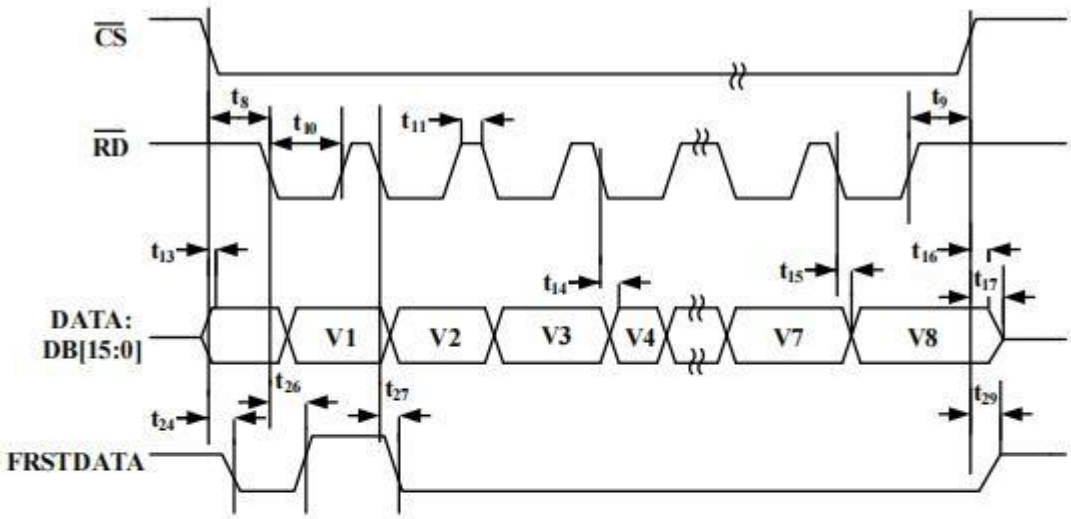

Figure15 Parallel mode, independentCSAndRDPulse

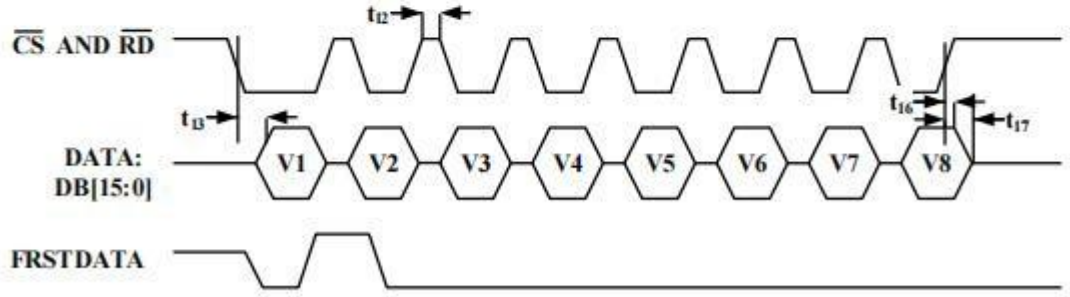

Figure16 CSAndRDConnected parallel mode

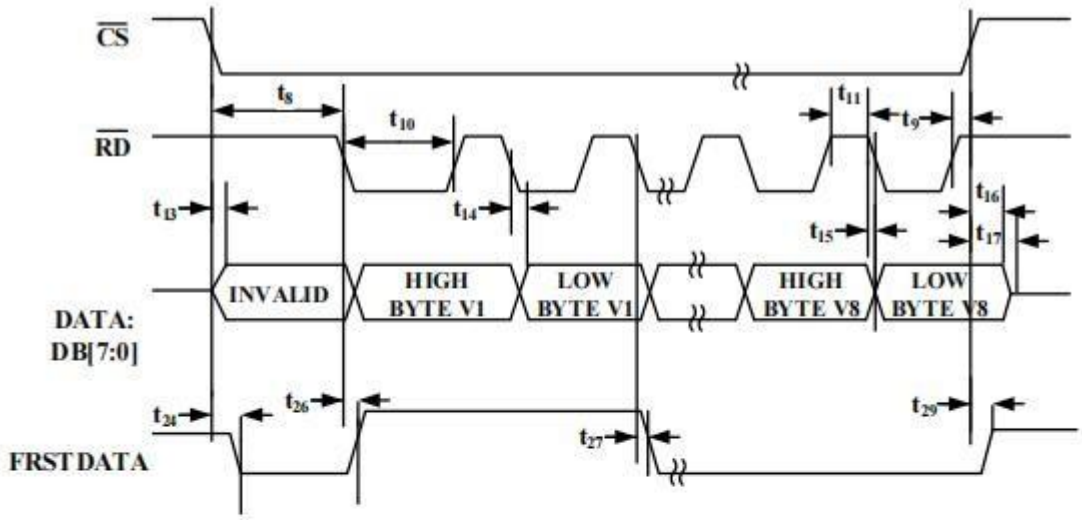

Figure17 Parallel byte mode

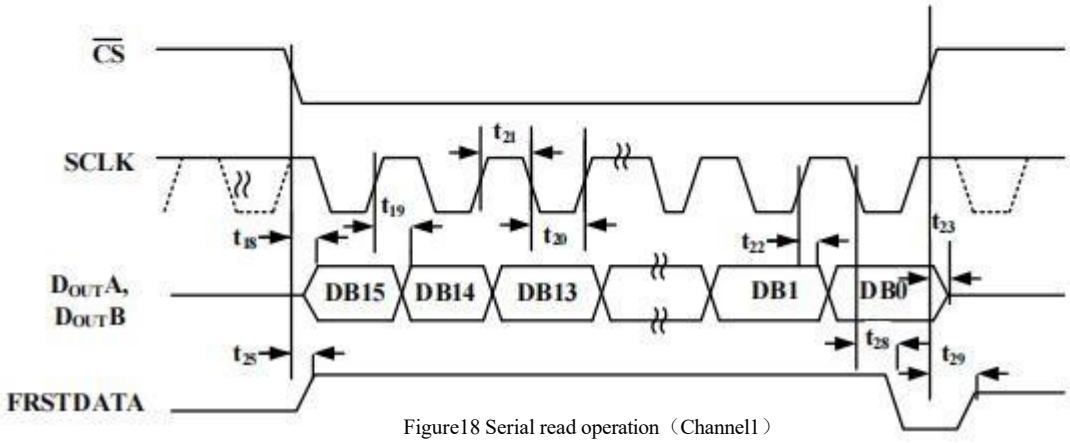

Figure18 Serial read operation（Channel1）

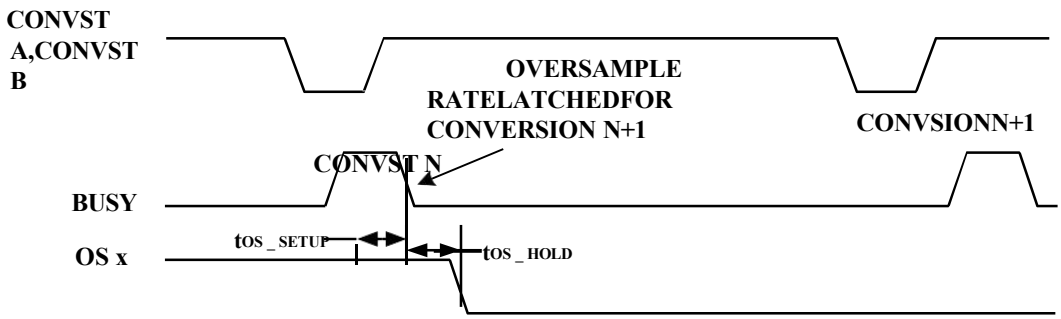

Figure19 OS x Pin timing

TABLE**5.**Oversampling bit decoding

OS [2: 0]	Oversampling magnification	5V scope SNR （dB）	10V Range SNR (dB)	5V range 3dB bandwidth (kHz)	10V range 3dB bandwidth (kHz)	Maximum throughput CONVST frequency (kHz)
0	NoOS	89.6	90.6	15	22	200
1	2	90.7	91.4	15	22	80
10	4	92.2	93	13.5	18.5	40
11	8	93.4	94.2	10	11.8	20
100	16	94.2	94.5	6	6	10
101	32	94.4	95.5	3	3	5
110	64	95.8	95.2	1.5	1.5	2.5
111（disable）						

11.0 Application instructions

11.1 Layout

The printed circuit board on which the CW7606 is located should be designed separately from the analog part and the digital part, and limited to different areas of the circuit board. At least one ground plane should be used. The digital and analog parts can share or split the ground plane. When using divided strata, digital and analog grounds should be connected at a single point. The single grounding point is preferably as close as possible to CW7606. If there are multiple devices in the CW7606 system that require analog-to-digital grounding, a single point grounding should still be adhered to, and the grounding point should be placed as close as possible to a star grounding point of the CW7606. Ensure that each ground pin has a good connection to the formation. Avoid situations where multiple ground pins share one connection to the formation. Each ground pin should use a single via or multiple vias to access the ground plane.

Avoid laying out digital wiring under the device, otherwise noise will be coupled to the chip. The analog ground plane should be allowed to be placed below CW7606 to avoid noise coupling. Fast switching signals such as CONVSTA, CONVSTB or clock should be digitally shielded to prevent noise from radiating to other parts of the circuit board, and the fast switching signal should never be close to the analog signal path. Overlap of digital signals with analog signals should be avoided. The traces on adjacent layers of the circuit board should be perpendicular to each other,

So as to reduce the feedthrough effect of the circuit board.

The power lines of AVCC and VDRIVE pins should be as wide as possible to provide a low impedance path and reduce glitch noise effects on the power lines. Where possible, the power layer should be used and a good connection between the power pins and the power traces of the board should be established; This includes that each power pin should be connected to the power trace and power layer using a single via or multiple vias.

Good decoupling is also important in order to reduce the power impedance of the CW7606 and reduce the power spike amplitude. Decoupling ceramic capacitors typically 100 nF should be connected to all power pins AVCC and VDRIVE. These decoupling capacitors should be placed close to (ideally close to) these pins and their corresponding ground pins. In addition, a low ESR 10μF capacitor should be placed on each power pin. Pin sharing these capacitors should be avoided. Large vias should be used to connect these capacitors to the power supply and ground planes. Wider, shorter traces should be used between vias and capacitor pads, or vias should be adjacent to capacitor pads to minimize parasitic inductance. For AVCC decoupling, recommended decoupling capacitors are 100 nF, low ESR, ceramic capacitors (Farnell 335-1816) and 10 μF, low ESR, tantalum capacitors (Farnell 197-130). A large decoupling tantalum capacitor should be placed where the AVCC power enters the board.

The decoupling capacitors of the REFIN/REFOUT pins and the REFCAPA, REFCAPB pins should be as close as possible to the corresponding pins. Where possible, these capacitors should be placed on the same side of the board as the CW7606 device.

12.0 Overall dimensions

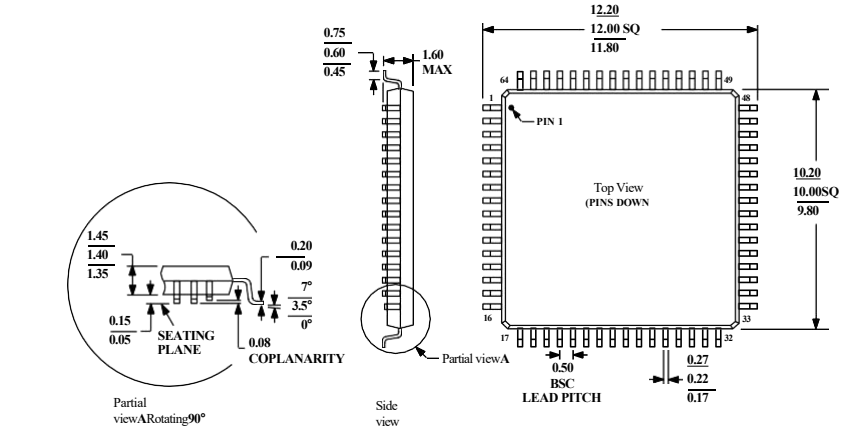

Figure20 64Pin thin square flat package[LQFP64]

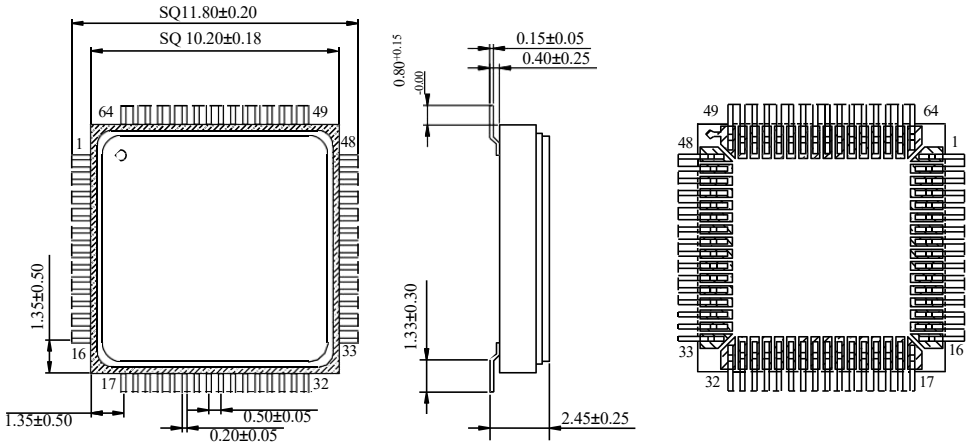

Figure21 64Pin thin square flat package[CQFP64]

13.0 Appendix

PCB Layout Packaging design reference, compatible with two packaging forms of chip: plastic packaging and ceramic packaging.

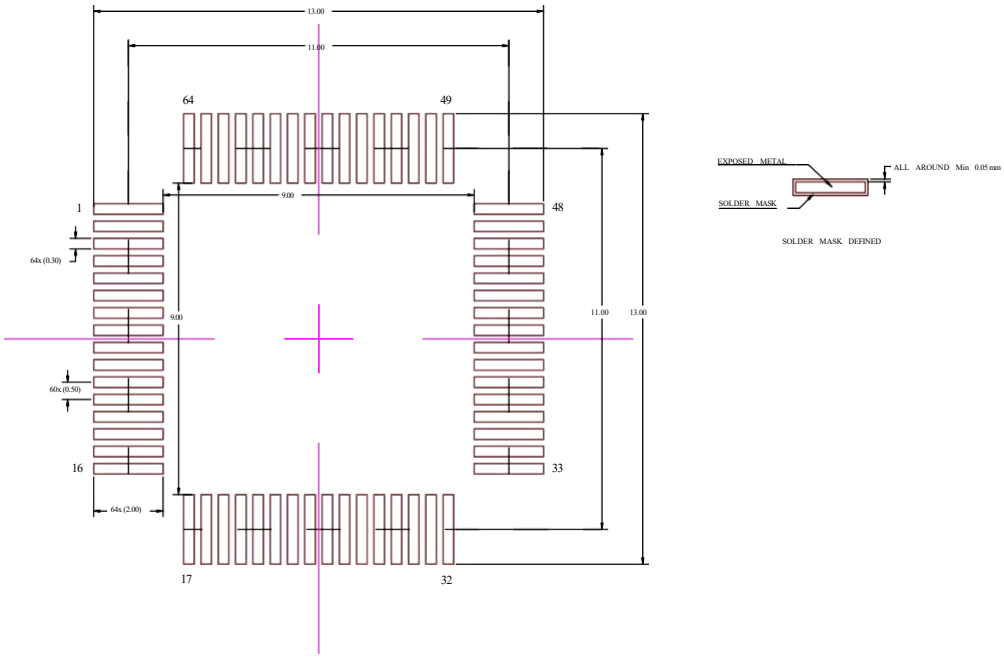

Figure22 PCB Layout Package Design Reference