CW9245 Data sheet

Single channel14 Bit20 MSPS\ 40 MSPS\ 65 MSPS\ 80 MSPS ADC

1.0 overview

The CW9245 is a monolithically integrated, single-supply, 14-bit analog-to-digital converter (ADC) that includes a high-performance sample-and-hold amplifier and voltage reference. It uses a differential multi-stage pipeline architecture with output error correction logic to provide 14-bit accuracy and ensure no code missing over the full temperature range. The wideband fully differential SHA allows for multiple selectable input ranges and wide input common mode, including single-ended applications. It is suitable for multiplexing systems that switch full-scale voltage levels in continuous channels, as well as sampling single-channel inputs at frequencies well above the Nyquist rate.

A single-ended clock input is used to control all internal conversion cycles, and a duty cycle stabilization circuit (DCS) is able to compensate for changes in clock duty cycle while maintaining excellent overall ADC performance. The digital output data is represented in an offset binary or binary complement format, and an over-the-range (OTR) signal indicates an input overflow condition, with the most significant bit to determine a low or high overflow.

CW9245 is manufactured using CMOS process and is in a 32-pin QFN package. The operating temperature range is:-55 ℃ ~ + 125 ℃.

3.0 peculiarity

- Single channel 20MSPS\ 40MSPS\ 65MSPS\ 80MSPS ADC
- Low power consumption: 210mW @ 80MSPS
- Input signal swing: 1Vpp-2Vpp
- Integrated on-chip voltage reference source and sample and hold circuit
- Offset binary or binary complement data format
- On-chip integrated clock duty cycle stabilization circuit
- Analog supply voltage AVDD: 3.3 V @ type
- Flexible energy-saving power-down mode
- Compatible with AD9245

4.0 Performance Metrics

- Differential analog input bandwidth: 500MHz
- Static performance : DNL-0.5/+0.5 LSB, INL-2.0/+2.0 LSB
- Dynamic performance (fs = 80MSPS)

-fin = 5MHz

ENOB = 11.3 Bit, SNDR = 70.0 dB, SNR = 71.0 dB

-fin = 70 MHz

ENOB = 11.1 Bit, SNDR = 69.0 dB, SNR = 69.5 dB

-fin = 100 MHz

ENOB = 10.7 Bit, SNDR = 66.5 dB, SNR = 67.0 dB

2.0 Application

- Medical imaging equipment
- Communication transceiver
- Battery-powered equipment
- Handheld oscilloscope, spectrum analyzer

4.0 Performance Metrics

- Differential Analog Input Bandwidth: 500 MHz
- Static Performance: DNL -0.5/+0.5 LSB, INL -2.0/+2.0 LSB
- Dynamic Performance (fs = 80 MSPS)
  - fin = 5 MHz ENOB = 11.3 Bit, SNDR = 70.0 dB, SNR = 71.0 dB
  - fin = 70 MHz ENOB = 11.1 Bit, SNDR = 69.0 dB, SNR = 69.5 dB
  - fin = 100 MHz ENOB = 10.7 Bit, SNDR = 66.5 dB, SNR = 67.0 dB

Chengdu Cuiwei Electronic Co.,LTD
Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

5.0 Simplified block diagram

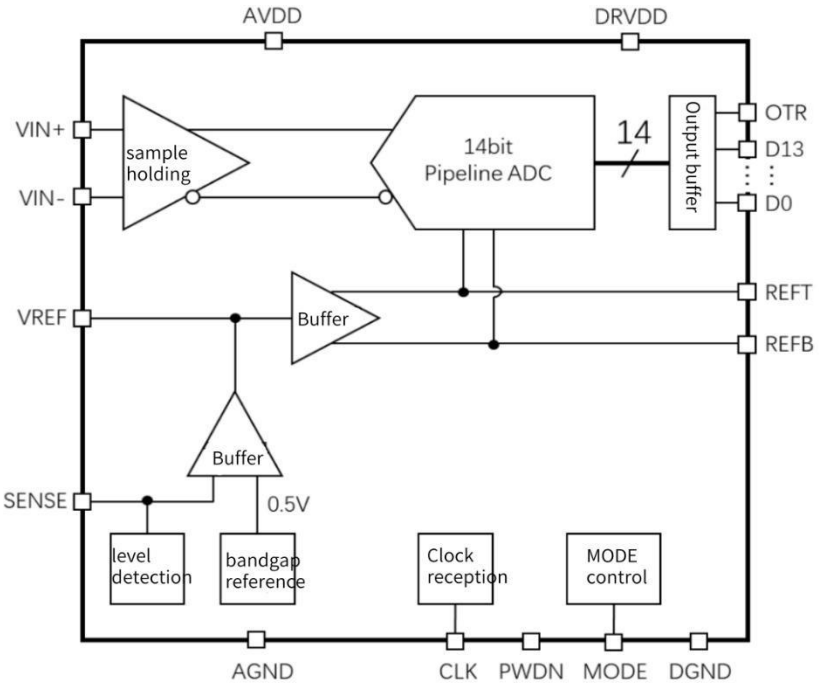

Figure5.1 CW9245 System block diagram

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E-mail:sales@cdcwtec.com
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6.0 Typical performance

TABLE**6-1** Conditions of use of chips

parameter	Symbols	annotation	Numerical value	Units
Power supply voltage	AVDD	Analog power supply	3.3	V
	DRVDD	Digital power supply	2.5	V
Power-on sequence		No power-on sequence requirement		
Ground	AVSS	Analogically	0	V
	DRVSS	Digitally	0	V
Differential input analog signal amplitude	V_{IN+}-V_{IN-}	Differential amplitude of input signal	2.0	Vpp
Logic input high	V_{IH}		V_{DR}	V
Logic input low	V_{IL}		GND	
Clock frequency	f_{MCLK}		$f_{MCLK} \leq 80$	MHz
Operating temperature range	T_A		$-55 \leq T_A \leq 125$	℃

TABLE**6-2** Electrical characteristics of power supply, inputs and outputs

parameter	Symbols	Minimum	Typical value	Maximum	Units
Resolution			14		Bit
Power supply voltage					
Analog power supply	AVDD	3	3.3	3.6	V
Digital power supply	DRVDD	2.2	2.5	1.95	V
Supply current					
Analog power supply	I_{AVDD}		58		mA
Digital power supply	I_{DR}		6		mA
Power consumption	P_D				
Low frequency input power consumption			210	230	mW
Standby Mode power consumption			1		mW
Data Entry					
Input differential analog signal amplitude	V_{IN+}– V_{IN-}		2.0		Vpp
Logic level					
High input voltage	V_{IH}	2.0			V
Low level input voltage	V_{IL}			0.8	V
High input current	I_{IH}	-10		+10	uA
Low level input current	I_{IL}	-10		+10	uA

TABLE**6-3** Static characteristics

parameter	Symbols	Minimum	Typical value	Maximum	Units
Differential nonlinearity	DNL	-1.0	±0.5	+1.0	LSB
Integral nonlinearity	INL	-5.15	±2	+5.15	LSB

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Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
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TABLE**6-4** Dynamic performance

parameter	Symbols	Temperature	Minimum	Typical value	Maximum	Units
AVDD = 3.3 V，DRVDD = 3.3 V,f_s =80MSPS，2Vpp Differential input,**1.0 V**Internal benchmark						
Significant digits（ENOB）	ENOB					
f_{in} = 5 MHz		25 °C		11.3		bit
f_{in} = 70MHz		25 °C		11.1		bit
f_{in} = 110 MHz		25 °C		10.7		bit
Signal-to-noise ratio（SNR）	SNR					
f_{in} = 5 MHz		25 °C	69	71		dB
f_{in} = 70MHz		25 °C	68	69.5		dB
f_{in} = 110 MHz		25 °C		67		dB
Signal ratio（SNDR）	SNDR					
f_{in} = 5 MHz		25 °C	68	70		dB
f_{in} = 70MHz		25 °C	67	69		dB
f_{in} = 110 MHz		25 °C		66.5		dB
Spur-free dynamic range（SFDR）	SFDR					
f_{in} = 5 MHz		25 °C		-85		dBc
f_{in} = 70MHz		25 °C		-82		dBc
f_{in} = 110 MHz		25 °C		-72		dBc

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E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

7.0 Pin configuration and function description

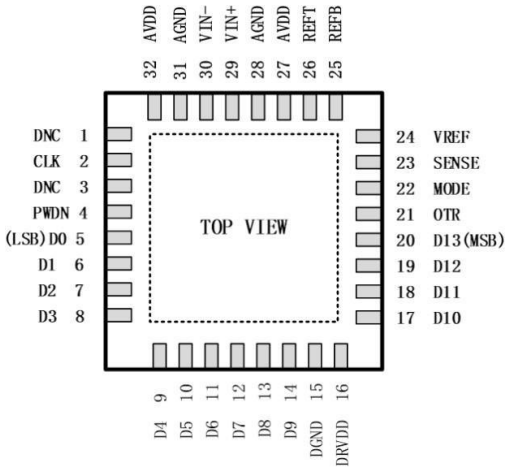

Figure7.1 CW9245 Pin arrangement（Top View）

Balloon serial number	Symbols	Gong can
1	DNC	Suspended foot
2	CLK	Clock input
3	DNC	Suspended foot
4	PWDN	Power-down Function selection
5	D0	Data outputD0
6	D1	Data outputD1
7	D2	Data outputD2
8	D3	Data outputD3
9	D4	Data outputD4
10	D5	Data outputD5
11	D6	Data outputD6
12	D7	Data outputD7
13	D8	Data outputD8
14	D9	Data outputD9
15	DGND	Data output place
16	DRVDD	Data-driven power supply
17	D10	Data outputD10
18	D11	Data outputD11
19	D12	Data outputD12
10	D13	Data outputD13
21	OTR	Out-of-range indication output
22	MODE	Mode suspension control
23	SENSE	Reference voltage control
24	VREF	Reference voltage input/Output
25	REFB	Negative differential reference voltage
26	REFT	Positive differential reference voltage
27	AVDD	Analog power supply
28	AGND	Analogically
29	VIN +	Positive analog input
30	VIN-	Negative analog input
31	AGND	Analogically
32	AVDD	Analog power supply
EPAD	AGND	Analog power supply common ground

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Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

8.0 Typical performance test curve

Test conditions: Unless otherwise specified,AVDD = 3.3 V，DRVDD = 3.3 V,fs=80MSPS，2Vpp Differential input,1.0 V Internal benchmarks,T_A= 25 ° C。

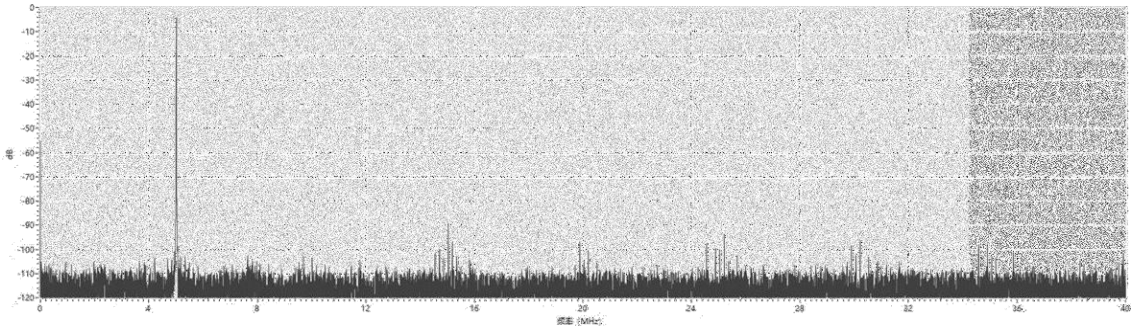

Figure8.1 Single frequency pointFFT（32 k）@ 5.01 MHz

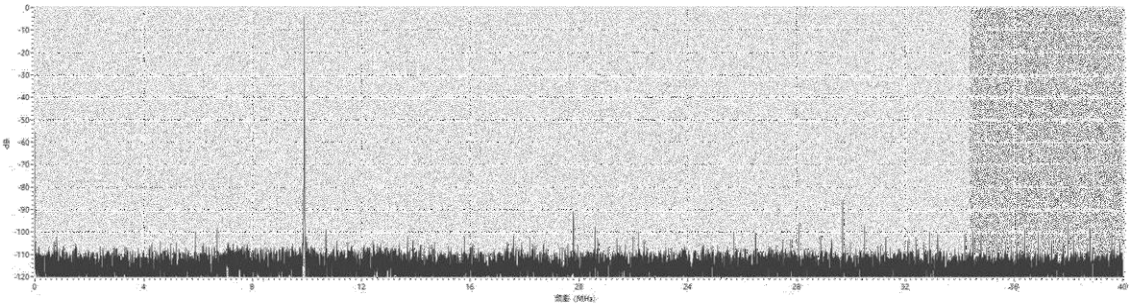

Figure8.2 Single frequency pointFFT（32 k）@ 70MHz

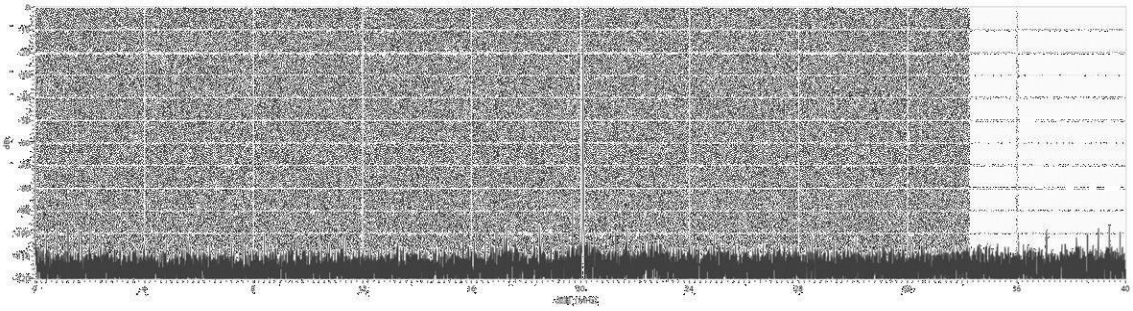

Figure8.3 Single frequency pointFFT（32 k）@ 100MHz

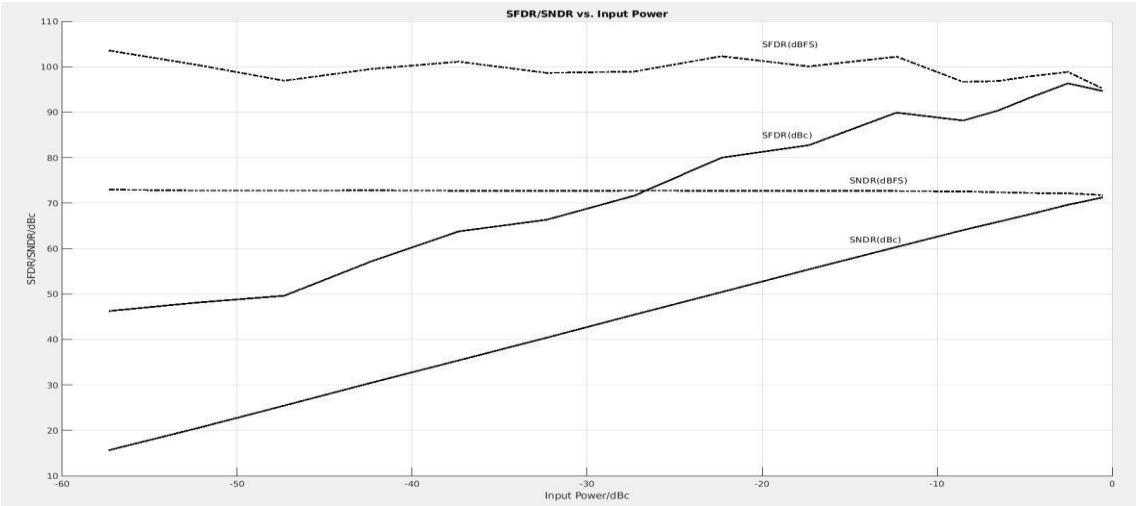

Figure8.4SNR + SFDR VS Input amplitude

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E-mail:sales@cdcwtec.com
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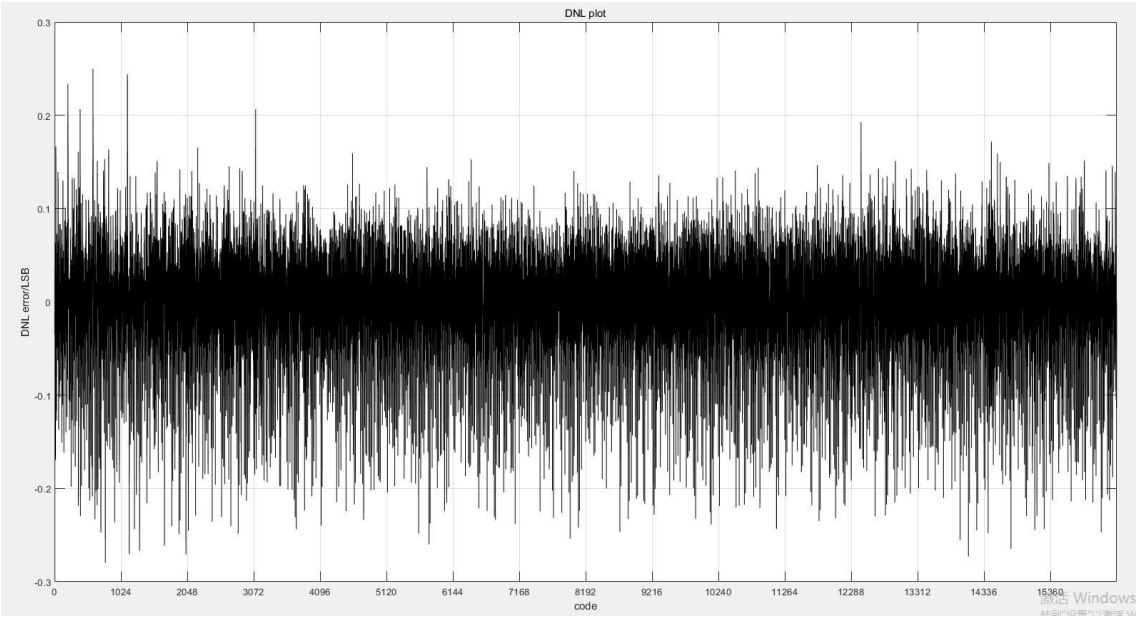

Figure8.5 typicalDNL Curve

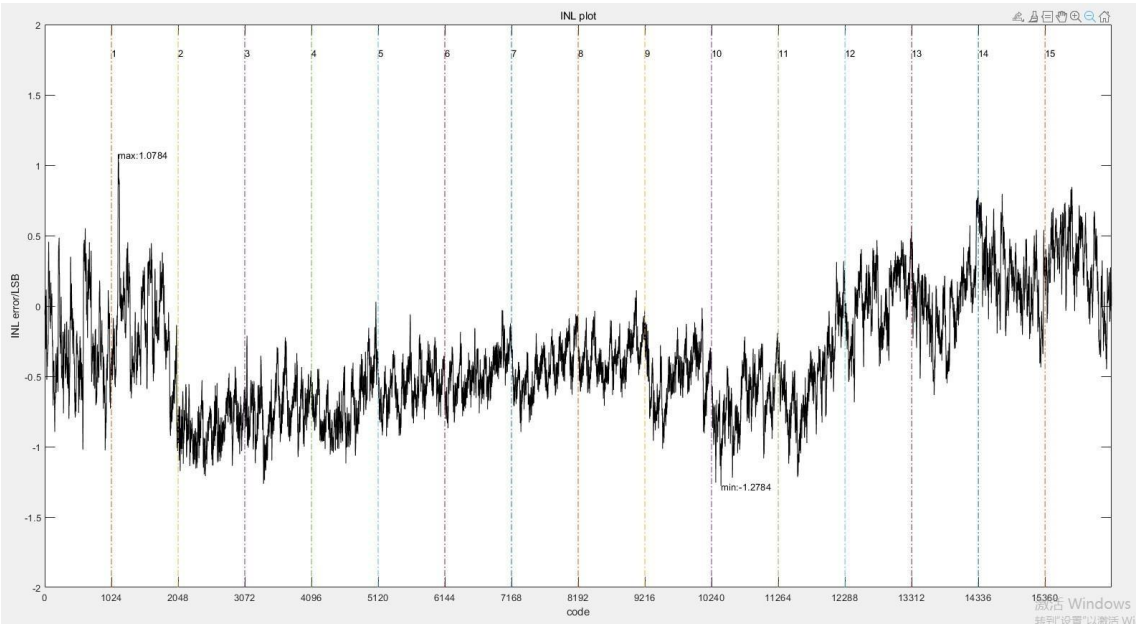

Figure8.6 typicalINLCurve

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E-mail:sales@cdcwtec.com
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9.0 Timing diagram

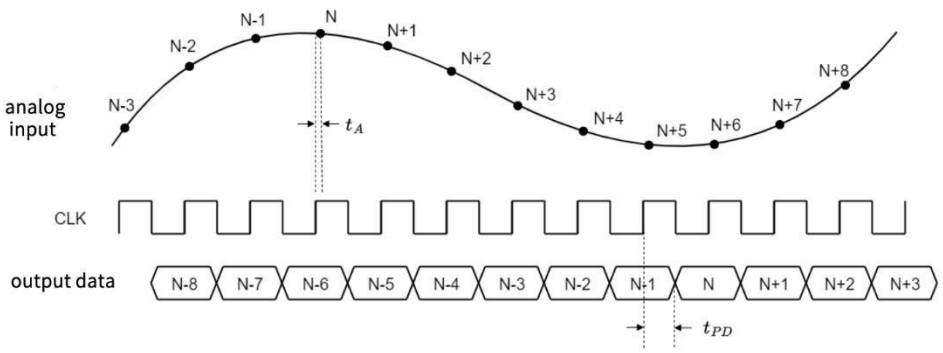
9.1 Data timing

Unless otherwise specified, AVDD = 3.3 V, DRVDD = 3.3 V, maximum sampling rate, 2 Vpp differential input, 1.0 V internal reference.

Table 9.1 Switch parameters

parameter	Temperature	Minimum	Typical value	Maximum	Units
Clock input parameters					
Maximum clock rate	Full	80			MHz
Data output parameters					
Minimum conversion rate	Full			1	MHz
Clock cycle	Full		12.5		ns
CLK High pulse width	Full	4.6			ns
CLK Low pulse width	Full	4.6			ns
Data transmission delay(t_{PD})	Full		4.2		ns
Pipeline delayLatency	Full		6		cycle
Aperture delay(t_A)	Full		1.0		ns
Aperture jitter(t_j)	Full		0.4		ns
Wakeup time	Full		7		ms
Out-of-range recovery time	Full		3		cycle

9.2 Timing diagram



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Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

1. canonical application circuit

2. Principle of Operation

The CW9245 analog inputs are sample-and-hold amplifiers (SHAs) followed by a 5-stage differential structure pipelined ADC with sufficient overlap between each stage. In order to correct the flash error of each stage, the quantized output of each stage is combined into a 14bit digital signal by digital correction logic. The pipelined architecture passes the residual signal to the next stage, allowing the first stage to process the new input samples while the following pipelined stages process the residual signal from the previous stage.

Except for the last stage, each stage of the pipeline contains a low-resolution flash ADC connected to a switched-capacitor DAC and an inter-stage residual amplifier, the DAC and amplifier form the MDAC. the residual amplifier amplifies the difference between the input and the output of the DAC as a flash input to the next stage, and a 1bit redundancy is used to digitally correct the flash error of each stage. The last stage contains only one flash ADC. The input stage contains a differential SHA that can be ac/dc coupled in differential or single-ended mode. The output segments align and correct the data and pass the corrected data to the output buffer. The output buffer is powered from a separate supply, allowing the output voltage swing to be adjusted.

2. Analog Input Configuration

The analog input to the CW9245 is a differential switched-capacitor SHA for optimal performance when processing differential input signals.The SHA input supports a wide common mode range (VCM) and maintains excellent performance, as shown in Figure 10.1. The input common-mode voltage is set to 0.5*AVDD, which minimizes signal-related errors and provides the best performance.

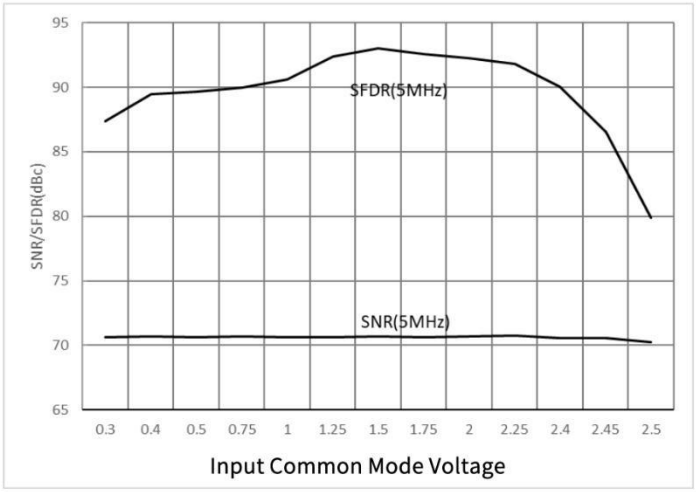

Figure10.1 SNR/SFDR VS Common mode voltage

Figure 10.2 shows the clock signal alternately switching the SHA between sample mode and hold mode.When the SHA switches to sample mode, the source must have enough drive to charge the sample capacitor and stabilize it for half a clock cycle. A small resistor in series with each input can help reduce the peak transient current required to drive the source output stage. In addition, a small capacitor can be placed in parallel at the inputs to provide dynamic charging current. This passive network creates a filter with low-pass characteristics at the input of the ADC; therefore, the exact value depends on the application. In IF undersampling applications, any shunt capacitors should be reduced or removed; they limit the input signal bandwidth.

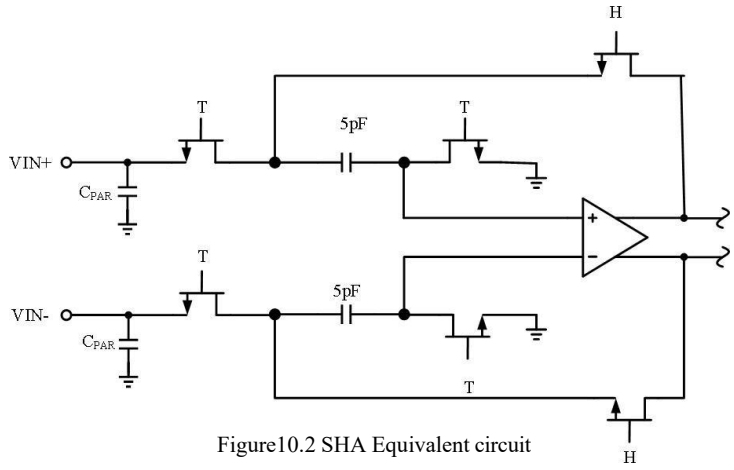

Figure10.2 SHA Equivalent circuit

For best dynamic performance, the source impedances driving VIN+ and VIN- should be matched so that the common-mode build-up errors are symmetrical. These errors are reduced by the ADC's common-mode rejection. The internal differential reference buffer generates positive and negative reference voltages, REFT and REFB, which define the quantization range of the ADC. Set the reference buffer output common-mode to 0.5*AVDD and define the REFT and REFB voltages and ranges as:

Chengdu Cuiwei Electronic Co.,LTD
Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

For best dynamic performance, the source impedances driving VIN+ and VIN- should be matched so that the common-mode build-up errors are symmetrical. These errors are reduced by the ADC's common-mode rejection. The internal differential reference buffer generates positive and negative reference voltages, REFT and REFB, which define the quantization range of the ADC. Set the reference buffer output common-mode to 0.5*AVDD and define the REFT and REFB voltages and ranges as:

= ½(+)

= ½(-)

= 2(-) = 2 ×

From the above equation, the REFT and REFB voltages are symmetrical with 0.5*AVDD, and by definition, the input range is twice the value of the VREF voltage. The internal reference voltage can be pin-controlled and set to a fixed value on 0.5 V or 1.0 V, or it can be adjusted depending on the application, refer to the discussion in the Internal Voltage Configuration section. Maximum signal-to-noise performance is achieved when the CW9245 is set to the maximum 2Vpp input amplitude. The relative signal-to-noise ratio degradation from 2Vpp mode to 1Vpp mode is 3dB.

SHA can be driven by a signal source that keeps the signal peaks within the allowable range of the selected reference voltage. The minimum and maximum common mode input levels are defined as:

= /2

VC = (+)/2

While differential inputs allow for optimal performance, the CW9245 can also accept single-ended input signals connected to VIN+ or VIN-. In this configuration, one input receives the signal while the other input is connected to a suitable reference. For example, a 2Vpp signal can be applied to VIN+ and VIN- connected to a 1V reference. The CW9245 then accepts an input signal between 2V and 0V. The single-ended configuration results in significantly lower distortion performance compared to the differential case. However, the effect is less pronounced at lower input frequencies.

10.3 Differential Input Mode

Differential Input Configuration As mentioned earlier, the best performance is achieved when driving the CW9245 in a differential input configuration. For baseband applications, the AD8351 differential driver provides excellent performance and a flexible ADC interface.The output common-mode voltage of the AD8351 can easily be set to AVDD/2, and the driver can be configured in a Sallen-Key filter topology to provide bandwidth limiting of the input signal, as shown in Figure 10.3.

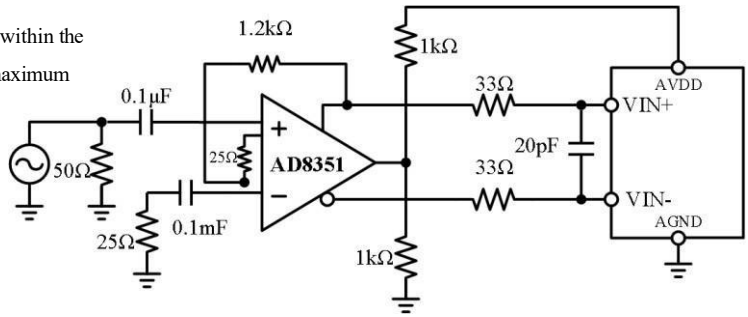

Figure10.3 Driving an application circuit using an amplifier

At input frequencies in the second Nyquist interval and above, most amplifiers do not have sufficient performance to meet the CW9245 performance requirements. This is especially true in IF undersampling applications with input frequencies from 70 MHz to 100 MHz, for which differential transformer coupling is recommended. The size of the shunt capacitance depends on the input frequency and the impedance of the signal source, and the capacitance value should be kept as small as possible or removed completely, as shown in Figure 10.4.

Signal characteristics must be considered when selecting a transformer; most RF transformers saturate at frequencies below a few MHz, and too much signal power can cause the core to saturate, leading to distortion.

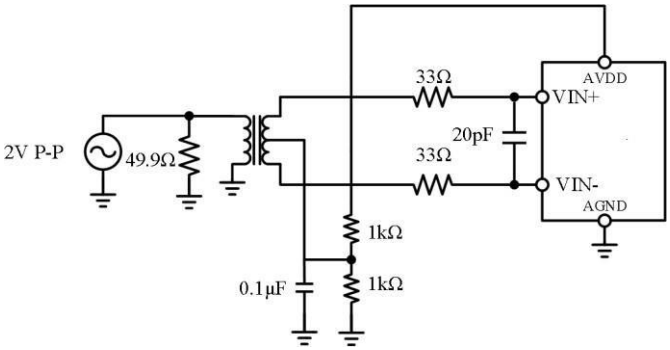

Figure10.4 Use balun drive application circuits

10.4 SINGLE-ENDED INPUT MODE

Single-ended inputs can provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance can be degraded due to the large input common mode swing. However, if the source impedance at each input is matched, the impact on signal-to-noise performance should be minimal. Figure 10.5 illustrates a typical single-ended input application circuit.

Chengdu Cuiwei Electronic Co.,LTD
Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

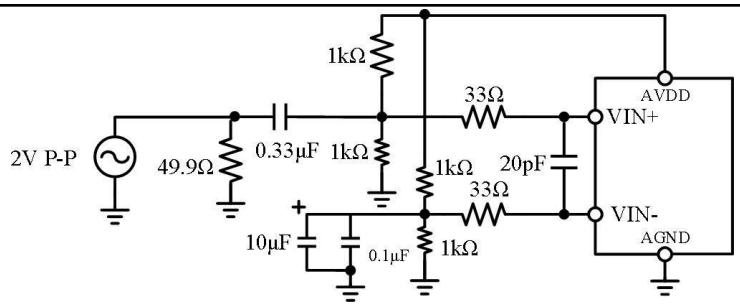

Figure10.5 Single-ended input drive application circuit

10.5 Clock input

Typical high speedADC Use clock rising and falling edges to generate various internal clock signals,Therefore sensitive to clock duty cycle. Usually when the clock duty cycle requiresWant to5%Tolerances to maintain dynamic performance characteristics.CW9245 Contains a clockDuty cycle stabilization circuit(DCS), the non-sampled edge can be readjusted to provideThe duty cycle is50%The internal clock signal of. Allows wide range of clock input dutiesThan, without affectingCW9245 The performance of. InDCS When on, the noise andDistortion performance in30%To70%It is almost flat under the duty cycle. Duty cycle stabilizer enablesLocked loop with delay(DLL)To reconstruct the unsampled edge. Therefore, the sampling frequencyAny changes, require approximately100 Clock cycles,DLL Acquire and lock to the new rate.

10.6JITTER Consider

High speed, high resolutionADC Very sensitive to the quality of the input clock.

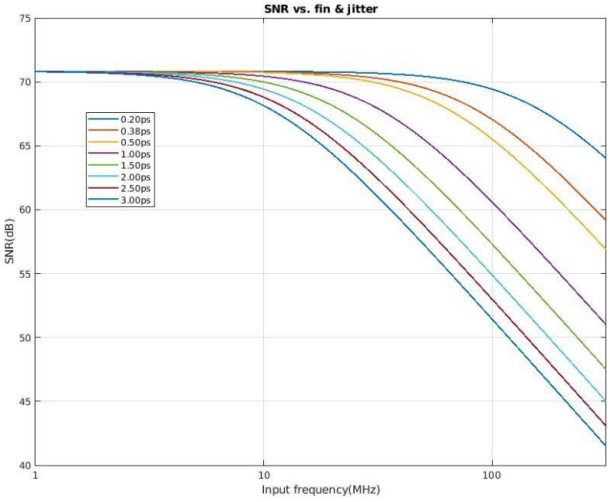

Figure10.6 SNR VS Input frequency/shake

Including clock input, analog input signal andADC Aperture jitter. IF undersampling

Applications are particularly sensitive to jitter(As shown in figure10.6 Shown in)。 Jitter at the aperture will affect CW9245 In the case of dynamic range, the input clock should be treated as an analog signal.The clock driven power supply should be the same asADC The output drive power supply is separated to avoid usingDigital noise modulated clock signal. Low-jitter, crystal-controlled oscillators are best

At a given input frequency (fINPUT), the decrease in the signal-to-noise ratio due to aperture jitter (tj) only can be calculated using the following equation

= -20 10[2 ×]

where the orifice diameter represents the root mean square of all jitter sources, including clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (as shown in Figure 10.6). In cases where aperture jitter affects the dynamic range of the CW9245, the input clock should be treated as an analog signal. The power supply for the clock driver should be separate from the ADC output driver power supply to avoid modulating the clock signal with digital noise. A low-jitter, crystal-controlled oscillator is the best clock source. If the clock is generated from another type of source (by gating, frequency division, or other means), it should be retimed at the end by the original clock.

10.7 Power Consumption and Standby Mode

The CW9245's digital power supply power consumption is proportional to its sampling rate, and the digital power consumption is primarily determined by the strength of the digital driver and the load on each output bit. The maximum DRVDD current ( ) can be calculated as:

= × × × where N is the number of output bits and the CW9245 is 14-bit . The maximum current is generated when each output switches on each clock cycle, i.e., a full-scale square wave with Nyquist frequency /2 . In practice, the DRVDD current is determined by the average number of output switches. Reducing the capacitive load on the output drivers minimizes digital power consumption. By pulling the PWDN pin high, the CW9245 is placed in standby mode. In this state, the ADC typically consumes 1 mW if the CLK and analog inputs are static. the output drivers are in a highly resistive state during standby. Pulling the PWDN pin low again restores the CW9245 to normal operating mode. Low power consumption in standby mode is achieved by turning off the bandgap reference, reference buffer, and bias network.

Decoupling capacitors on REFT and REFB are discharged when entering standby mode and then must be recharged when normal operation is resumed. Therefore, the wake-up time is related to the duration of the standby mode; the shorter the standby period, the shorter the wake-up time. With the recommended 0.1uF and 10uF decoupling capacitors on the REFT and EFB, it takes approximately 1 second for the reference buffer decoupling capacitor to fully discharge and 7 milliseconds to return to full operation.

Chengdu Cuiwei Electronic Co.,LTD
Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

8. Digital output

The CW9245 output driver can be configured with 2.5 V or 3.3 V logic by matching the DRVDD to the digital power supply of the interface logic. The output driver is sized to provide sufficient output current to drive various logic levels. However, large drive currents tend to lead to short-term pulse interference on the power supply, which may affect the performance of the converter. Applications that require an ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

9. Timing

The CW9245 provides latched data output with a pipeline delay of 6 clock cycles. The data output is available at a propagation delay (tPD) after the rising edge of the clock signal. For a detailed timing diagram, see Figure 9.1. The length and load of the output data line should be minimized to reduce transients of the CW9245 power supply. These transients can degrade the dynamic performance of the converter. The lowest typical conversion rate for the CW9245 is 1MSPS. Dynamic performance degrades at clock rates below 1MSPS.

10. Reference Voltage Configuration

The CW9245 has a stable, accurate 0.5 V reference built into it. The CW9245 input range can be adjusted by changing the reference voltage applied inside or outside the CW9245. The input range of the ADC has a linear relationship with the reference voltage. Various reference modes are described in Table 10.1 and described later. If the ADC is differentially driven through a transformer, the reference voltage can also be used to bias the center tap.

11. Internal Reference

The comparator in the CW9245 detects the potential of the SENSE pin and configures the reference to one of four possible states, as shown in Table 10.1. If SENSE is grounded, the reference amplifier switch is connected to the internal resistive divider (as shown in Figure 10.7), setting VREF to 1V. Connect the SENSE pin to the VREF and the reference amplifier output to the SENSE pin to form a loop and provide a 0.5 V reference output. If a resistive divider is connected as shown in Figure 10.8, the switch is set to the SENSE pin again. This puts the reference amplifier into non-inverting mode with a VREF output voltage of:

$= 0.5 \times (1 + 2/1)$

In all reference configurations, REFT and REFB drive the A/D conversion core and establish its input range. Whether it is an internal reference or an external reference, the input range of the ADC is always equal to twice the reference pin voltage. If the internal reference of the CW9245 is used to drive multiple converters to improve gain matching, the load of other converters on the reference must be considered, with a maximum load of 2mA recommended.

Table 10.1 VREF Voltage Selection

mode	SENSE Voltage	VREF Output voltage	Analog input range
External reference mode	AVDD	N/A	2 × VREF
Internal reference mode	VREF	0.5 V	1.0 V
Programmable mode	0.2 V ToVREF	0.5 × (1 + R2/R1)	2 × VREF
Internal reference mode	AGND To0.2 V	1.0 V	2.0 V

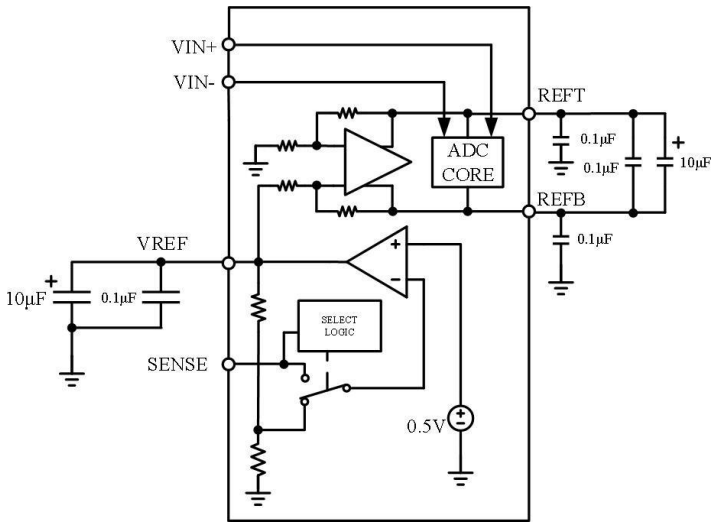

Figure10.7 Internal reference connection mode

Chengdu Cuiwei Electronic Co.,LTD
Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

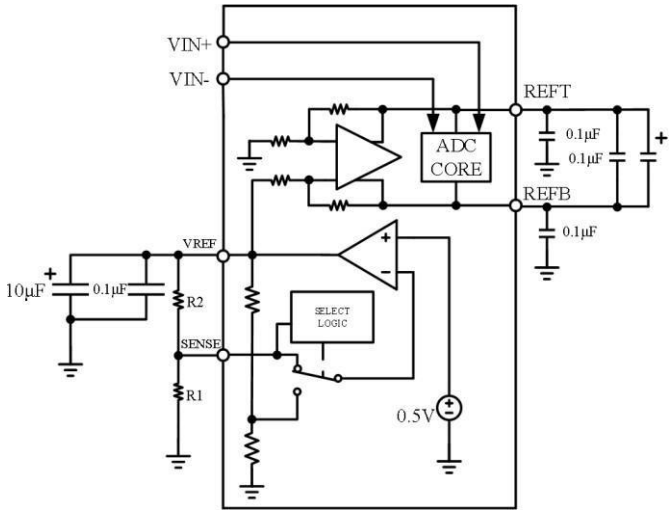

Figure10.8 Programmable mode connection mode

12. External Reference

In order to improve the gain accuracy of the ADC or to improve the thermal drift characteristics, an external reference may be used. When multiple ADCs are tracking each other, a single reference may be required to reduce the gain matching error to an acceptable level. When the SENSE pin is connected to the AVDD, the internal reference is turned off and the external reference is used. The internal reference buffer loads the external reference with an equivalent 7KΩ. The internal buffer still generates positive and negative full-scale reference voltages REFT and REFB for the ADC core. The input range is always twice the reference voltage value, so the external reference voltage must be limited to a maximum of 1.0 V.

13. Operating Mode Selection

As previously mentioned, the CW9245 may output offset binary or complement format data. Pins are also provided to enable or disable the clock DCS. The MODE pin is a multi-level input that controls the data format and DCS status. The input thresholds and corresponding mode selections are shown in Table 10.2

TABLE10.2 MODE Control Mode

MODE Voltage	Data format	Duty cycle correction(DCS)
AVDD	Binary complement	DCSclose
2/3 AVDD	Binary complement	DCSopen
1/3 AVDD	Offset binary	DCSopen
AGND	Offset binary	DCSclose

Chengdu Cuiwei Electronic Co.,LTD
Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com

11.0 Encapsulation information

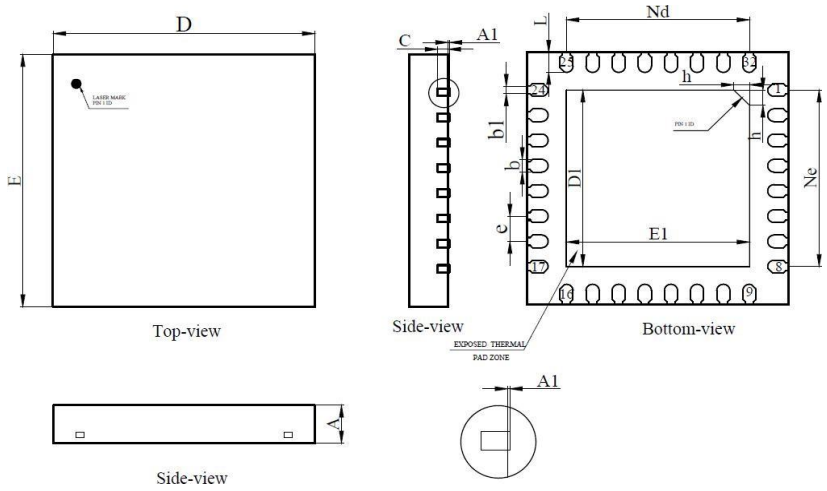

Figure10.1 Package Dimensional Drawing

Symbol	Dimensions Milimeters		
	Min	Nom	Max
A	0.75/0.85/1.00/1.30/1.70±0.05		
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.32	0.36	0.40
b1	0.15 REF		
c	0.203 REF		
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D1	3.60	3.70	3.80
E1	3.60	3.70	3.80
e	0.50 BSC		
h	0.30	0.35	0.40
L	0.35	0.40	0.45
Nd	3.50 BSC		
Ne	3.50 BSC		

Chengdu Cuiwei Electronic Co.,LTD
Address: A107, No.3 Ke Yuan Er Road, Chengdu Hi-Tech Zone, Chengdu, China
E-mail:sales@cdcwtec.com
Website: www.cdcwtec.com