CW9268 Data Manual

2024 June
V1.0

Dual Channel 16 Bit 125MSPS ADC

1.0 Overview

CW9628 It is a 16 -bit high-speed ADC product with two built-in 16- Bit and a maximum of 125MSPS Analog-to-digital converter ADC . Each channel ADC The core uses a multi- stage, differential pipeline architecture and integrates output error correction logic . Both feature wide bandwidth, differential sample-and-hold analog input amplifiers that support a variety of user - selectable input ranges. ADC Output data can be sent directly to two external 16 These outputs can be set to 1.8V. CMOS or LVDS . Flexible power-down options can significantly reduce power consumption when needed . Programming of settings and controls utilizes 3-wire SPI compatible serial interface.

CW9268 According to application requirements, 60M/80M/105M/125M can be provided The product series with different speed gears can realize flexible power consumption control and the gear can be identified through the speed grade register.

CW9268 Use 64 Leaded LFCSP Package, operating temperature range -55 ℃ ~ + 125 ℃ industrial temperature range.

2.0 application

- communication
- I/Q Demodulation system
- Smart Antenna System
- Automatic test equipment
- Ultrasound equipment
- Broadband data applications
- Multi-mode digital receiver
  GSM , CDMA2000 , TD- SCDMA ,
  LTE , W-CDMA , EDGE , WiMAX

3.0 Features

- Built-in dual-channel 125MSPS ADC
- Low power consumption, no heat sink required
- Optional on-chip dither
- Programmable ADC Internal voltage reference
- Integrated ADC Sample and hold input
- Single power supply 1.8 V Power Supply
- 1.8V CMOS/LVDS Output
- Flexible analog input range: 1Vpp Upto2Vpp
- Serial port control
- Flexible energy-saving power-down mode

4.0 Performance Indicators

- Differential analog input bandwidth: 650MHz
- Static performance: DNL -1.1 /+1.2 LSB , INL -4.0 /+4.0 LSB
- Dynamic performance (f_s = 125MSPS , input signal power - 1 dBFS)
  - *fin* = 2.4MHz
    ENOB = 12.7 Bit , SNDR = 78.3 dBFS , SNR = 78.8 dBFS
  - *fin* = 70 MHz
    ENOB = 12.6 Bit , SNDR = 77.7 dBFS , SNR = 78.1 dBFS
  - *fin* = 140 MHz
    ENOB = 12.3 Bit , SNDR = 75.6 dBFS , SNR = 76.9 dBFS
  - *fin* = 200 MHz
    ENOB = 12.0 Bit , SNDR = 73.8 dBFS , SNR = 75.3 dBFS

5.0

Simplified Block Diagram

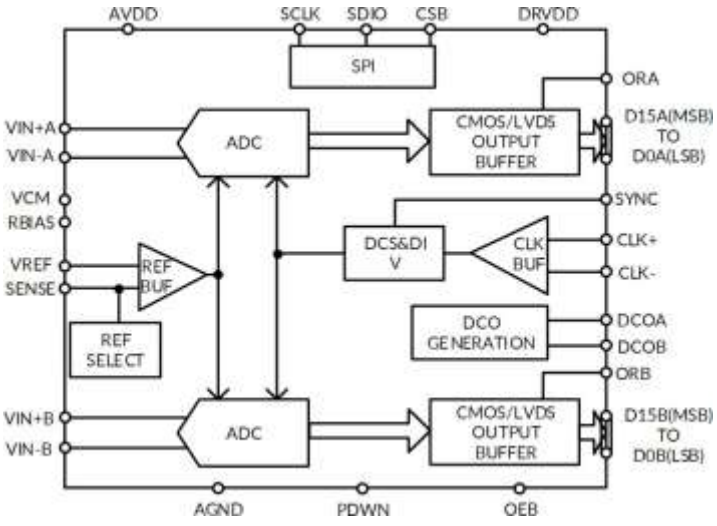


Figure 5.1 CW9268 System Block Diagram

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

6.0 Typical performance

Table **6-1** Chip usage conditions

parameter	symbol	Notes	Numeric	unit
Supply voltage	V_A	Analog circuit power supply	1.8	V
	V_{DR}	Output drive circuit power supply	1.8	V
Power-on sequence		No power-up sequence required		
land	GND_A	Analog circuit ground	0	V
	GND_{DR}	Output driver circuit ground	0	V
Differential input analog signal amplitude (1)	$V_{IN+A} - V_{IN-A}$ $V_{IN+B} - V_{IN-B}$	Input signal differential amplitude	2	Vpp
Logic input high	V_I		V_A	V
Logic input low	V_{IL}		GND	
Clock differential input signal amplitude	$V_{CLK+} - V_{CLK-}$		$0.3 \le V_{CLK+} - V_{CLK-} \le 3.6$	Vpp
Clock frequency	f_{MCLK}		$f_{MCLK} \le 625$	MHz
Operating temperature range	T_A		$-55 \le T_A \le 125$	℃

Note: (1) Measured under input frequency, full-scale sine wave, and approximately 5pF load per output bit .

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

Table**6-2** Power supply, input and output electrical characteristics

parameter	symbol	Minimum	Typical Value	Maximum	unit
Resolution			16		Bit
Supply voltage					
Analog circuit power supply	V_A	1.7	1.8	1.9	V
Output drive circuit power supply	V_D	1.7	1.8	1.9	V
Supply Current					
Analog circuit power supply	I_A (1)		390	400	mA
Output drive circuit power supply	$I_{DR(cmos)}$ (1)		55		mA
Output drive circuit power supply	$I_{DR(LVDS)}$ (1)		95		mA
Power consumption					
DC input power consumption	P_D		750	780	mW
Sine wave input power consumption (CMOS Output)			800		mW
Sine wave input power consumption (LVDS Output)			870		mW
Standby (2)			45		mW
Shutdown power consumption			0.5	2.5	mW
Analog Input					
Input differential analog signal amplitude	$V_{IN+A}-V_{IN-A}$ $V_{IN+B}-V_{IN-B}$		2		Vpp
Differential input resistance	R_{IN}		16		kΩ
Clock Input					
Clock source type	Differential sine wave				
Clock input differential swing	$V_{CLK+}-V_{CLK-}$	0.3		3.6	Vpp
Clock differential input resistance	R_{MCLK}	8	10	12	kΩ
Clock duty cycle requirements	Duty Cycle	48	50	52	%

Note: (1) The measurement conditions are input frequency, full-scale sine wave, and a load of approximately 5pF per output bit.
(2) Standby power consumption is measured under the following conditions: DC input, CLK pin is not in operation (set to AVDD or AGND).

Table**6-3** Static characteristics

parameter	symbol	Minimum	Typical Value	Maximum	unit
Differential Nonlinearity	DNL	-1.0	±0.55	1.2	LSB
Integral Nonlinearity	INL		±4	+5.8	LSB

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

Table**6-4** AC Characteristics

parameter	symbol	temperature	Minimum	Typical Value	Maximum	unit
AVDD=1.8V,DRVDD= ***1.8V*** **,** ***fs*** **= 125MSps,V** ***in*** **= - 1 dBFS , 1.0V** Internal reference voltage						
Effective Number of Bits (ENOB)	ENOB					
fin = 2.4MHz		25℃		12.7		bit
fin = 70MHz		25℃		12.6		bit
fin = 140 MHz		25℃		12.3		bit
fin = 200 MHz		25℃		12.0		bit
Signal-to-Noise Ratio (SNR)	SNR					
fin = 2.4 MHz		25℃		78.8		dBFS
fin = 70 MHz		25℃	77.2	78.1		dBFS
		Full temperature	76.5			dBFS
fin = 140 MHz		25℃		76.9		dBFS
fin = 200 MHz		25℃		75.3		dBFS
Signal-to-Noise/Distortion Ratio (SNDR)	SNR					
fin = 2.4 MHz		25℃		78.3		dBFS
fin = 70 MHz		25℃	76.8	77.7		dBFS
		Full temperature	76.2			dBFS
fin = 140 MHz		25℃		75.6		dBFS
fin = 200 MHz		25℃		73.8		dBFS
Worst second harmonic	|2nd Harm|					
fin = 2.4 MHz		25℃		95		dBc
fin = 70 MHz		25℃	89	92		dBc
		Full temperature	86			dBc
fin = 140 MHz		25℃		91		dBc
fin = 200 MHz		25℃		83		dBc
Spurious Free Dynamic Range (3rd Harmonic)	|3nd Harm|					
fin = 2.4 MHz		25℃		93		dBc
fin = 70 MHz		25℃	84	90		dBc
		Full Temp	82			dBc
fin = 140 MHz		25℃		79		dBc
fin = 200 MHz		25℃		77		dBc
Spurious Free Dynamic Range No disturbance (AIN=-23dBFS)	SFDR					
fin = 2.4 MHz		25℃		90		dBc
fin = 70 MHz		25℃		88		dBc
fin = 140 MHz		25℃		89		dBc
fin = 200 MHz		25℃		88		dBc
Spurious Free Dynamic Range With disturbance (AIN=-23dBFS)	SFDR					
fin = 2.4 MHz		25℃		106		dBc
fin = 70 MHz		25℃		105		dBc
fin = 140 MHz		25℃		106		dBc
fin = 200 MHz		25℃		104		dBc
Two-tone SFDR , no ripple						
fin = 25/28MHz (-7dBFS)	SFDR	25℃		83		dBc
Crosstalk (3) (All)		Full temp		- 95		dB
Analog input bandwidth		25℃		650		MHz

(3) Note: Crosstalk measurement conditions: One channel input parameter is -1dBFS, 100MHz signal and there is no input signal on the adjacent channel.

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

7.0 Pin Configuration and Function Description

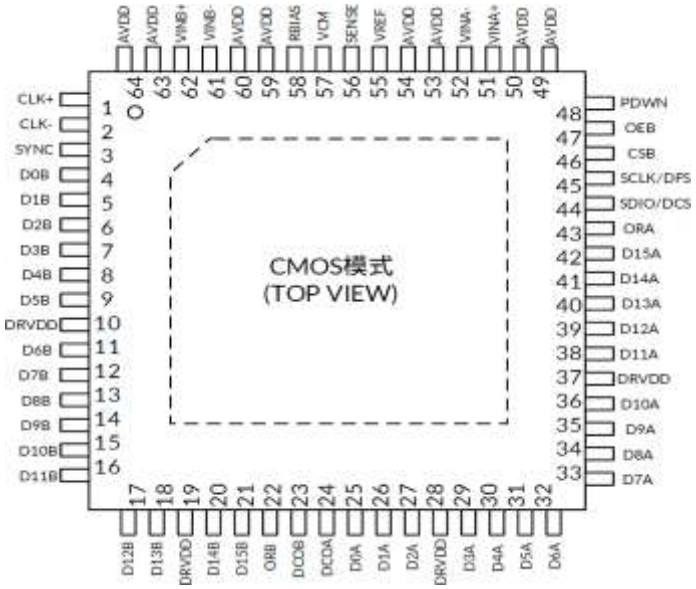


Figure 7.1 CW9268 Parallel CMOS Pinout (top view)

Table **7-1** Pin Function Description **(**Parallel **CMOS** model **)**

Pin number	symbol	Function
0	AGND, Exposed Pad	The exposed pad on the bottom of the package must be connected to ground for proper operation.
1,2	CLK+/ CLK-	Clock input positive terminal /clock input negative terminal
3	SYNC	Digital sync pin for slave mode
4,5,6,7,8,9,11,12,13,14,15,16,17,18,20,21	DB0 - DB15	Channel B digital output
10,19,28,37	DRVDD	Digital power supply (nominal value 1.8V)
22	ORB	Channel B digital output, overflow indication
23	DCOB	Digital output synchronization clock
24	DCOA	Digital output synchronization clock
25,26,27,29,30,31,32,33,34,35,36,38,39, 40,41,42	DA0- DA15	Channel A digital output
43	ORA	Channel A digital output, overflow indication
44	SDIO/DCS	SPI Data bits, low speed digital
45	SCLK/DFS	SPI Clock bit, low speed digital
46	CSB	SPI Chip select, low effective
47	OEB	Output enable, low effective
48	PDWN	Shutdown control can be controlled via SPI Configure as standby control
49,50,53,54,59,60,63,64	AVDD	Analog power supply (nominal value 1.8V)
51,52	VINA+/VINA-	A Channel input positive terminal /A Channel input negative terminal -
55	VREF	Reference voltage input / output
56	SENSE	Reference voltage mode selection
57	VCM	Output common mode bias
58	RBIAS	External reference resistor
61,62	VINB-/VINB+	B Channel input negative terminal /B Channel input positive terminal

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

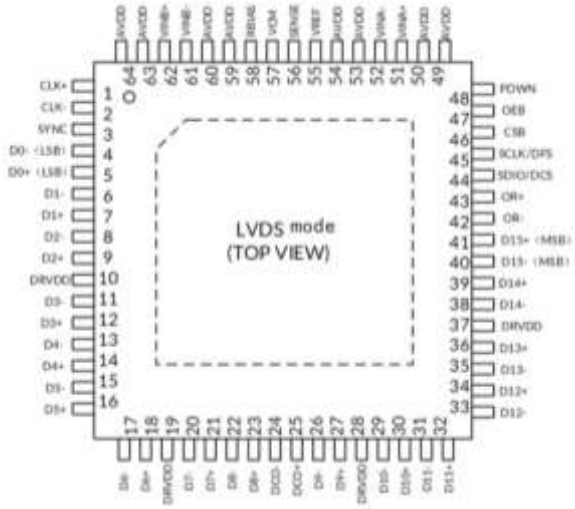


Figure7.2 CW9268 Interleaved Parallel LVDS Pinout (top view)

Table**7-2** Pin Function Description **(** Interleaved Parallel **LVDS** Mode **)**

Pin number	symbol	Function
0	AGND, Exposed Pad	The exposed pad on the bottom of the package must be connected to ground for proper operation.
1,2	CLK+/ CLK-	Clock input positive terminal /clock input negative terminal -
3	SYNC	Digital sync pin for slave mode
4,5	D0- / D0+	Channel A/B output data 0-, channel A/B Output data 0+
6,7	D1- / D1+	Channel A/B output data 1-, Channel A/B Output data 1+
8,9	D2- / D2+	Channel A/B output data 2-, Channel A/B Output data 2+
10,19,28,37	DRVDD	Digital power supply (nominal value 1.8V)
11,12	D3- / D3+	Channel A/B output data 3-, Channel A/B Output Data 3+
13,14	D4- / D4+	Channel A/B output data 4-, Channel A/B Output data 4+
15,16	D5- / D5+	Channel A/B output data 5-, Channel A/B Output data 5+
17,18	D6- / D6+	Channel A/B output data 6-, Channel A/B Output data 6+
20,21	D7- / D7+	Channel A/B output data 7-, Channel A/B Output data 7+
22,23	D8- / D8+	Channel A/B output data 8-, Channel A/B Output data 8+
24,25	DCO- / DCO+	Channel A/B Output Clock - , Channel A/B Output Clock +
26,27	D9- / D9+	Channel A/B output data 9-, Channel A/B Output data 9+
29,30	D10- / D10+	Channel A/B output data 10-, Channel A/B Output data 10+
31,32	D11- / D11+	Channel A/B Output data 11-, channel A/B Output data 11+
33,34	D12- / D12+	Channel A/B output data 12-, Channel A/B Output data 12+
35,36	D13- / D13+	Channel A/B output data 13-, Channel A/B Output data 13+
38,39	D14- / D14+	Channel A/B output data 14-, Channel A/B Output data 14+
40,41	D15- / D15+	Channel A/B output data 15-, Channel A/B Output data 15+
42,43	OR- /OR+	Channel A/B Over range output -, Channel A/B Over range output +
44	SDIO/DCS	SPI Data bits, low speed digital
45	SCLK/DFS	SPI Clock bit, low speed digital
46	CSB	SPI Chip select, low effective
47	OEB	Output enable, low effective

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

Pin number	symbol	Function
48	PDWN	Shutdown control can be controlled via SPI Configure as standby control
49,50,53,54,59,60,63,64	AVDD	Analog power supply (nominal value 1.8V)
51,52	VINA+/VINA-	A Channel input positive terminal /A Channel input negative terminal
55	VREF	Reference voltage input / output
56	SENSE	Reference voltage mode selection
57	VCM	Input common mode bias
58	RBIAS	External reference resistor
61,62	VINB-/VINB+	B Channel input negative terminal /B Channel input positive terminal

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

8.0 Typical performance test curve

AVDD = 1.8 V ,DRVDD = 1.8 V , nominal sampling rate, 1.0 V internal reference, 2 V p-p differential input, VIN = -1.0 dBFS ,16 K samples, T_A = 25°C , unless otherwise noted .

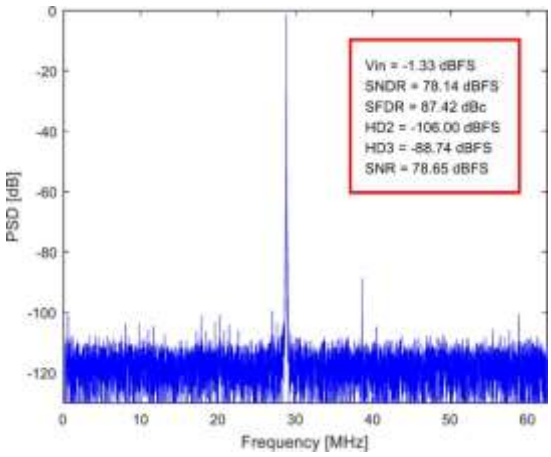


Figure 8.1 Single tone FFT (fin = 29MHz)

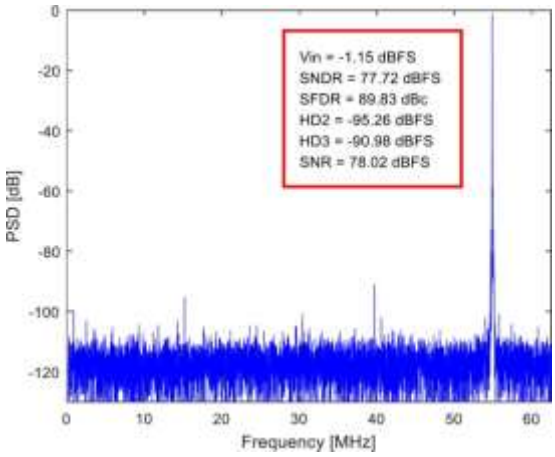


Figure 8.2 Single tone FFT (fin = 70MHz)

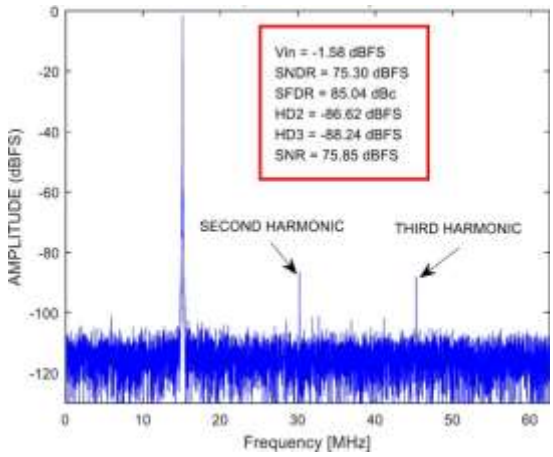


Figure 8.3 Single tone FFT (fin = 140MHz)

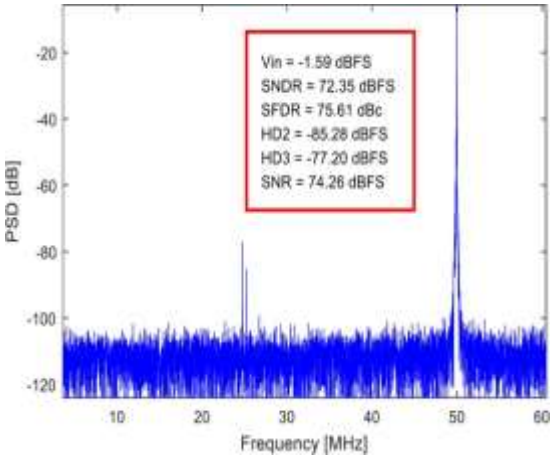


Figure 8.4 Single tone FFT (fin = 200MHz)

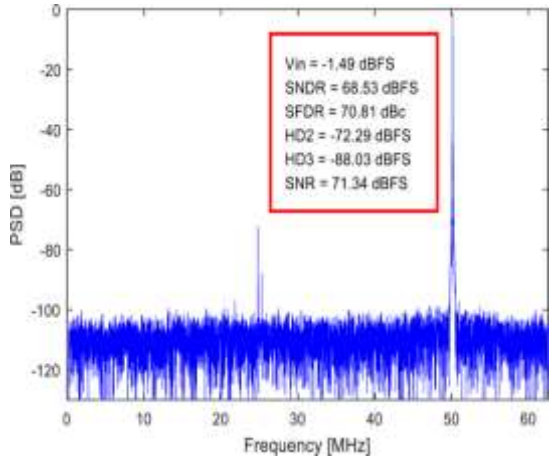


Figure 8.5 Single tone FFT (fin = 300MHz)

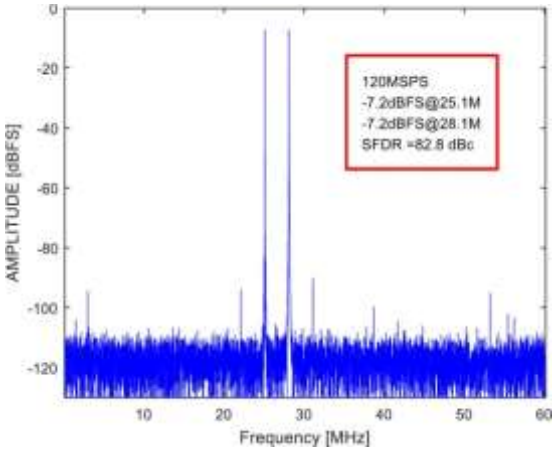


Figure 8.6 Dual tone @120MSps Spectrum

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

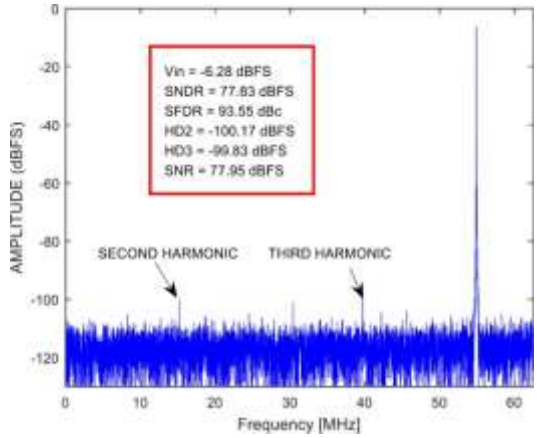


Figure8.7 Single tone FFT (fin = 70MHz@-6dBFS, dither enabled)

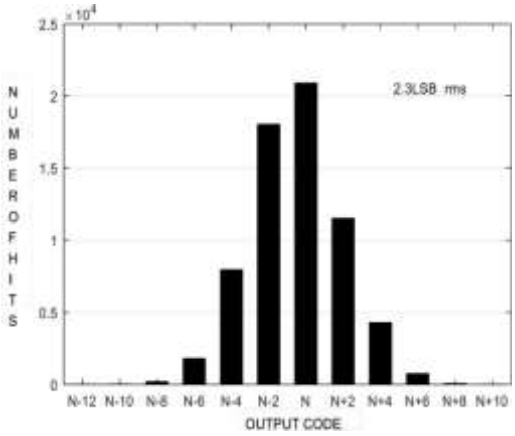


Figure8.8 Ground Input Histogram

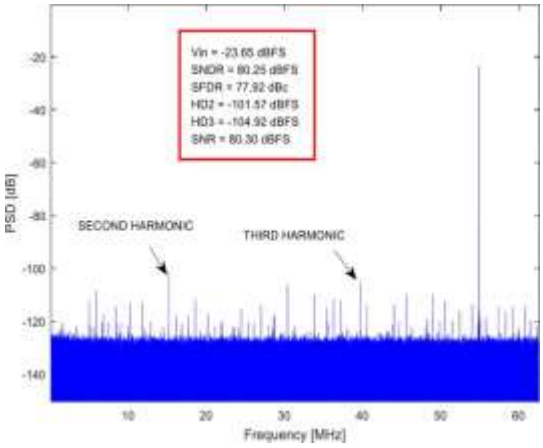


Figure8.9 Single tone FFT (fin = 70MHz@-23dBFS, dither disabled , 1M point)

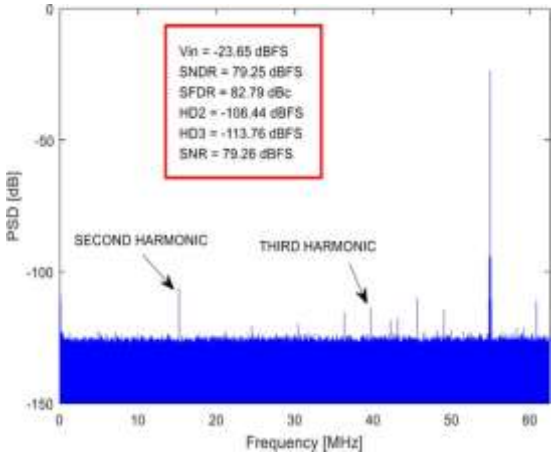


Figure8.10 Single tone FFT (fin = 70MHz@-23dBFS, dither enabled , 1M point)

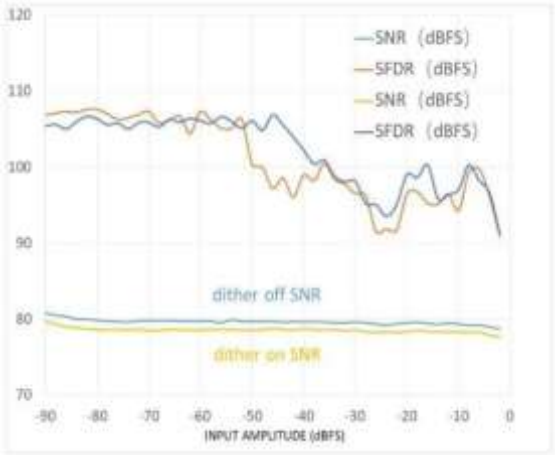


Figure 8.11 SNR/SFDR Relationship with input amplitude (fin = 30MHz , dither disabled / enabled)

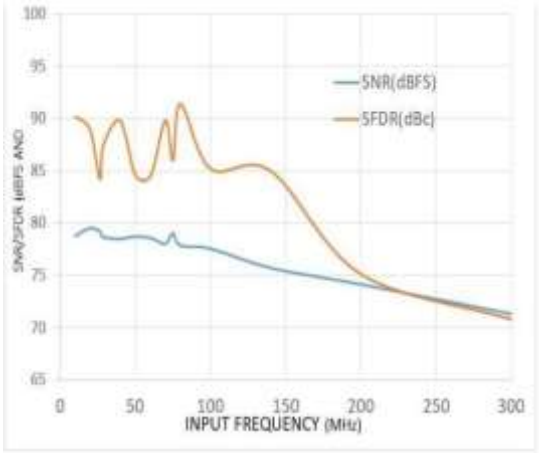


Figure 8.12 SNR/SFDR Relationship with input frequency

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

9.0 Timing diagram

9.1 Data Timing

Unless otherwise specified, AVDD = 1.8 V , DRVDD=1.8 V , typical sampling rate, VIN=−1.0dBFS Differential input, 1.0V Internal reference voltage.

Table **9.1** Switch parameters

parameter	temp	Minimum	Typical Value	Maximum	unit
Clock input parameters					
Input clock rate	Full temp			625	MHz
Conversion rate					
DCS Enable	Full temp	20		125	MSPS
DCS Disable	Full temp	10		125	MSPS
Clock cycle, divide-by-one mode (t_{CLK})	Full temp	8			ns
Clock pulse width high level (t_{CH})					
One-way mode, DCS Enable	Full temp	2.4	4	5.6	ns
One-way mode, DCS Disable	Full temp	3.8	4	4.2	ns
Divide-by-2 to Divide-by-8 Modes	Full temp	0.8			ns
Aperture delay (t_A)	Full temp		1.0		ns
Aperture jitter (t_j)	Full temp		0.07		ps
Data output parameters					
Data transfer delay (t_{PD})	Full temp	2.8	3.5	4.2	ns
DCO Propagation Delay (t_{DCO})	Full temp		3.8		ns
DCO To data offset (t_{SKEW})	Full temp	0.1	0.35	0.6	ns
LVDS model	Complete				
Data transfer delay (t_{PD})	Full temp	2.9	3.7	4.5	ns
DCO Propagation Delay (t_{DCO})	Full temp		3.3		ns
DCO To data offset (t_{SKEW})	Full temp	- 1.1	- 0.45	- 0.2	ns
CMOS Mode pipeline delay	Full temp		12		cycle
LVDS Mode Delay, Channel A/B	Full temp		12.5/12		cycle
Wake-up time	Full temp		500		us
Out of range recovery time	Full temp		2		cycle

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

Table9.2 Timing parameters

parameter	condition	Minimum	Typical Value	Maximum	unit
Synchronous timing requirements					
tSSYNC	SYNC To the rising edge of CLK+ setup time		0.3		ns
tHSYNC	SYNC to rising edge of CLK+ hold time		0.4		ns
SPI Timing requirements					
dD	Data and SCLK Setup time between rising edges	2			ns
DH	Data and SCLK Hold time between rising edges	2			ns
tCLK	SCLK cycle	40			ns
t_S	CSB With SCLK The build time between	2			ns
t_H	CSB With SCLK Keep time between	2			ns
t_{HIGH}	SCLK High level pulse width	10			ns
t_{LOW}	SCLK Low level pulse width	10			ns
tEN_SDIO	Relative to SCLK Falling edge, SDIO The time required for a pin to switch from input state to output state	10			ns
tDIS_SDIO	Relative to SCLK Rising edge, SDIO The time required for a pin to switch from an output state to an input state	10			ns

9.2 Timing diagram

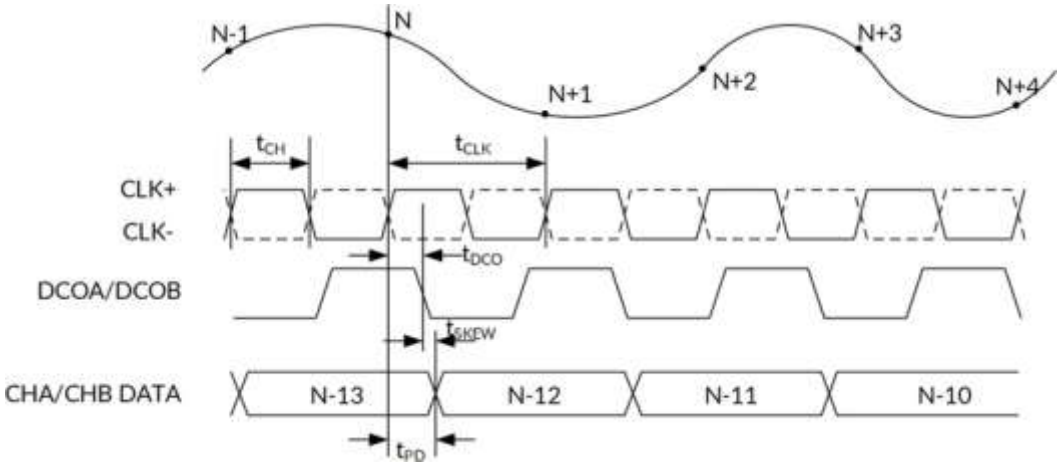


Figure 9.1 CMOS Default output mode data output timing

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

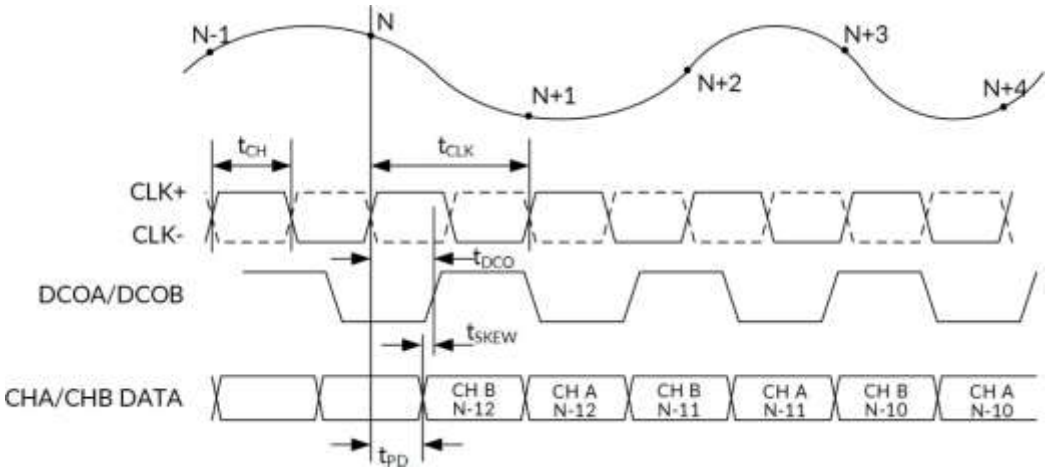


Figure 9.2 CMOS Data output timing in interleaved output mode

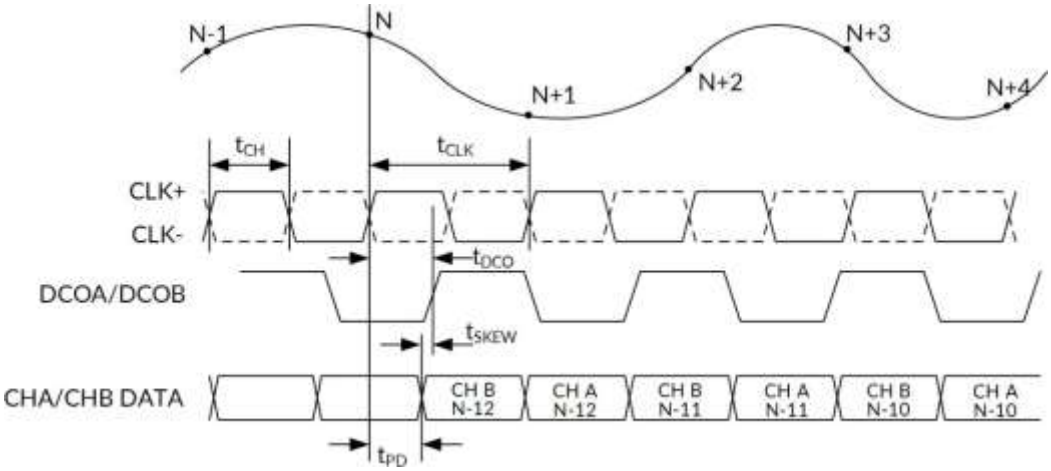


Figure 9.3 LVDS Mode data output timing

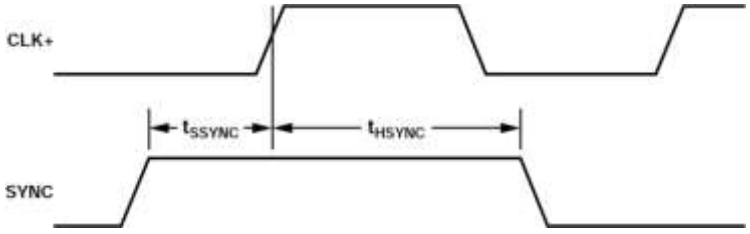


Figure 9.4 SYNC Input Timing Requirements

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

10.0 Typical Application Circuit

CW9268 The typical application circuit of the input signal, input clock, external DC pin and other peripheral devices is as follows.

10.1 Analog Input Network

In baseband applications where SNR is a critical parameter, the recommended input configuration is differential transformer coupling, as shown in Figure 10.1. In order to bias the analog input, the VCM voltage must be connected to the center tap to the secondary winding of the transformer.

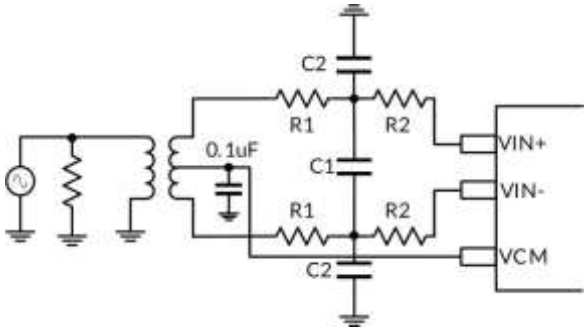


Figure10.1 Differential Transformer Coupled Configuration

When selecting a transformer, its signal characteristics must be considered. Most RF transformers operate at frequencies below a few MHz. Excessive signal power can also cause the core to saturate, resulting in distortion.

When the input frequency is in the second or higher Nyquist region, the noise performance of most amplifiers cannot meet the requirements to achieve the true SNR performance of the ADC. In applications where SNR is a critical parameter, the recommended input configuration is differential dual balun coupling, as shown in Figure 10.2. In this configuration, the inputs are AC coupled and the CML is supplied to each input through a 33Ω resistor. These resistors compensate for the loss of the input balun, providing a 50 Ω impedance to the drive.

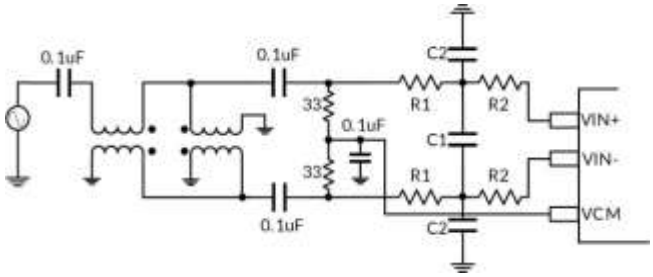


Figure10.2 Differential Dual Balun Input Configuration

In the double balun and transformer configuration, the values of the input capacitors and resistors depend on the input frequency and source impedance and may need to be reduced or removed. Table 1 0. 1 Recommended values for setting up the RC network are listed . When the input frequency is high, adding a ferrite bead in series with the resistor and removing the capacitor can achieve good performance. However, these values depend on the input signal and should only be used as an initial reference.

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

Table 10.1 RC Network Example

Frequency range /MHz	Series resistance **R1/Ω**	Series resistance **R2**/ Ohm	Differential capacitance **C1/pF**	Parallel capacitor **C2/pF**
0-100	33	15	5	15
100- 200	10	10	5	10
200-300	10 [7]	66	none	none

Note: In the configuration, R1 is a ferrite bead, and its value is 10 Ohms @ 100MHz.

10.2 Clock Input Network

to the performance of the chip, a differential signal should be used as CW9268 The clock signal at the sampling clock input (CLK +/ CLK -) . Typically, this signal should be AC-coupled into the CLK+ and CLK- pins using a transformer or two capacitors . The CLK+ and CLK- pins are internally biased, as shown in Figure 10.3 If these inputs are left floating, the CLK- pin should be pulled low to prevent stray clocks.

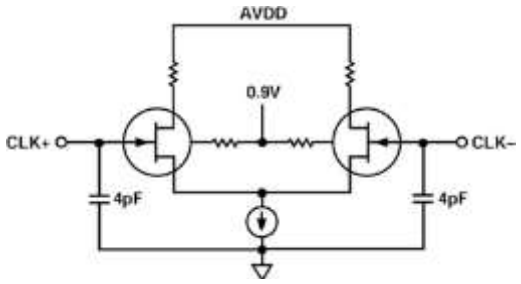


Figure 10.3 Equivalent clock input configuration

The clock input structure of the CW9268 is very flexible. CMOS, LVDS, LVPECL or sine wave signals can be used as their clock input signals. Regardless of which signal is used, clock source jitter must be taken into account.

Figure 10.4 and Figure 10.5 are two preferred methods of providing clock signals for the CW9268 (clock rates up to 625MHz). The single-ended signal of a low-jitter clock source can be converted into a differential signal using RF balun or RF transformer. For clock frequencies of 125MHz to 625MHz, it is recommended to sample the RF balun configuration; For clock frequencies of 10MHz to 200MHz, it is recommended to sample the RF transformer configuration. A back-to-back Schottky diode across the transformer/balun secondary can limit the clock signal input into the ADC to about a differential 0.8 V peak-to-peak. In this way, the large voltage swing of the clock can be prevented from feeding through to other parts of the ADC, and the rapid rise and fall time of the signal can be preserved, which is very important for low jitter performance.

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

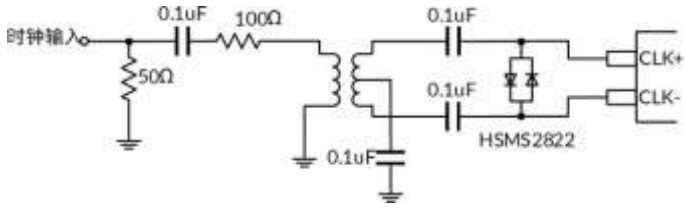


Figure 10.4 Transformer coupled differential clock (up to 200MHz)

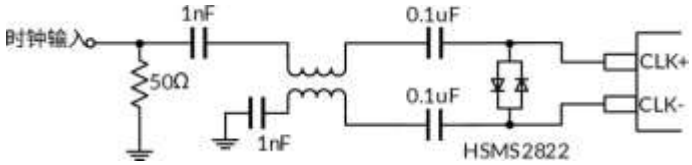


Figure10.5 Balun coupled differential clock (frequency up to 625MHz)

10.3 Benchmark configuration

CW9628The built-in comparator can detect the SENSE pin voltage, thereby configuring the reference voltage into two different modes (see Table 1.2) . pin to ground, the reference amplifier switches internally to VREF Set to 1.0V (for 2.0 V p p In this mode , SENSE Ground, can also be connected via SPI Port adjustment full scale, see the corresponding SPI Register. Set SENSE Pin and VREF pins connected, 0.5 V is provided Reference output voltage (for 1 V p p If the chip is connected to an external resistor divider as shown in Figure 10.6 As shown, the reference amplifier enters the programmable reference voltage mode, VREF The output voltage is calculated as follows :

$$VREF = 0.5 \times (1 + \frac{R2}{R1})$$

Whether the chip uses an internal reference voltage or an external reference voltage, the ADC The voltage input range of the reference voltage pin (VREF) is always twice the voltage.

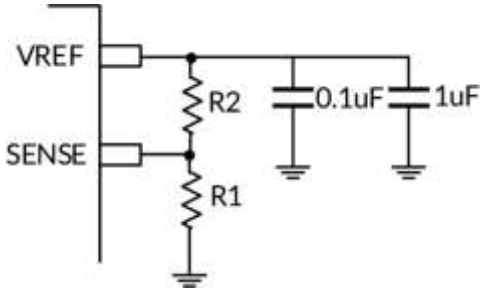


Figure 10.6 Programmable reference voltage mode

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

Table**10.2** Reference Voltage Configuration Summary

Selected Mode	**SENSE** Voltage	The corresponding **VREF**（**V**）	Corresponding differential range（**Vpp**）
External reference voltage	AVDD	N/A	2× external reference voltage
Internal fixed reference voltage	VREF	0.5	1.0
Programmable reference voltage	0.2V To VREF	$0.5\times(1+\frac{R2}{R1})$	2×VREF
Internal fixed reference voltage	AGND To 0.2V	1.0	2.0

10.4 Digital Output

The CW9268 output drivers can be configured to operate with 1.8 V CMOS logic family interface. In addition, using a 1 . 8 V DRVDD Power supply, you can also use CW9628Configured as LVDS Output (standard ANSI or small output swing mode) . In CMOS output mode, the output driver should provide enough output current to drive various logic circuits . However, large drive current may cause glitch pulses in the power supply signal, affecting the performance of the converter.

Therefore, in those applications where ADC In applications where the output is to drive large capacitive loads or have a large fan-out, an external buffer or latch may be required. The default output mode is CMOS, and each channel is output on a separate bus, as shown in Figure 9.1 As shown. It can also be connected via SPI port configures the output as interleaved CMOS mode. In this interleaved CMOS In this mode, the data of both channels are output through the output bit of channel A and the output bit of channel B. The output is placed in high impedance mode. The timing diagram of the output mode is shown in Figure 9.2 shown.

In external pin mode, set SCLK/DFS The pin can control the data to be output in offset binary format or two's complement format (see Table 10.3 and Table 10.4) , in SPI control mode, the output format of data can be offset binary, two's complement or Gray code.

Table**10.3 SCLK** , **SDIO** External pin mode selection

Pin voltage	**SCLK/DFS**	**SDIO/DCS**
AGND	offset binary (default)	DCS Disabled (default)
AVDD	Two's complement	DCS Enable

Input (**V**)	condition	Offset Binary Mode	Two's complement mode	Over range
VIN+ - VIN-	< - VREF – 0.5LSB	0000 0000 0000 0000	1000 0000 0000 0000	1
VIN+ - VIN-	= - VREF	0000 0000 0000 0000	1000 0000 0000 0000	0
VIN+ - VIN-	=0	1000 0000 0000 0000	0000 0000 0000 0000	0
VIN+ - VIN-	=+VREF – 1LSB	1111 1111 1111 1111	0111 1111 1111 1111	0
VIN+ - VIN-	> +VREF – 0.5LSB	1111 1111 1111 1111	0111 1111 1111 1111	1

Table**10.4** Data output format

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

11.0 Serial Port Interface (SPI)

CW9268 The serial port interface (SPI) allows the user to utilize the ADC An internal structured register space is used to configure the converter to meet specific functional and operational needs. SPI It is flexible and can be customized to the specific application. The address space can be accessed, read and written through the serial port. The memory space is organized in bytes and can be further subdivided into multiple areas as described in the memory map section.

11.1 Configuration

The AD C SPI Consists of three parts : SCLK/DFS Pins, SDIO/DCS Pins and CSB pins are shown in Table 1 1 . 1 The SCLK/DFS (serial clock) pin is used to synchronize the A / D The SDIO/DCS (serial data input / output) dual function pin allows data to be sent to the internal ADC The CSB (Chip Select Signal) pin is an active low control pin that enables or disables read and write cycles

Table**11.1 SCLK** , **SDIO** External pin mode selection

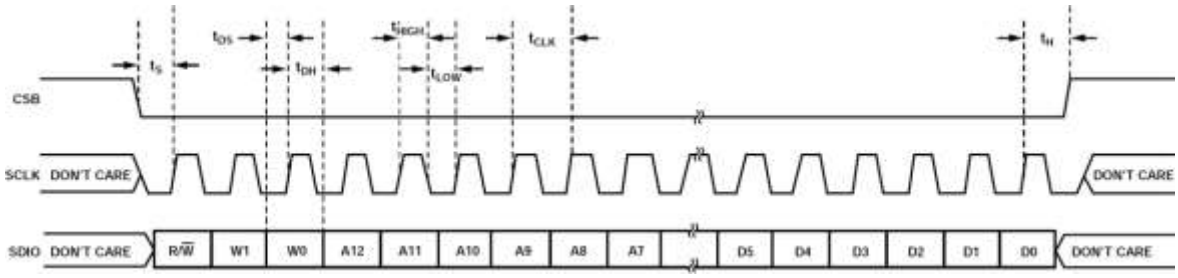
Pinout	Function
SCLK	Serial Clock. Serial shift clock input used to synchronize the serial interface.
SDIO	Serial data input / output, usually used as input or output, depending on the instructions sent and the relative position in the timing frame.
CSB	Chip Select Signal. An active low control signal used to select read and write cycles.

CSB The falling edge of SCLK and the rising edge of SCLK together determine the start of the frame. An example of a serial timing diagram is shown in Figure 11.1 shown.

CSB can operate in multiple modes. When CSB is always held low, the device is always enabled, which is called streaming. CSB can stay high between bytes to allow for other external timing. CSB When the pin is pulled high, the SPI The function is in high impedance mode. In this mode, you can turn on SPI Secondary function of pin .

In one instruction cycle, a 16 After the instruction is transmitted, data will be transmitted. The data length is determined by the W0 bit and the W1 bit. Joint decision.

In addition to the word length, the instruction cycle also determines whether the serial frame is a read operation instruction or a write operation instruction, thereby programming the chip or reading data from the on-chip memory through the serial port. The first bit of the first byte of a multi-byte serial data transmission frame indicates whether a read command or a write command is issued. If the instruction is a read-back operation, executing the read-back operation will cause the data transmission direction of the serial data input / output (SDIO) pin to change from input to output at a certain position in the serial frame. All data consists of 8 -bit words. Data can be transmitted in MSB first mode or LSB first mode. After the chip is powered on, the MSB is used by default. The preferred method is to use SPI Port configuration registers to change the way data is sent.



ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

Figure 11.1 SPI Serial Port Interface Timing

11.2 Configuration

When not using SPI In applications where the control register interface is used, SDIO/DCS pin, SCLK/DFS pin, OEB pin, and PDWN pins are used as independent CMOS When the device is powered up, it is assumed that the user wishes to use these pins as static control lines to control the duty cycle stabilizer, output data format, output enable, and power-down feature control, respectively . In this mode, the CSB chip select pin should be tied to the AVD D Connect to disable the serial port interface.

When the device is in SPI Mode , PDWN and OEB pins are still valid. Control output enable and power down, OEB should be and PDWN The pins are set to the default state, as shown in Table 1 1 .2 shown.

Table **11.2 SCLK**, **SDIO** External pin mode selection

Pinout	External voltage	Configuration
SDIO/DCS	AVDD	Duty cycle stabilizer enable
	AGND (default)	Duty Cycle Stabilizer Disable
SCLK/DFS	AVDD	Twos complement enable
	AGND (default)	Offset Binary Enable
OEB	AVDD	Output is in high impedance state
	AGND (default)	Output Enable
PDWN	AVDD	The chip is in power-off or standby state
	AGND (default)	Normal operation

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

12.0 Application Information

12.1 Design Guide

In the CW9268 Before designing and laying out a system, it is recommended that the designer familiarize themselves with the following design guidelines, which discuss the special circuit connections and layout requirements required for certain pins .

12.2 Power and Grounding Recommendations

to use two independent 1.8 V Power supply: CW9628 Power supply: one for analog AVDD and one for digital DRVDD . a n d DRVDD , multiple different decoupling capacitors should be used to support high and low frequencies. The decoupling capacitors should be placed close to the PCB The entry point should be located close to the device pins and the trace length should be kept as short as possible .

CW9268 Only one PCB required Ground plane . Reasonable decoupling and clever separation of analog, digital and clock modules can easily achieve the best performance .

12.3 LVDS operate

When powered on, CW9628 CMOS is used by default Output mode. If LVDS is required Working mode, must use SPI after power on Configuration register sets this mode. When CW9628 Power on in CMOS mode, and the output has LVDS When the termination resistor (100Ω) is connected, DRVDD Current may be higher than typical unless the device is placed in LVDS mode. This additional DRVDD The current will not damage the CW9268 , but the maximum DRVDD of the device should be considered. This must be taken into account when current is drawn.

To eliminate this additional DRVDD current, the OEB pin can be pulled high at power-up to disable the CW9628 Output. Through SPI The port places the device in the LVDS After the mode , the OEB pin can be pulled low to enable the output.

12.4 Exposed Pad Heatsink Recommendations

To achieve the best electrical and thermal performance, the AD C The exposed pad on the bottom side should be connected to the analog ground AGND . The exposed (solder mask - free) continuous copper plane on the PCB should be connected tothe CW9268 The exposed pad (pin 0) of the

The copper plane should have multiple vias in order to obtain the lowest possible thermal resistance path through the PCB. The bottom is used for heat dissipation. These through holes should be filled or blocked to prevent tin seepage through the through holes and affect the connection performance.

In order to maximize the A/ C With PCB To cover and connect the two parts, a silk screen layer should be covered on the PCB to divide the continuous plane on the PCB into multiple equal parts. In this way, during the reflow process, the A C A continuous, undivided plane only guarantees multiple connection points between the A /D C There is one connection point tothe PCB .

12.5 VCM

VCM The pin should be connected through a 0.1uF Capacitor decoupling to ground.

12.6 RBIAS

CW9628 The user is required to connect a 10kΩ Resistor placed at RBIAS pin and ground. This resistor is used to set the A/ D The resistor has a tolerance of at least 1% .

12.7 Reference Decoupling

VREF pin should be connected to an external low ESR 0.1uF capacitor and a low ESR 1.0uF Parallel decoupling capacitor to ground.

12.8 **SPI** port

When the full dynamic performance of the converter is required, the SPI should be disabled. port. Usually the SCLK signal, CSB signal, and SDIO signal are asynchronous to the ADC clock, so noise in these signals can degrade converter performance. bus, you may need to connect the CW9268 A buffer is connected between the two to prevent these signals from changing at the input of the converter during the critical sampling period.

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

13.0 Register List

Address 0x08 To address 0x1 8 and address 0x 3 0 is masked unless a Writing 0 x 0 1 sets the transfer bit to issue a transfer command, otherwise, writing to these addresses will not affect the operation of the device. In this way, these registers can be updated internally at the same time when the transfer bit is set. When the transfer bit is set, the internal update is performed and the transfer bit is automatically cleared.

the key registers are loaded with default values. The default values for each register are listed in Table 13.1 (Memory Map Register Table). The device does not currently support the default values in Table 13.1 . All addresses and bits not included in .

Table**13.1** Register List

address (HEX)	Register Name	Bit 7 (MSB)	Position 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	default value (HEX)	Notes
Chip Configuration Register											
0x00	SPI Port Configuration	0	LSB first	Soft reset	0	0	Soft reset	LSB priority	0	0x00	Inter-nibble mirroring
0x01	Chip ID	8 -bit chip ID (CW9268=0x32)								0x32	Read-only
0x02	Chip level			Speed Class ID 01 = 125M , 10 = 105M 11 = 80M ,00 = 60M						0x01	Distinguish device level ; read-only
Channel Index and Transfer Registers											
0x05	Channel Index	0	0	0	0	0	0	Channel B	Channel A	0x03	Channel Selection
0xFF	Teleport	0	0	0	0	0	0	0	Teleport	0x00	Transport Control
ADC Function											
0x08	Power Mode	1	0	External power-down pin function 0 = power off, 1 = standby	0	0	0	00 = normal operation, 01 = complete power down 10 = s t a n d b y , 11 = normal operation		0x80	Determines the general operating mode of the chip
0x09	Global clock	0	0	0	0	0	0	0	Duty Cycle Stabilizer	0x00	
0x0B	Clock Divider	0	0	0	0	0	000 = 1 , 001 = 2 , 010 = 3 , 011 = 4 . 100 = 5 , 101 = 6 , 110 = 7 , 111 = 8			0x00	Clock division
0x0E	BIST Enable	0	0	0	0	0	0	0	BIST Enable	0x00	
0x0F	ADC Input	0	0	0	0	0	0	0	Common mode servo enable	0x00	
0x10	Offset Adjustment	Offset adjustment in LSB units from +127 to -128 (twos complement format)								0x00	
0x14	Output Mode	0 = ANSI LVDS, 1 = Small swing LVDS	0 = CM0S, 1 = LVDS	CMOS output staggered enable	Output Enable	CMOS drive force control : 0 = x1,1 = x2	Output inversion	00 = Offset Binary 01 = Two's complement 10 = Gray code 11 = RAND encoding		0x00	Configuring output and data formats
0x16	Clock bit control	DCO Inversion	0	0	0	0	000 = no delay, 001 = 1 input clock cycle, 002 = 2 input clock cycles, 003 = 3 input clock cycles, 004 = 4 input clock cycles, 005 = 5 input clock cycles, 006 = 6 input clock cycles, 007 = 7 input clock cycles, 008 = 8 input clock cycles			0x00	Allows selection of clock delay time for input clock divider
0x17	DCO output delay	0	0	0			Under typical conditions, the delay per bit is about 80ps, and the total delay = 2500ps* register /31 00000 = 0ps , 00001 = 81ps, ... , 11111 = 2500ps			0x00	
0x18	ref_sel	11 = 2Vpp (default) , 10 = 1.75Vpp 01 = 1.5Vpp , 00 = 1.25Vpp		0	0	0	0	0	0	0xC0	Read Display <1:0>
0x30	Disturbance Enable	0	0	0	Disturbance Enable	0	0	0	0	0x00	
0x100	Synchronous control	0	0	0	0	0	The clock division is synchronized only with the next sync pulse	Clock Divider Synchronous Enable	Host synchronization enable	0x00	

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

13.1 Synchronous control

Bit 2 -- Clock divider is synchronized only with the next: pulse if the master sync enable bit (address 0 x 10 0 bit 0 of address 0) and the clock divider synchronization enable bit (address 0 x 1 0 0 If bit 1) of Allows the clock divider to synchronize with the next sync pulse it receives and ignore other sync pulses. After synchronization, the clock divider sync enable bit (Address 0x1000 Bit 1) is reset.

Bit 1 --Clock divider synchronization enable: Bit 1 This is the sync pulse that selects the clock divider. High level and bit 0 When high, the sync signal is enabled. This is continuous sync mode.

Bit 0 - Host synchronization enable To enable: any synchronization function, bit 0 Must be high. If the synchronization function is not used, this bit should be kept low to save power.

14.0 Packaging information

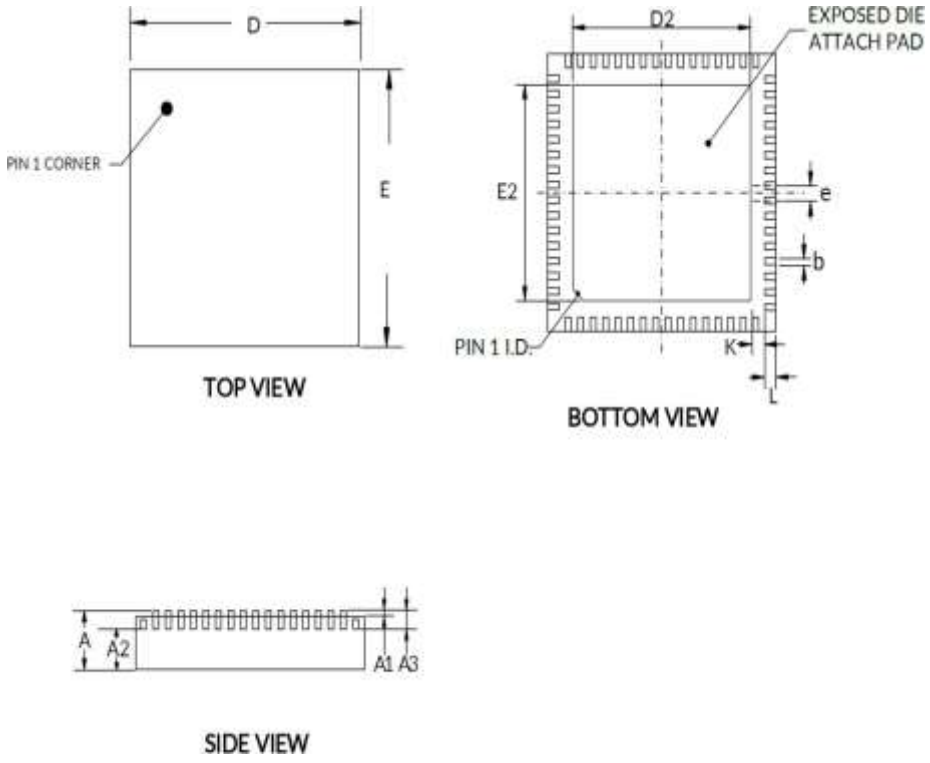


Figure 14.1 CW9268 Package Outline

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com

Symbol	Dimensions Milimeters	
	Min	Max
A (1)	0.800	0.900
A1	0.000	0.050
A2	0.650	
A3	0.203REF (2)	
B	0.200	0.300
D (1)	9.000 BSC (3)	
E (1)	9.000 BSC (3)	
E	0.500 BSC (3)	
D2	7.100	7.300
E2	7.100	7.300
L	0.300	0.500
K	0.500REF (2)	

Note: (1) Not including each side 0.075 maximum mm plastic or metal protrusions.

(2) REF It is the abbreviation of Reference.

(3) BSC (Basic Spacing Between Centers) , the" basic " spacing is nominal.

15.0 Ordering Information

Order Model	Operating temperature	Package	Implementation standards (quality levels)
CW9268	- 55°C ~ +125°C	Plastic LFCSP (64 foot)	Military temperature level

ChengduCuiweiElectronicCo., LTD
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China
E-mail: sales @ cdcwtec.com
Website:www.cdcwtec.com