CW9689 Data Sheet

Low power dual channel 14- Bit , 2.6 GSPS high speed ADC

1. Overview

The CW9689 is a dual-channel, 14 -bit, 2.6GSPS analog-to-digital converter (ADC) . The device has an on-chip buffer and a sample / hold circuit designed for low power, small size, and ease of use . This product is designed to support communication applications that can directly sample wide bandwidth analog signals up to 5GHz . The −3dB input bandwidth of the ADC is 6GHz . CW9689 has the advantages of large input bandwidth, high sampling rate, good linearity, small package, and low power consumption.
The dual-channel ADC core uses a multi-stage differential pipeline structure with integrated output error correction logic. Each ADC has a wide bandwidth input to support a variety of user-selectable input ranges. The integrated reference voltage source simplifies the design complexity. The analog input and clock signals are differential inputs. The ADC data output is connected to four digital down converters (DDCs) through an internal cross multiplexer . Each DDC consists of multiple cascaded signal processing stages, including: a 48 -bit frequency converter (digitally controlled oscillator (NCO)) and a decimation rate. The NCO can select preset frequency bands on the general-purpose input / output (GPIO) pin. Up to three frequency bands can be selected. The switching of the CW9689 between DDC modes is controlled by an SPI programmable configuration file.

2. application

- Multi-frequency / multi-mode digital receiver
- Electronic test and measurement systems
- Phased Array Systems
- High speed test equipment
- Broadband radar
- 3G/4G digital communications

3. Features

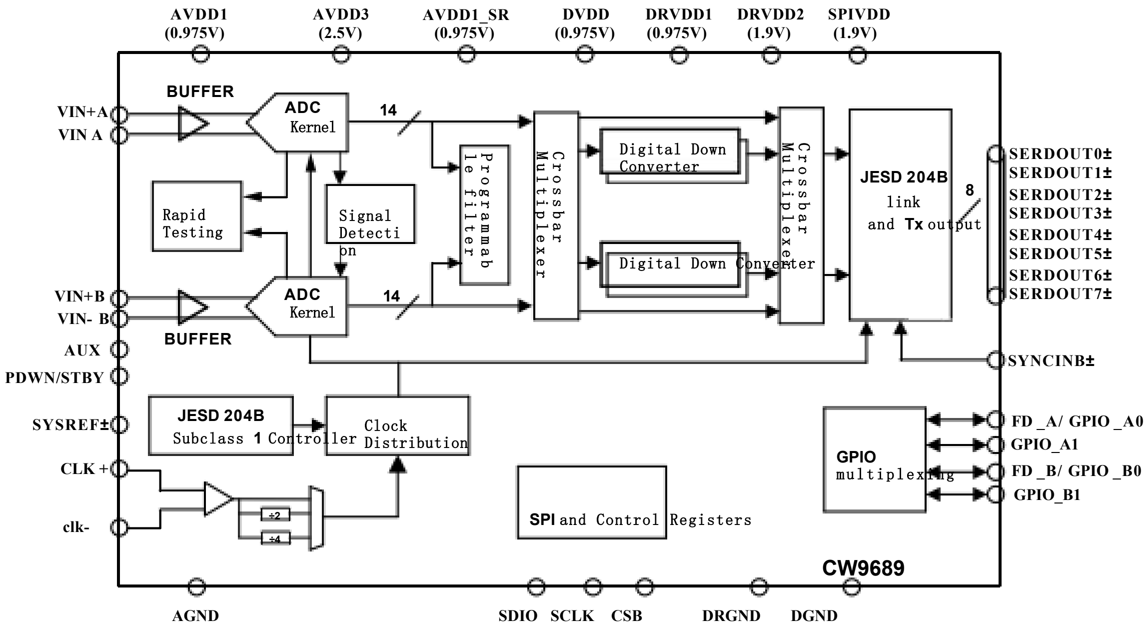
- Integrated input buffer
- Analog input bandwidth6 GHz (-3 dB)
- Over-range fast detection
- Each roadADC There are two integrated data processing channels
- support4 channelsNCO Quick Switch
- Low power consumption,No heat sink required
- Plastic packagingFC - PBGA 196 (12 mm ×12 mm, 0.8 mm Ball spacing)
- With importAD 9689 andAD 9208 Pin compatible

4. Performance Indicators

- Full Power Bandwidth: 6 GHz (-3 dB)
- Dynamic performance (f_s = 2.4 GSPS , input signal power -2 dBFS)

— f_{in} = 155 MHz
ENOB = 9.42 Bit， SFDR = 72.94 dBFS， SNR = 59 dBFS
— f_{in} =750MHz
ENOB = 9.23 Bit， SFDR = 68.42 dBFS， SNR =57.9 dBFS
— f_{in} = 900MHz
ENOB = 9.17 Bit， SFDR = 69.34 dBFS， SNR = 57.3 dBFS
— f_{in} = 1800 MHz
ENOB = 8.96 Bit， SFDR = 66.68 dBFS， SNR = 56.3 dBFS
— f_{in} = 2100 MHz
ENOB = 8.74 Bit， SFDR = 65 dBFS， SNR = 55 dBFS
— f_{in} = 3300 MHz
ENOB = 8.3 Bit， SFDR = 60.2 dBFS， SNR = 52.5 dBFS

5. Simplified Block Diagram



picture 1 CW9689 Block Diagram

6. Functional Description

CW9689 is a 14 -bit 2.6 GSPS analog-to-digital conversion chip with a flexible and configurable sampling rate. CW9689 contains 2 independent ADCs , each of which contains an input buffer that supports DC input. The analog input -3dB bandwidth is greater than 6GHz , which can ensure stable ADC performance when the input signal exceeds 8GHz .
Built-in 4- channel DDC module, can support two ADCs with flexible and configurable real or complex input. DDC can also flexibly configure real or complex output.
Multiple DDCs are connected through a cross-switch matrix, supporting up to 4 frequency bands. At the same time, it supports NCO fast switching frequency.

In addition to the DDC module, the CW9689 can also simplify the design of AGC functions in communication receivers. The programmable threshold detector allows the input signal power to be monitored using the fast detect control bits in the ADC register. If the input signal level exceeds the programmable threshold, the fast detect indication signal goes high. Because this threshold indication has low latency, the user can quickly turn down the system gain to avoid over-range conditions at the ADC input. In addition to the fast detect output, Built-in signal amplitude monitoring function, convenient for system configuration of automatic gain control AGC . Up to 8 JESD204B channels supporting up to 16Gbps . Multiple modes for flexible user configuration.

With built-in SYSREF automatic correction function, the internal algorithm can quickly align high-speed clock and SYSREF , which can be applied to multi-chip synchronization in various scenarios.
The CW9689 has two analog input channels and eight JESD204B paired output channels. The CW9689 is optimized for wide input bandwidth, high sampling rate, good linearity and low power in a very small package.
This dual-channel ADC core samples a multi-stage, differential pipeline architecture and integrates output error correction logic. Each ADC has a wide bandwidth input to support a variety of user-selectable input ranges. An integrated voltage reference reduces design considerations.
At the same time, a temperature diode is integrated on the chip, which can be used for system thermal management and detect the heating condition of the main chip on the board.

Based on subclass 1-JESD204B of high-speed serial output data lanes , it can be configured as single-lane (L=1), dual-lane (L=2), quad-lane (L=4), and octal-lane (L=8) configurations, depending on the sampling rate and decimation rate. Multi-device synchronization can be achieved through the SYSREF ± and SYNCINB ± input pins. The SYSREF ± pin of the CW9689 can also be used as a timestamp for data as it passes through the ADC and out of the JESD204B interface.

7. Typical performance

surface 1. Chip usage conditions

parameter	symbol	Notes	Numeric	unit
Supply voltage	AVDD1	Analog supply voltage 1	0.975	V
	AVDD3	Analog supply voltage 3	2.5	V
	AVDD1_SR	SYSREF Analog supply voltage	0.975	V
	DVDD	Digital supply voltage	0.975	V
	DRVDD1	SERDES Supply voltage 1	0.975	V
	DRVDD2	SERDES Supply voltage2	1.9	V
	SPIVDD	SPI Supply voltage	1.9	V
Power-on sequence		It is recommended to follow the order of power supply voltage Power on. 0.975V Before 1. 9V before2.5V .		
land	AGND 1	Analog circuit ground	0	V
	AGND 2	Clock domain analog ground	0	V
	AGND 3	Digital and analog isolation	0	V
	DGND	Digital circuit ground	0	V
	DRGND	SERDES Digitally	0	V
Differential input analog signal amplitude		Input signal differential amplitude	1.7	Vpp
Logic input high	V_I		0.8 V_{in}	V
Logic input low	V_{IL}		GND	
Clock differential input signal amplitude	$V_{CLKP} - V_{CLKN}$		800	mVpp
Clock frequency	f_{MCLK}		2.4	GHz
Operating temperature range	T_A		$-55 \le T_A \le 105$	℃

surface 2 Power supply, input electrical characteristics

Unless otherwise stated, AVDD 1 = 0.975 V , AVDD3 = 2.5V , DVDD = 0.97 5V , DRVDD 1 = 0.975V , DRVDD 2 = 1.8V , SPIVDD = 1.8V , f_S = 2.4 GSPS , full scale 1.7 Vp -p input range,-55℃≤TA≤ + 105 ℃ .

parameter	symbol	Minimum	Typical Value (2.4GSPS)	Maximum	unit
Supply voltage:					
Analog supply voltage 1	AVDD1	0.95	0.975	1.0	V
Analog supply voltage 3	AVDD3	2.4	2.5	2.56	V
SYSREF Analog supply	AVDD1_SR	0.95	0.975	1.0	V
voltage Digital supply	DVDD	0.95	0.975	1.0	V
voltage	DRVDD1	0.95	0.975	1.0	V
SERDES Supply voltage 1	DRVDD2	1.8	1.9	2.0	V
SERDES Supply voltage2	SPIVDD	1.8	1.9	2.0	V
SPI Supply voltage					
Supply Current:					
Analog supply current 1	I_{AVDD1}		455	700	mA
Analog supply current 3	I_{AVDD3}		65	75	mA
SYSREF Analog supply	I_{AVDD1_SR}		25	45	mA
current Digital supply	I_{DVDD}		340	830	mA
current	I_{DRVDD1}		320	500	mA
SERDES Supply Current 1	I_{DRVDD2}		25	30	mA
SERDES Supply Current2	I_{SPIVDD}		1	5	mA
SPI Supply Current					
Resolution:			14		Bits
Power consumption :(Full scale)					
Normal operation			1.48	2.4	W
Power - Down model			120	500	mW
Standby mode (stby)			0.9		W
Analog Input:					

Differential input signal amplitude		1100	1700	1880	mVpp
Common mode voltage		1.48	1.5	1.53	V
Differential Input Capacitance			0.35		pF
Differential input resistance			200	213	Ω
Full Power Bandwidth			6		GHz
Clock Input					
Logical compatibility	LVDS/LVPECL				
Clock source type		Differential sine wave			
Differential Input Voltage Swing	$V_{CLKP} - V_{CLKN}$	400	800	1800	mVpp
Clock differential input resistance	R_{MCLK}		106		
External clock jitter requirements	Jitter		100		fs
System Reference Input (SYSREF)					
Logical compatibility	LVDS				
Differential Input Voltage Swing		400	800	1800	mVpp
Common mode voltage			0.675	2	V
Input differential impedance			340		kΩ
Logic input (SDIO , SCLK , CSB , PDWN / STBY , FD_A / GPIO_A0 , FD_B / GPIO_B0 , GPIO_A1 , GPIO _B1)					
Logical compatibility	CMOS				
Logic Low		0		0.85	V
Logic High		1			V
Logic output (SDIO , FD_A , FD_B)					
Logical compatibility	CMOS				
Logic Low				0.45	V
Logic High		SPIVDD − 0.45V			V
Differential Sync Input (SYNCINB +/ SYNCINB -)					
Logical compatibility	LVDS				
Differential Input Voltage Swing		400	800	1800	mVpp
Common mode voltage			0	0	V
Input differential impedance			320		kΩ
Single-ended synchronization input (SYNCINB +)					
Logical compatibility	CMOS				
Logic Low				0.1	V
Logic High		1.7			V
Digital Output (SERDOUTx ±, x = 0 to 7)					
Output common mode voltage			0.49		V
Differential Output Voltage Swing		360	560	770	mVpp
Differential terminal impedance matching			100		Ω

surface 3 Static characteristics

parameter	symbol	Minimum	Typical Value	Maximum	unit
Differential Nonlinearity	DNL	-0.99		1.5	LSB
Integral Nonlinearity	INL	-6		10	LSB

surface4 Dynamic characteristics[1]

Unless otherwise stated, AVDD 1 = 0.975 V , AVDD3 = 2.5V , DVDD = 0.9 75V , DRVDD 1 = 0.975V , DRVDD 2 = 1.8V , SPIVDD = 1.8V , f_S = 2.4 GSPS , full scale 1.7 Vp -p input range,-55℃≤TA≤ + 105 ℃.

parameter	symbol	Minimum	Typical Value	Maximum	unit
f_s =2.4 Gsps， V_{in} = -2 dBFS					
Number of effective digits					
f_{in} = 155 MHz	ENOB		9.42		bits
f_{in} = 750 MHz			9.23		bits
f_{in} = 900 MHz			9.17		bits
f_{in} = 1800 MHz			8.96		bits
f_{in} = 2100 MHz			8.74		bits
f_{in} = 3300 MHz			8.29		bits
Signal-to-Noise Ratio					
fin = 155 MHz	SNR		58.6		dBFS
fin = 750 MHz			57.9		dBFS
fin = 900 MHz			57.36		dBFS
fin = 1800 MHz			56.2		dBFS
fin = 2100 MHz			55		dBFS
fin = 3300 MHz			52.5		dBFS
Total Harmonic Distortion					
fin = 155 MHz	| THD |		75		dBFS
fin = 750 MHz			69		dBFS
fin = 900 MHz			67.4		dBFS
fin = 1800 MHz			64.7		dBFS
fin = 2100 MHz			62.9		dBFS
fin = 3300 MHz			59.2		dBFS
Spurious Free Dynamic Range					
fin = 155 MHz	| SFDR |		73		dBFS
fin = 750 MHz			69.7		dBFS
fin = 900 MHz			69.3		dBFS
fin = 1800 MHz			66.7		dBFS
fin = 2100 MHz			65		dBFS
fin = 3300 MHz			60.2		dBFS
Second Harmonic					
f_{in} = 155 MHz	|2nd Harm|		79.4		dBFS
f_{in} = 750 MHz			70		dBFS
f_{in} = 900 MHz			69.7		dBFS
f_{in} = 1800 MHz			69.4		dBFS
f_{in} = 2100 MHz			65		dBFS
f_{in} = 3300 MHz			60.3		dBFS
Third harmonic					
fin = 155 MHz	| 3rd Harm |		78.6		dBFS
fin = 750 MHz			72.5		dBFS
fin = 900 MHz			71.6		dBFS
fin = 1800 MHz			68.8		dBFS
fin = 2100 MHz			67.4		dBFS
fin = 3300 MHz			65.7		dBFS

1. All test results are based on our test environment. Changes in test conditions may cause certain differences in test results.

surface 5 Timing Specifications

parameter	describe	Minimum	Typical Value	Maximum	unit
CLK + to SYSREF + timing requirements (Figure 5)					
tSU_SR	CLK + to SYSREF + Build Time		-70		ps
t_{H_SR}	CLK + to SYSREF + Keep time		120		ps
SPI Timing requirements (Fig.6)					
DS	Data and SCLK Setup time between rising edges	4			ns
DH	Data and SCLK Hold time between rising edges	2			ns
tCLK	SCLK Time period	40			ns
t_S	CSB and SCLK The build time between	2			ns
t_H	CSB and SCLK Keep time between	2			ns
t_{HIGH}	SCLK Minimum high level time	10			ns
t_{LOW}	SCLK Minimum low level time	10			ns
ACCESS	During read operation SCLK The maximum time delay between the falling edge and the output data		6	10	ns
tDIS_SDIO	Relative to CSB Rising edge, SDIO The pin is switched from output to input . time	10			ns

8. Pin Configuration and Function Description

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	AVDD1	AVDD1	AVDD1_2	AGND	CLK+	CLK-	AGND_1	AVDD1_3	AVDD1	AVDD1_5	NC	NC
B	NC	NC	AVDD1_6	AVDD1	AGND_2	AGND_3	AGND_4	AGND_5	AGND_6	AGND_7	AVDD1	AVDD1_9	NC	NC
C	NC	NC	AVDD1_10	AGND_8	AGND_9	AGND_10	AGND_11	AGND_12	AGND_13	AGND_14	AGND_15	AVDD1_11	NC	NC
D	AVDD3	AGND_16	AGND_17	AGND_18	AGND_19	AGND_20	AGND_21	AGND_22	AGND_23	AGND_24	AGND_25	AGND_26	AGND_27	AVDD3_1
E	VIN-B	AGND_28	AGND_29	AGND_30	AGND_31	AGND2	AVDD1_SR	AGND_32	AGND_33	AGND_34	AGND_35	AGND_36	AGND_37	VIN-A
F	VIN+B	AGND_38	AGND_39	AGND_40	AGND_41	AGND_42	SYSREF+	SYSREF-	AGND_43	AGND_44	AGND_45	AGND_46	AGND_47	VIN+A
G	AVDD3_2	AGND_48	AGND_49	AGND_50	AGND_51	AGND_52	AGND_53	AGND_54	AGND_55	AGND_56	AGND_57	AGND_58	AGND_59	AVDD3_3
H	AGND_60	AGND_61	AGND_62	AGND_63	AGND_64	AGND_65	AGND_66	AGND_67	AGND_68	AUX	AGND_69	AGND_70	AGND_71	AGND_72
J	AGND_73	AGND_74	AGND_75	AGND_76	AGND_77	AGND_78	AGND_79	AGND_80	AGND_81	AGND_82	AGND_83	AGND_84	AGND_85	AGND_86
K	AGND_87	AGND_88	AGND_89	AGND_90	AGND_91	AGND_92	AGND_93	AGND_94	AGND_95	AGND_96	AGND_97	AGND_98	AGND_99	AGND_100
L	DGND	GPIO_B1	SPIVDD	FD_B/GPIO_B0	CSB	SCLK	SDIO	PDWN/STBY	FD_A/GPIO_A0	SPIVDD_1	GPIO_A1	DGND_1	DGND_2	DGND_3
M	DGND_4	DGND_5	DRGND	DRGND_1	DRVDD1	DRVDD1_1	DRVDD1_2	DRVDD1_3	DRGND_2	DRGND_3	DRVDD1_4	DRGND_4	DRVDD2	DVDD
N	DVDD_1	DVDD_2	DRGND_5	SERDOUT7+	SERDOUT6+	SERDOUT5+	SERDOUT4+	SERDOUT3+	SERDOUT2+	SERDOUT1+	SERDOUT0+	DRGND_6	SYNCINB+	DVDD_3
P	DVDD_4	DVDD_5	DRGND_7	SERDOUT7-	SERDOUT6-	SERDOUT5-	SERDOUT4-	SERDOUT3-	SERDOUT2-	SERDOUT1-	SERDOUT0 -	DRGND_8	SYNCINB-	DVDD_6

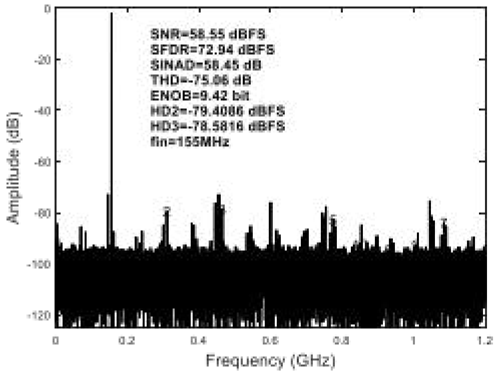
picture 2 CW9689 Pinout

surface6 Pin Function Description

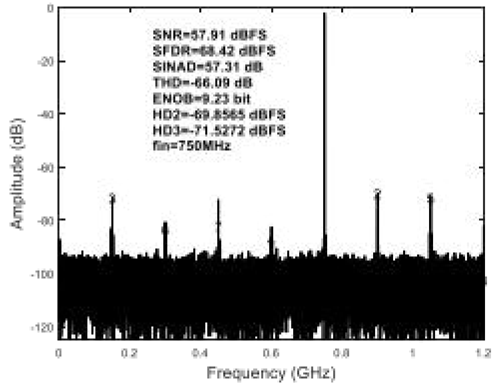
Pin number	name say	achievement able
Power pin		
A3, A12, B3, B12, C 3, C12	AVDD 1	Analog supply voltage1 , default0.975 V
A4, A5, A10, A11, B4, B11	AVDD 1	Clock domain analog power supply voltage, default 0.975V
A1, A2, A13, A14, B1, B2, B13, B14, C1, C2 , C13, C14	NC	The chip cancels this power supply group, and you can choose to leave it floating during design.
D1, D14, G1, G1 4	AVDD 3	Analog supply voltage3 , default2.5V
E7	AVDD_SR	SYSREF ± analog supply voltage, default0.975V
L3, L10	SPIVDD	SPI Digital supply voltage, default 1.9V
M14, N1, N2, N14, P1, P2, P14	DVDD	Digital supply voltage, default0.975V
M5 to M 8, M11	DRVDD 1	SERDES Supply voltage1 , default0.975V
M13	DRVDD 2	SERDES Supply voltage2 , default 1.9 V
B5, B10, C4, C5, C10, C11, D2 to D6, D9 to D13, E2 to E5, E9 to E13, F2 to F6, F9 to F13, G2 to G13, H1 to H9, H11 to H14, J1 to J14	AGND	Analog Ground (Connect to analog ground plane)
A6, A9, B6 to B 9, C6 to C 9, D7, D8	AGND	Analog ground (clock domain)
E6, E8	AGND	Analog Ground (SYSREF ±)
K1 to K 14	AGND	Digital and analog isolation
L1, L12 to L 14, M1, M2	DGND	Digitally
M3, M4, M9, M10, M12, N3, N12, P3, P12	DRGND	SERDES Digitally
Analog Input		
E1 , F1	VIN −B, VIN +B	B channel differential analog input pin
E14, F14	VIN −A, VIN +A	A channel differential analog input pin
A7, A8	CLK +, CLK −	Clock Input
H10	AUX	Temperature diode voltage output
CMOS Input / Output		
L2	GPIO_B1	GPIO_B1
L4	FD _B/ GPIO _B0	B channel amplitude fast detection / GPIO _B0
L9	FD _A/ GPIO _A0	A channel amplitude fast detection / GPIO _A0
L11	GPIO_A1	GPIO_A1
Digital Input		
F7, F8	SYSREF +, SYSREF −	SYSREF System reference signal input pin
N13	SYNCINB+	204B interface synchronization signal input (low effective)
P13	SYNCINB-	204B interface synchronization signal input
Data Output		
N4, P4	SERDOUT 7+ , SERDOUT 7−	aisle7 Data Output
N5, P5	SERDOUT 6+ , SERDOUT 6−	aisle6 Data output
N6, P6	SERDOUT 5+ , SERDOUT 5−	aisle5. Data Output
N7, P7	SERDOUT 4+ , SERDOUT 4−	aisle4 Data output
N8, P8	SERDOUT 3+ , SERDOUT 3−	aisle3. Data Output
N9, P9	SERDOUT 2+ , SERDOUT 2−	aisle2Data output
N10, P10	SERDOUT 1+ , SERDOUT 1−	aisle 1Data output
N11, P11	SERDOUT 0+ , SERDOUT 0−	aisle0 data output
Digital Control		
L5	CSB	SPI CS Signal
L6	SCLK	SPI CLK Signal
L7	SDIO	SPI SDIO Signal
L8	PDWN/STBY	PD signal (high effective) or standby signal , Available throughSPI Configuration

9. Typical performance test curve

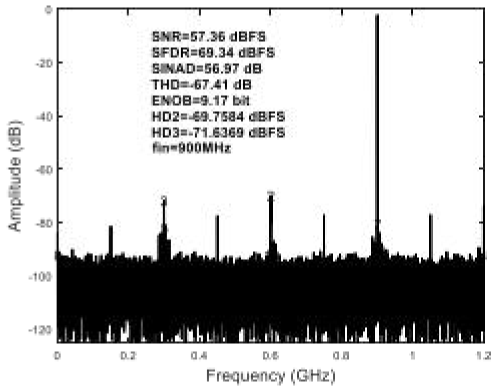
The following performance index curve is the chip working underL=8 , M=2 , F=1 configuration, AVDD 1 = 0.975V , AVDD 3 = 2.5 V , DVDD = 0.975V , DRVDD1 = 0.975V , DRVDD 2 = 1.8V , SPIVDD = 1.8V .AC Coupled signal input,Unused channels are terminated with " AC land " , AC Coupled sine wave sampling clock, f_{CLK} = 2.4 GHz @ 1 V_{PP} (Single-ended signal through 1:2 Balun Convert to differential signal input); Input signal source impedance 50 Ω (Single-ended signal through 1:2 Balun Convert to differential signal input); TA = 25° C .



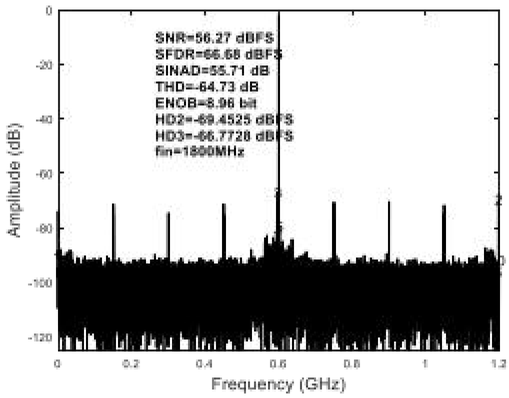
(a) f_{in} =155MHz



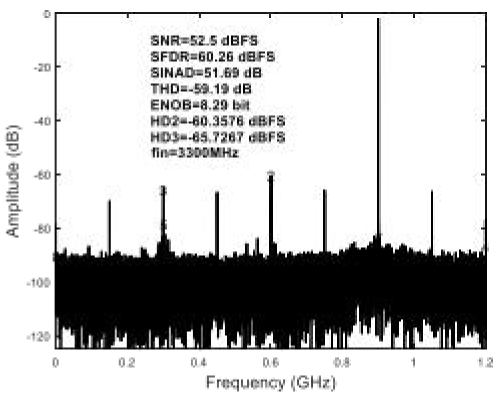
(b) f_{in} = 750MHz



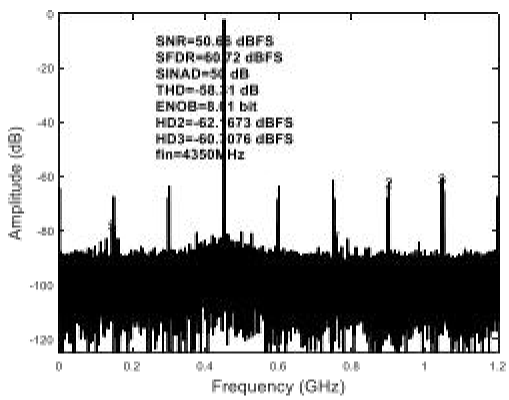
(c) f_{in} = 900MHz



(d) f_{in} = 1800MHz



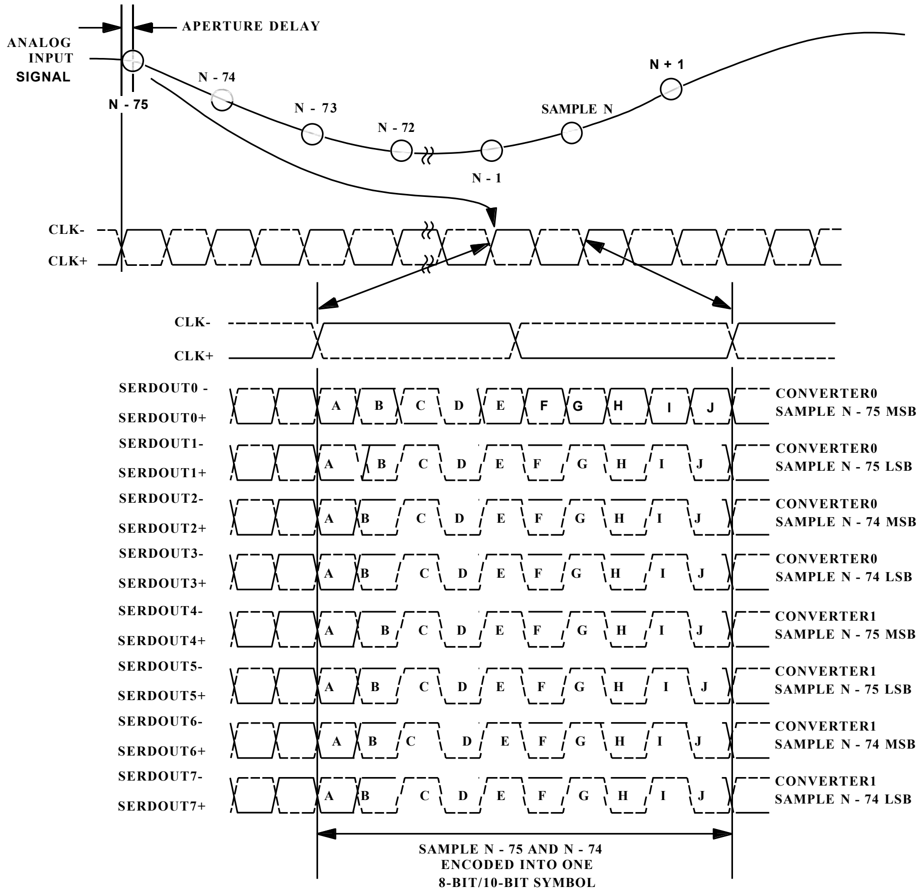
(e) f_{in} =3300MHz



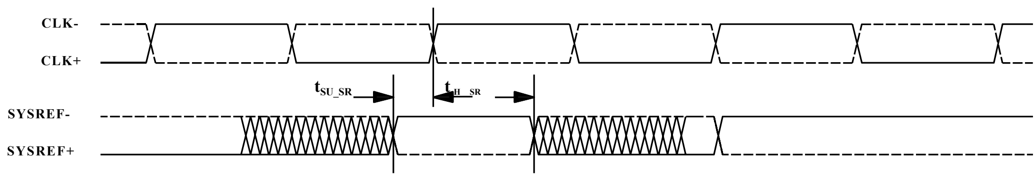
(f) f_{in} =4350MHz

picture3 CW9689 Dynamic characteristics test spectrum (f_s = 2.4 GHz)

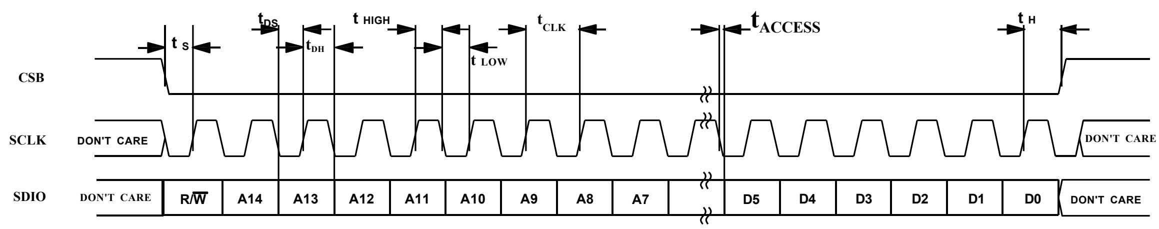
10. Timing diagram



picture4 CW9689 Data output timing diagram



picture5 System synchronization reference signal establishment and maintenance timing diagram



picture6 SPI Interface Timing Diagram

11. ADC Functional Description

11.1 Chip Architecture

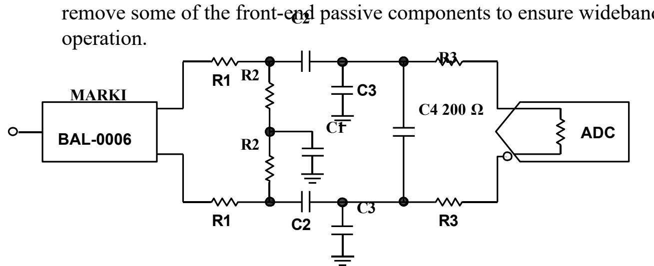
CW9689 includes an input buffer pipeline ADC . The input buffer provides a 200Ω analog input signal terminal impedance. The input buffer is further optimized for linearity, noise, and power consumption over wide bandwidth.
The input buffer provides linear high input impedance (to simplify driving) , The buffer is optimized for high linearity, low noise, and low power consumption. The quantized outputs of each stage are combined to form a final 14- bit conversion result in the digital correction logic. The pipeline architecture allows the first stage to process new input samples while other stages continue to process previous samples.

11.2 Analog input

the CW9689 is a differential buffer. The common-mode voltage inside the buffer is 1.5 V. The clock signal alternately switches the input circuit between sample mode and hold mode.
A differential capacitor or two single-ended capacitors (or a combination of both) can be placed at the input to provide a matched passive network. These capacitors ultimately form a low-pass filter that limits unwanted broadband noise. For best dynamic performance, the source impedance driving VIN+x must be matched to the source impedance driving VIN−x to ensure that the common-mode settling errors are symmetrical. These errors are attenuated by the common-mode rejection of the ADC . In a differential configuration, setting the ADC to its maximum range achieves the best SNR performance, and the CW9689 supports a 1.8 Vpp rail-to-rail input.

11.3 Differential Input Configuration

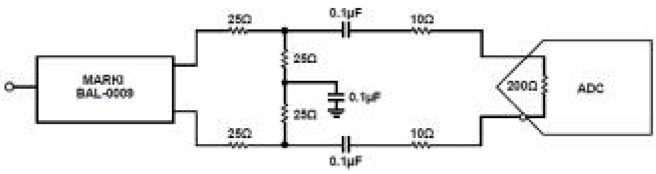
The CW9689 can be driven by a variety of active or passive methods, but the best performance is achieved by driving the analog inputs differentially. In applications where SNR and SFDR are critical parameters , Because the noise performance of most amplifiers is not sufficient to achieve the true performance of the CW9689 , differential transformer coupling is recommended for the input configuration (See Figure 7 and Table 7).
For low to mid frequencies, a dual balun or dual transformer network is recommended to achieve the best performance from the CW9689 .
For higher frequencies in the second or third Nyquist zone, it is best to remove some of the front-end passive components to ensure wideband operation.



picture7 Differential transformer coupling configuration (parameter values see Table 1)

surface7 Differential Transformer Coupled Input Configuration Parameter Values

frequency scope	transformer	R1	R2	R3	C1	C2	C3	C4
<5G Hz	BAL-0006	25Ω	25Ω	10Ω	0.1 uF	0.1 uF	0.4 pF	0.4 pF

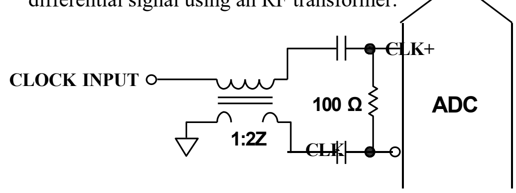


picture8 Input frequency > 5 GHz Input coupling configuration

11.4 Clock input configuration

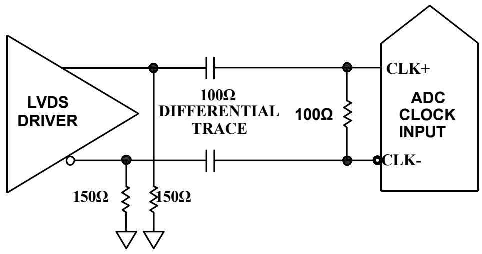
In order to give full play to the performance of the chip , A differential signal should be used as the clock signal for the CW9689 sampling clock inputs (CLK+ and CLK−) . Typically, this signal should be AC-coupled to the CLK+ and CLK− pins using a transformer or clock driver . The CLK+ and CLK− pins are internally biased and do not require additional biasing.

the CW9689 is shown in Figure 9. The single-ended signal from a low-jitter clock source can be converted to a differential signal using an RF transformer.

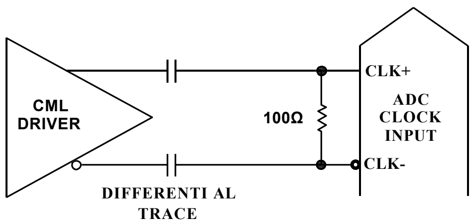


picture9 Transformer coupled differential clock

Another option is to AC-couple the differential CML or LVPECL signals to the same clock input pins. As shown in Figures 10 and 11 .



picture 10 DifferenceLVPECL Sampling Clock



picture 11 DifferenceCML Sampling Clock

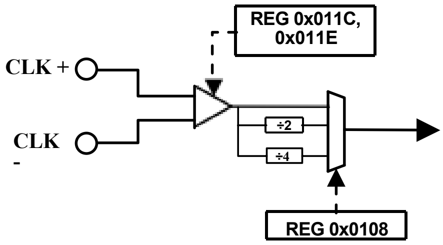
11.5 Clock Duty Cycle

In applications where a 50% clock duty cycle cannot be guaranteed , It is recommended to use a higher multi-frequency clock along with a clock divider. Figure 12 shows the different controls for the CW9689 clock input. The output of the divider provides a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC .

11.6 Input clock divider

CW9689 has a built-in input clock divider that can divide the Nyquist input clock by 1 , 2 , or 4. The division ratio can be selected by register 0x0108 , as shown in the figure below: " Clock Divider Circuit " .

In applications where the clock input is a multiple of the sampling clock, care must be taken to set the clock divider ratio and then add the clock signal to ensure that current transients during device startup are controlled.



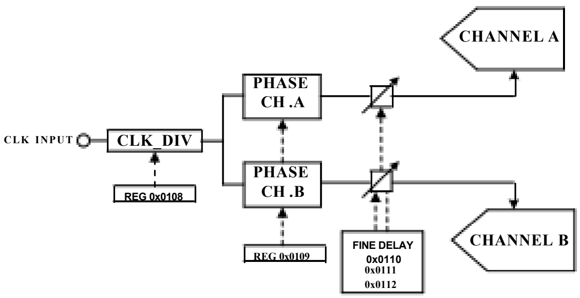
picture 12 Clock frequency division circuit

Using an external SYSREF ± input signal, The CW9689 clock dividers can be synchronized . An active SYSREF ± signal resets the clock dividers to a programmable state. This synchronization feature allows the clock dividers of multiple devices to be aligned to ensure synchronous input sampling. For more information, see the Register Map Table section.

11.7 Clock accuracy delay adjustment

The CW9689 sampling edge instant can be adjusted by writing registers 0x0110 , 0x0111 , and 0x0112 . Bits [2:0] of register 0x0110 can set the delay to select fine delay or super fine delay. Fine delay allows the user to delay the clock edge using 16- step or 192- step delay options. Super fine delay is an unsigned control that adjusts the clock delay in super fine steps of 0.25ps .
[7:0] of register 0x0112 provide the user with 192 delay steps for clock delay selection. Bits [7:0] of register 0x0111 provide the user with 128 ultra-fine delay steps for clock delay selection. These values can be set individually for each channel.

If you want to use ultra-fine delay, set the clock delay of bits [2:0] in register 0x0110 to Figure 13 shows the controls available for the clock divider in CW9689 when the time control is set to 0x2 or 0x6 . It is recommended to apply the same delay setting to both the digital delay circuit and the analog delay circuit to maintain channel sampling accuracy.



picture 13 Clock Divider Phase and Delay Control

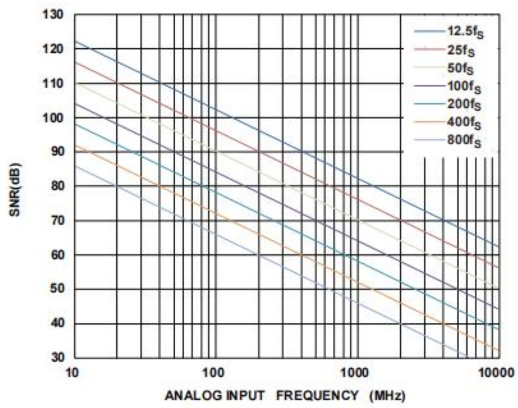
Enabling clock delay adjustment via SPI write takes effect immediately. Enabling clock accuracy delay adjustment in register 0x0110 can reset the data path. Note that changing the values of registers 0x0111 and 0x0112 will not affect the stability of the JESD204B link.

11.8 Clock Jitter Recommendations

High-speed, high-resolution ADCs are very sensitive to the quality of the clock input signal. At a given input frequency (fIN), the degradation of the signal-to-noise ratio (SNR) caused by aperture jitter (tJ) alone is given by:

$$SNR_{JITTER} = -20 \times \log_{10}(2 \times \pi \times f_{IN} \times t_J)$$

In the formula, the rms aperture jitter represents all jitter sources (including the clock input signal, Analog input signal andADC The rms of aperture jitter) . Movement is particularly sensitive (see Figure 1 4) .



picture 14 Relationship between ideal signal-to-noise ratio and input frequency and jitter

When aperture jitter may affect CW9689 The clock input signal should be treated as an analog signal when the dynamic range of the clock driver is limited . The output driver power supply is separated to avoid digital noise being mixed into the clock signal . If the clock signal comes from another type of clock source (through gating, frequency division or other methods) , it needs to be retimed with the original clock in the last step.

11.9 Shutdown / Standby Mode

CW9689 Can bePDWN_STBY The pin is configured for power-down or standby mode. By default, the pin is logic high. In power-down mode, the JESD 204B link is interrupted. You can also use register0x003F and0x0040 to set the power-down mode.

In standby mode, the JESD 204B link is not interrupted and all converter samples are transmitted.0 . Can be registered0x0571 , bit7. SelectK character to change the transmitted value.

11.10 Temperature diode

CW9689 A diode-based temperature sensor is built in to measure the chip temperature. This function is provided by H10 This diode can output a voltage to AUX and act as a general temperature sensor to monitor the internal chip temperature.

12. ADC Over range and fast detection

In receiver applications, a reliable mechanism is needed to determine when the converter clamps. The standard overrange bit in the JESD204B output provides limited information about the status of the analog input. Therefore, it is desirable to set a programmable threshold below full scale so that the gain can be reduced before clamping occurs. Also, since the slew rate of the input signal can be very high, the delay time of this function is very critical. However, highly pipelined converters have very large delays. CW9689 has built-in detection circuits that can be used by each channel to monitor the threshold and set the FD_A and FD_B pins.

12.1 ADC overrange

The receiver usually hopes to detect whether the transmitted data is clipped due to over-amplitude. Therefore, CW9689 provides over-amplitude detection and over-threshold fast detection modules for the two ADCs .
an overrange is detected at the input of the ADC , the ADC overrange indicator is set. The overrange indicator can be embedded in the JESD204B link as a control bit (when CS > 0) with the delay of the overrange indicator aligned with the sampling delay.

12.2 Fast threshold detection

As soon as the absolute value of the input signal exceeds the programmable upper threshold, the FD bit is immediately set to 1 (same configuration for both channels). The FD bit is cleared only when the absolute value of the input signal drops below the lower threshold for a period longer than the programmable dwell time . This feature provides hysteresis to prevent the FD bit from toggling too frequently.

The operation of the upper and lower threshold registers and the dwell time register are shown in Figure 15 .
When the input signal amplitude exceeds the value set in the fast detect upper threshold register (registers 0x247 and 0x248), the FD indicator is set. The value of the selected threshold register is compared with the signal amplitude at the ADC output. The fast upper threshold detection has a latency of 28 clock cycles (maximum). The approximate upper threshold amplitude is defined by the following equation:
Upper threshold amplitude (dBFS) = 20 log (threshold amplitude /213)
FD indicator is not cleared until the signal drops below the lower threshold and remains below it for a set dwell time .
The lower threshold is set in the fast detect lower threshold register (registers 0x249 and 0x24A). The value of the 13 -bit fast detect lower threshold register is compared to the signal amplitude at the ADC output. This comparison is controlled by the ADC pipeline delay; the accuracy of the comparison depends on the converter resolution. The lower threshold amplitude is defined by the following equation:
Lower threshold amplitude (dBFS) = 20 log (threshold amplitude /213)
For example, to set the upper threshold of −6 dBFS , 0xFFF should be written to Register 0x247 and Register 0x248 , and to set the lower threshold of −10 dBFS , 0xA1D should be written to Register 0x249 and Register 0x24A . The dwell time can be set from 1 to 65535 sample clock cycles by writing the desired value to the fast detect dwell time registers (Registers 0x24B and 0x24C).

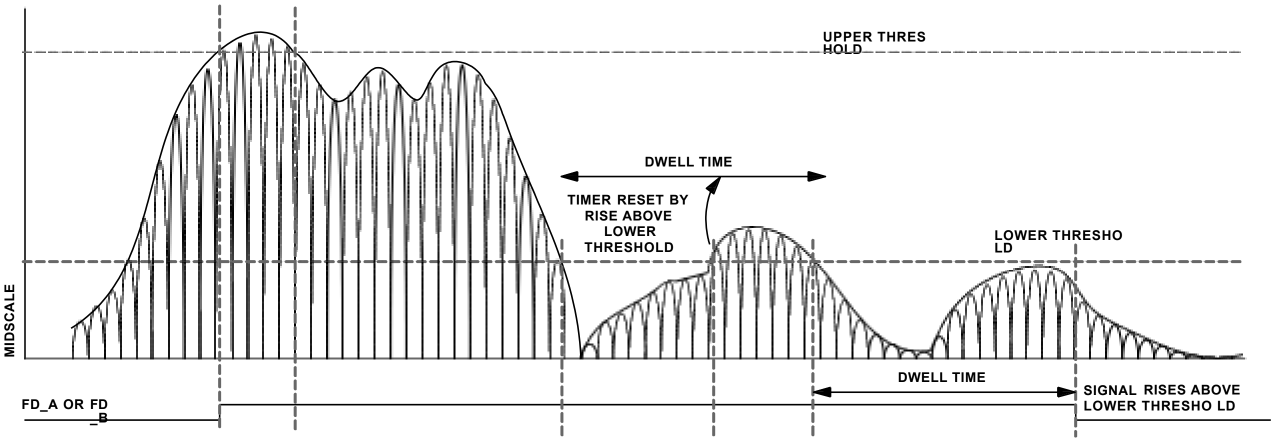


Figure 15 Threshold setting of FD_A and FD_B signals

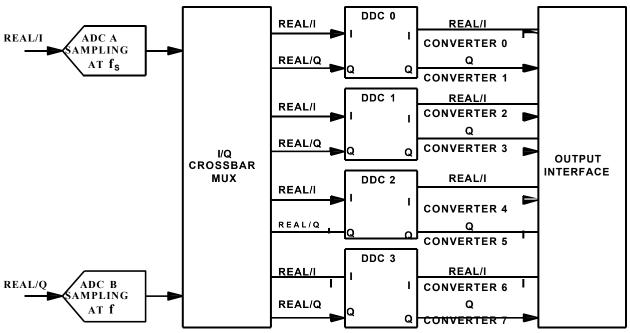
13. ADC Application mode andJESD 204 B Tx Transformation Mapping

The CW9689 contains a configurable signal path that can enable different functions for different applications. These functions are controlled by register 0x0200 . The chip operating mode is controlled by bits [3:0] in register 0x0200 , and the complex Q ignore is controlled by bit 5 .
CW9689 includes the following modes:
Full bandwidth mode: two 14 -bit ADC cores, full sampling rate.
DDC mode: Up to 4 digital down converter (DDC) channels.
After selecting the chip application mode, use the chip decimation rate (bits [3:0]) in register 0x0201 to set the output decimation rate. Output sampling rate = ADC sampling rate / chip decimation rate. In order to support different application layer modes, CW9689 converts each sample stream (real , I , and Q) as separate virtual converters.

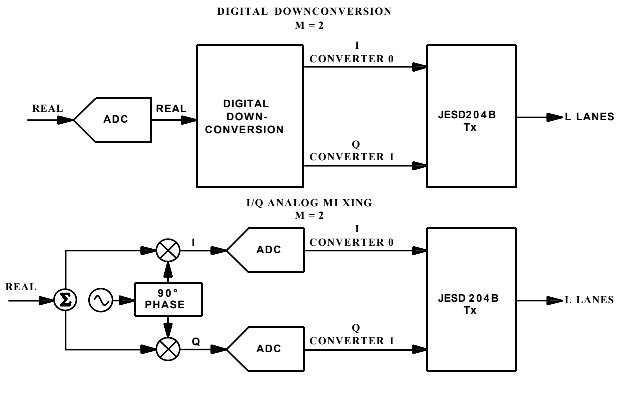
Table 8 shows the number of virtual converters and transport layer mapping required when channel swapping is disabled. Figure 16 shows the relationship between the virtual converters and DDC outputs for complex outputs. Each DDC channel outputs two sample streams (real I/ complex Q), or one sample stream (real I) data. The CW9689 can be configured with up to 8 virtual converters, depending on the DDC configuration. The I/Q samples are always mapped in pairs with the I sample mapped to the first virtual converter and the Q sample mapped to the second virtual converter . With this transport layer mapping, either a single real converter and a digital downconverter that produces an I/Q output are mapped in pairs. Use together, Again analog down-conversion is used with two real converters producing I/Q outputs, the number of virtual converters is the same. Figure 17 shows a block diagram of the two scenarios described for the I/Q transport layer mapping.

surface 8 Virtual converter mapping relationship

Number of Virtual Converters Supported	Chip Operating Mode (Reg. 0x0200, Bits[3:0])	Chip Q Ignore (0x0200, Bit 5)	**Virtual Converter Mapping**							
			0	1	2	3	4	5	6	7
1 to 2	Full bandwidth mode (0x0)	Real or complex (0x0)	ADC A samples	ADC B samples	Unused	Unused	Unused	Unused	Unused	Unused
1	One DDC mode (0x1)	Real (I only) (0x1)	DDC0 I samples	Unused	Unused	Unused	Unused	Unused	Unused	Unused
2	One DDC mode (0x1)	Complex (I/Q) (0x0)	DDC0 I samples	DDC0 Q samples	Unused	Unused	Unused	Unused	Unused	Unused
2	Two DDC mode (0x2)	Real (I only) (0x1)	DDC0 I samples	DDC1 I samples	Unused	Unused	Unused	Unused	Unused	Unused
4	Two DDC mode (0x2)	Complex (I/Q) (0x0)	DDC0 I samples	DDC0 Q samples	DDC1 I samples	DDC1 Q samples	Unused	Unused	Unused	Unused
4	Four DDC mode (0x3)	Real (I only) (0x1)	DDC0 I samples	DDC1 I samples	DDC2 I samples	DDC3 I samples	Unused	Unused	Unused	Unused
8	Four DDC mode (0x3)	Complex (I/Q) (0x0)	DDC0 I samples	DDC0 Q samples	DDC1 I samples	DDC1 Q samples	DDC2 I samples	DDC2 Q samples	DDC3 I samples	DDC3 Q samples



picture 16 DDC and virtual converter mapping



picture 17 I/Q Transport layer mapping

14. Programmable Finite Impulse Response (FIR) Filter

14.1 Supported modes

CW9689 The following operation modes are supported (an asterisk (*) indicates convolution):

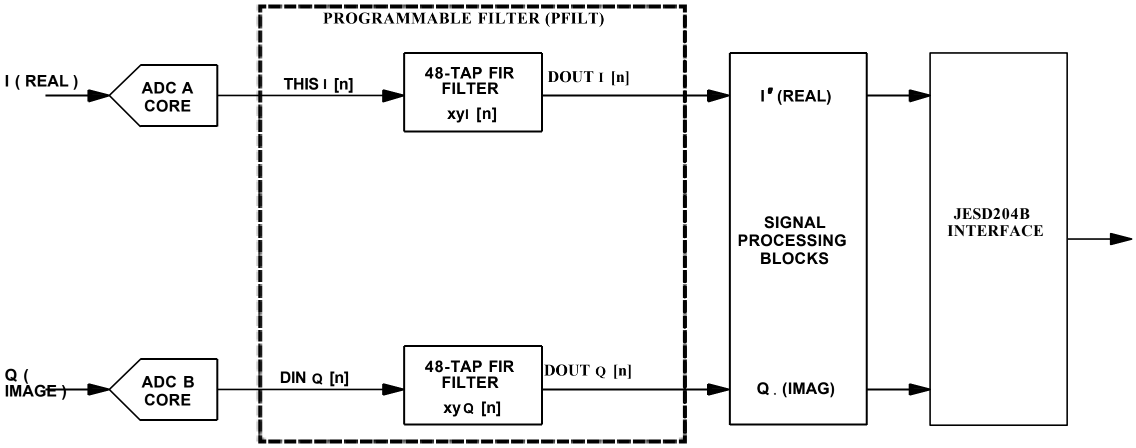
- Each I/Q channels 48 Order real filter (see Figure 18)
  - ✓ DOUT_I [n] = DIN _I[n] * XY _I[n]
  - ✓ DOUT _Q [n] = DIN _Q[n] * XY _Q[n]
- I or Q Channel 96 Order real filter (see Figure 1 9)
  - ✓ DOUT_I [n] = DIN _I[n] * XY _I_ XY _Q[n]
  - ✓ DOUT _Q [n] = DIN _Q[n]
- Each I/Q channel two cascade twenty four Order real filter (see Figure 20)
  - ✓ DOUT_I [n] = DIN_I[n] * X_I[n] * Y_I[n]
  - DOUT_Q [n] = DIN_Q[n] * X_Q[n] * Y_Q[n]

l I /Q channels two 48 Semi- complex filter composed of real filters of order (See Figure 21)

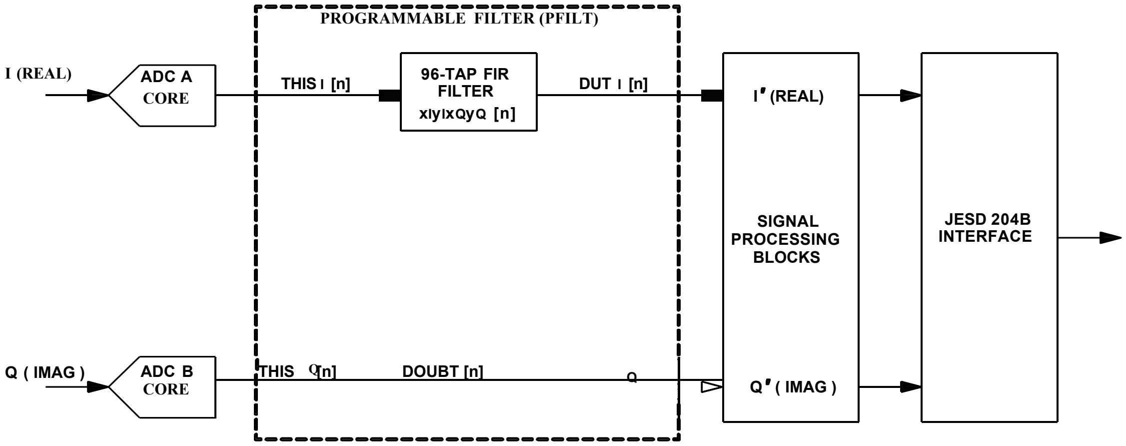
- ✓ DOUT_I [n] = DIN _I[n]
- ✓ DOUT _Q [n] = DIN _Q [n] * XY _Q [n] + DIN _I [n] * XY _I [n]

l Four I /Q channelstwenty four A complex filter composed of real filters of order (see Figure 22)

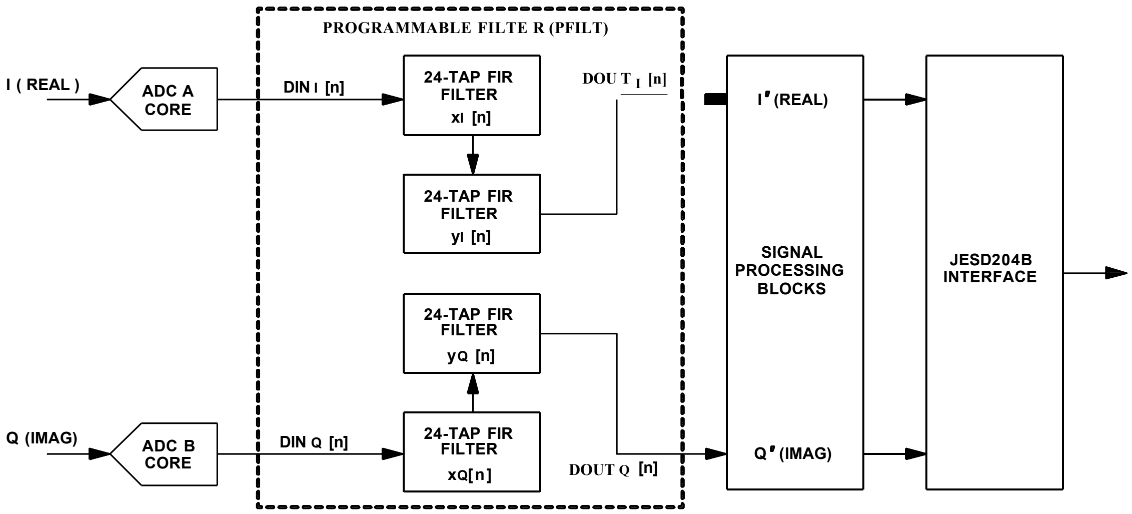
- ✓ DOUT_I [n] = DIN_I [n] * X_I [n] + DIN_Q [n] * Y_Q [n]
- ✓ DOUT_Q [n] = DIN_Q [n] * X_Q [n] + DIN_I [n] * Y_I [n]



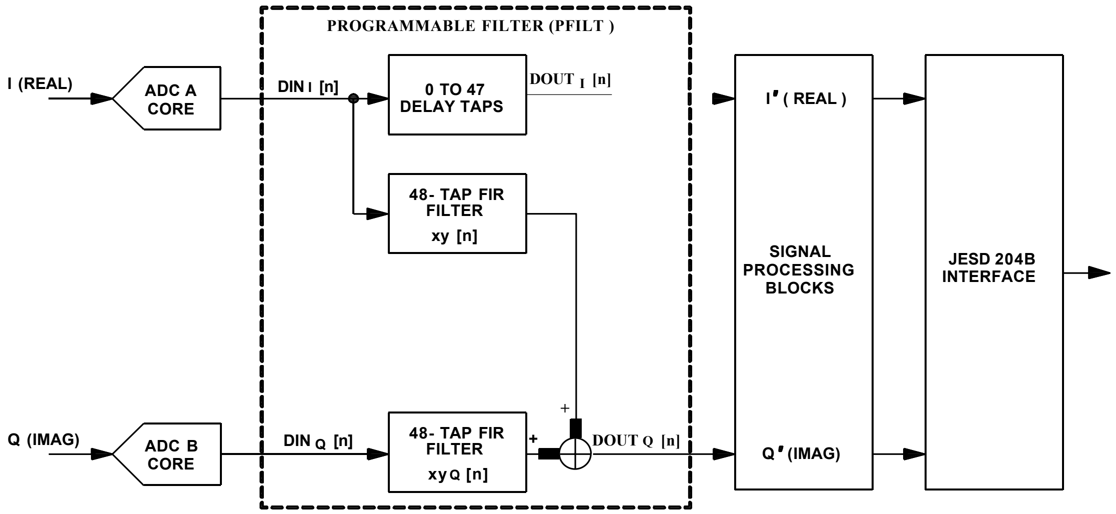
picture 18 48 Order real filter configuration



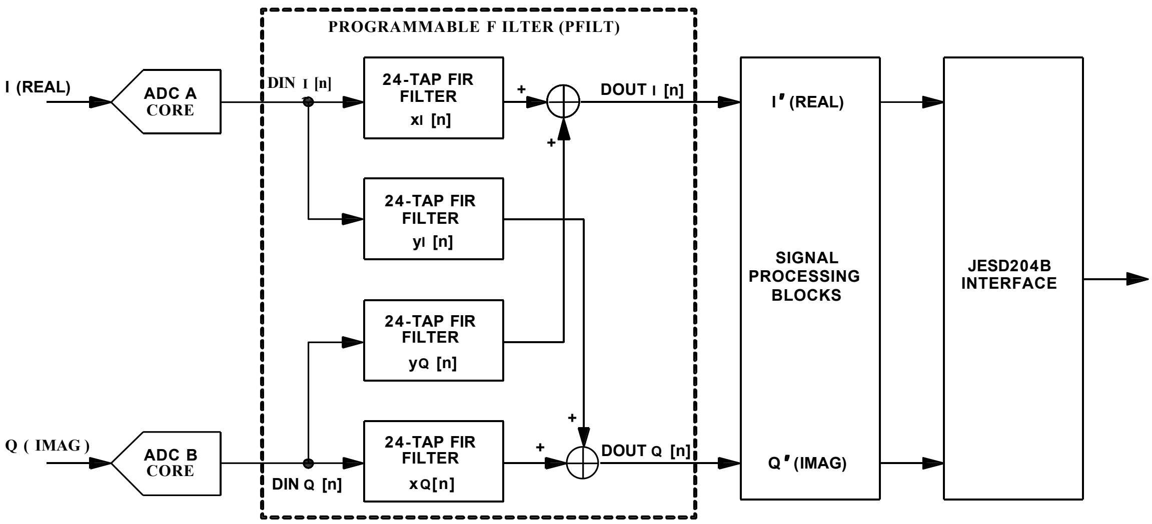
picture 19 96 Order real filter configuration



picture20 24 Cascaded Real Filter Configuration



picture21 24 Order complex filter configuration



picture22 24 Order complex filter configuration

14.2 Programming Instructions

Use the following procedure to set the programmableFIR filter:

1. Enables the sampling clock for the device.
2. The mode register is configured as follows :
   a. Set the device index to channela (I path)(register0x0008 = 0x01).
   b. Setting Registers0x0 DF 8 and register0x0 DF 9 ofI Path Mode (I mode) and gain (see Table 9 and Table 10) .
   c. Set the device index to channelB （ Q Path) (Register 0x0008 = 0x02).
   d. In the " Register0x0 DF 8" and " Register0x0 DF 9" is setQ Pass channel mode (Q -mode) and gain.
3. Wait at least5μs to power up the programmable filter.
4. WillTheI path coefficients are programmed into internal shadow registers as follows:
   a. Set the device index to channela (I path)(register0x0008 = 0x01).
   b. Register0x0F00 InXI Coefficients programmed into registers0x0 E2F (See Table 11 and Table 12).
   c. Register0x0F00 InYI Coefficients programmed into registers0x0F2F (See Table 11 and Table 12).
   d. Programming Registers0x 0F30 The tap delay (note that this step is optional of).
5. WillThe Q path coefficients are programmed into internal shadow registers as follows:
   a. Set the device index to channelB （ Q Path) (Register 0x0008 = 0x02).
   b. Setting Registers 0x0 DF 8 and registers 0x0 DF 9 of Q Path Model formula and gain (see Table 9 and Table 10).
   c. Set the XQ in register 0x0E00 Coefficients programmed into registers 0x0E2F (see Table 11 and Table 12).
   d. Set register 0x0F00 YQ Coefficients programmed into registers 0x0F2F (see Table 11 and Table 12)
   e. Programming register0x0F30 The tap delay (note that this step is optional of).
6. Use one of the following methods to set the chip transfer bit (note that setting the chip transfer bit The input bit will apply the programmed transfer coefficients to the filter):
   a. Set the chip transfer bit through the register map (register0x000F = 0x01).
   b. passGPIO The pinout is as follows:
      i. Connect one of the GPIO Pin configuration is register 0x0040 arrive register0x0042 The chip transfer bit in.
      ii. SwitchGPIO The pin starts chip transfer (rising edge triggered).
7. When the register0x0 DF 8 InI orQ When the path mode register changes, All coefficients must be reprogrammed.
8. The internal shadow register configuration must follow the following rules:
   a. The channel index is configured as0x0 When , all shadow registers will be cleared;
   b. When the channel index is configured as a certain channel, all shadow registers of this channel need to be configured.

surface9 Registers0x0 DF 8 definition

Bit	describe
[7:3]	Reserve
[2:0]	Filter mode (I mode or Q -mode) 000 : Filter bypass 001 : twenty four Order real filter (only X) 010 : 48 order real filter (X and Y together) 100 : Two twenty four Cascaded real filters (X then Y Cascade) 101 : A/B channel four 24 Complex filter composed of real filters of order (The opposite channel must also be set to 101) 110 : Two 48 Order real filter + 48 Semi-complex number composed of delay lines Filters (X and Y together) (the opposite channel must also be set to 010) 111 : 96 order real filters (XI , YI , XQ and YQ Together) (The opposite channel must also be set to 000)

surface 10 register0x0 DF 9 definition

Bit	describe
7	Reserve
[6:4]	Y filter gain 110 : -12 dB loss 111 : -6 dB loss 000 : 0 dB Gain 001 : 6 dB Gain 010 : 12 dB Gain
3	Reserve
[2:0]	X filter gain Y filter gain 110 : -12 dB loss 111 : -6 dB loss 000 : 0 dB Gain 001 : 6 dB Gain 010 : 12 dB Gain

Table 11 and Table 12 show the register0x0E00 to register 0x0F30 In Coefficient table. All coefficients areQ1.15 format (1 sign bit + 15 decimal places).

surface 11 I coefficient table (device selection = 0x 1) [1]

Addr.	Single 24-Tap Filter (IM ode [2:0] = 0x1)	Single 48-Tap Filter (I Mode [2:0] = 0x2)	Two Cascaded 24-Tap Filters (I Mode [2:0] = 0x4)	Full Complex 24-Tap Filters (I Mode [2:0] = 0x5 and Q Mode [2:0] = 0x5)	Half Complex 48-Tap Filters (I Mode [2:0] = 0x6 and Q Mode [2:0] = 0x2)[2]	I Path 96-Tap Filter (I Mode[2:0] = 0x7 and Q Mode [2:0] = 0x0)[3]	Q Path 96-Tap Filter (I Mode [2:0] = 0x0 and Q Mode [2:0] = 0x7)[3]
0x0E00	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]	XQ C48 [7:0]
0x0E01	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]	XQ C48 [15:8]
0x0E02	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]	XQ C49 [7:0]
0x0E03	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]	XQ C49 [15:8]
…	…	…	…	…	…	…	…
0x0E2E	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]	XQ C71 [7:0]
0x0E2F	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]	XQ C71 [15:0]
0x0F00	Unused	DO C24 [7:0]	DO C0 [7:0]	DO C0 [7:0]	DO C24 [7:0]	DO C24 [7:0]	YQ C72 [7:0]
0x0F01	Unused	DO C24 [15:8]	DO C0 [15:8]	DO C0 [15:8]	DO C24 [15:8]	THIS C24 [15:8]	YQ C72 [15:8]
0x0F02	Unused	THIS C25 [7:0]	THIS C1 [7:0]	THIS C1 [7:0]	THIS C25 [7:0]	THIS C25 [7:0]	YQ C73 [7:0]
0x0F03	Unused	THIS C25 [15:8]	THIS C1 [15:8]	THIS C1 [15:8]	THIS C25 [15:8]	THIS C25 [15:8]	YQ C73 [15:8]
…	…	…	…	…	…	…	…
0x0F2E	Unused	THIS C47 [7:0]	THIS C23 [7:0]	THIS C23 [7:0]	THIS C47 [7:0]	THIS C47 [7:0]	YQ C95 [7:0]
0x0F2F	Unused	YI C47 [15:0]	YI C23 [15:0]	YI C23 [15:0]	YI C47 [15:0]	YI C47 [15:0]	YQ C95 [15:0]
0x0F30	Unused	Unused	Unused	Unused	I path tapped delay 0: 0 tapped delay (matches C0 in the filter) 1: 1 tapped delays … 47: 47 tapped delays	Unused	Unused

[1] XI Cn expressI -PathX coefficient n , YI Cn expressI pathY Coefficient n .

[2] whenI channel uses semi-complex 48 In order filter mode,Q route must adopt single 48 Order filter mode.

[3] whenI -way adopts96 When using the filter mode of the order, the Q path must be in bypass mode.

surface 12 Q coefficient table (device selection = 0x2) [1]

Addr.	Single 24-Tap Filter (Q Mode [2:0] = 0x1)	Single 48-Tap Filter (Q Mode [2:0] = 0x2)	Two Cascaded 24-Tap Filters (Q Mode [2:0] = 0x4)	Full Complex 24-Tap Filters (Q Mode [2:0] = 0x5 and Q Mode [2:0] = 0x5)	Half Complex 48-Tap Filters (Q Mode [2:0] = 0x6 and Q Mode [2:0] = 0x2)[2]	I Path 96-Tap Filter (Q Mode[2:0] = 0x7 and Q Mode [2:0] = 0x0)[3]	Q Path 96-Tap Filter (Q Mode [2:0] = 0x0 and Q Mode [2:0] = 0x7)[3]
0x0E00	XQ C0 [7:0]	XQ C0 [7:0]	XQ C0 [7:0]	XQ C0 [7:0]	XQ C0 [7:0]	XI C48 [7:0]	XQ C0 [7:0]
0x0E01	XQ C0 [15:8]	XQ C0 [15:8]	XQ C0 [15:8]	XQ C0 [15:8]	XQ C0 [15:8]	XI C48 [15:8]	XQ C0 [15:8]
0x0E02	XQ C1 [7:0]	XQ C1 [7:0]	XQ C1 [7:0]	XQ C1 [7:0]	XQ C1 [7:0]	XI C49 [7:0]	XQ C1 [7:0]
0x0E03	XQ C1 [15:8]	XQ C1 [15:8]	XQ C1 [15:8]	XQ C1 [15:8]	XQ C1 [15:8]	XI C49 [15:8]	XQ C1 [15:8]
…	…	…	…	…	…	…	…
0x0E2E	XQ C23 [7:0]	XQ C23 [7:0]	XQ C23 [7:0]	XQ C23 [7:0]	XQ C23 [7:0]	XI C71 [7:0]	XQ C23 [7:0]
0x0E2F	XQ C23 [15:0]	XQ C23 [15:0]	XQ C23 [15:0]	XQ C23 [15:0]	XQ C23 [15:0]	XI C71 [15:0]	XQ C23 [15:0]
0x0F00	Unused	YQ C24 [7:0]	YQ C0 [7:0]	YQ C0 [7:0]	YQ C24 [7:0]	THIS C72 [7:0]	YQ C24 [7:0]
0x0F01	Unused	YQ C24 [15:8]	YQ C0 [15:8]	YQ C0 [15:8]	YQ C24 [15:8]	THIS C72 [15:8]	YQ C24 [15:8]
0x0F02	Unused	YQ C25 [7:0]	YQ C1 [7:0]	YQ C1 [7:0]	YQ C25 [7:0]	THIS C73 [7:0]	YQ C25 [7:0]
0x0F03	Unused	YQ C25 [15:8]	YQ C1 [15:8]	YQ C1 [15:8]	YQ C25 [15:8]	THIS C73 [15:8]	YQ C25 [15:8]
…	…	…	…	…	…	…	…
0x0F2E	Unused	YQ C47 [7:0]	YQ C23 [7:0]	YQ C23 [7:0]	YQ C47 [7:0]	YI C95 [7:0]	YQ C47 [7:0]
0x0F2F	Unused	YQ C47 [15:0]	YQ C23 [15:0]	YQ C23 [15:0]	YQ C47 [15:0]	YI C95 [15:0]	YQ C47 [15:0]
0x0F30	Unused	Unused	Unused	Unused	Q path tapped delay 0: 0 tapped delay (matches C0 in the filter) 1: 1 tapped delays … 47: 47 tapped delays	Unused	Unused

[1] XQ Cn expressQ -PathX coefficient n , YQ Cn expressQ -PathY Coefficient n .

[2] whenI channel uses semi-complex 48 In order filter mode,Q route must adopt single 48 Order filter mode.

[3] whenI -way adopts96 When using the filter mode of the order, the Q path must be in bypass mode.

15. Digital Down Conversion (DDC)

The CW9689 includes four digital downconverters (DDC0 to DDC3) that provide filtering and decimation to reduce the output data rate. The digital processing section includes an NCO , multiple decimation FIR filters, a gain stage, and a complex- to- real conversion stage. Each of these processing blocks has control lines that can be individually enabled or disabled to provide the desired processing functionality. The digital downconverter can be configured to output either real or complex data.

The DDC outputs a 16 -bit data stream. To enable this operation, the converter bit count N must be set to 16 , even though the analog core only outputs 14 bits. In full bandwidth operation, the ADC output is 14 data bits plus 2 zeros , unless the control bits are used otherwise.

15.1 DDC I/Q Input Selection

CW9689 has 2 ADC channels and 4 DDC channels . Each DDC channel has two input ports, which can be paired to multiplex through I/Q The DDC supports real or complex inputs. For real signals, both DDC input ports must be Select the same ADC channel (i.e. DDC input port I = ADC channel A , DDC input port Q = ADC channel A). For complex signals, each DDC input port The DDC input ports must select different ADCs (i.e., DDC input port I = ADC channel A , DDC input port Q = ADC channel B).

Each DDC input is selected by the DDC Input Select Register (Register 0x0311 , Register 0x0331 , Register 0x0351 , and Register 0x0371) control.

15.2 DDC I/Q Output Selection

Each DDC channel has 2 output ports, which can be paired to support real or complex output. For real output signals, only DDC output port I is used (DDC output port Q is invalid) For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

I/Q output of each DDC channel is controlled by the DDC control register (register 0x310 , The DDC complex-to-real enable bit (Bit 3) in Register 0x330 , Register 0x350 , and Register 0x370) controls the DDC complex-to-real conversion.

Q Ignore bit (Bit 5) in the Chip Application Mode Register (Register 0x200) controls the chip output complex for all DDC channels. When all DDC channels use real output, this bit must be set high to ignore all DDC Q output ports. When any DDC channel is set to use complex I/Q output, the user must clear this bit to use both DDC output port I and DDC output port Q.

15.3 DDC Overview

Four DDCs The module is used to extract the Captures a portion of the fully digital spectrum for use in IF-sampled or oversampled baseband radio applications requiring wide bandwidth input signals.

EachDDC The module contains the following signal processing stages :

- ●Frequency conversion stage (optional)
- ●Filtration stage
- ●stage (optional)
- ●Realization conversion phase (optional)

15.3.1. Frequency Conversion Stage (Optional)

The frequency conversion stage consists of a phase-continuous NCO It is composed of a phase-continuous NCO and a quadrature mixer , and can be used for frequency conversion of real or complex input signals. Allows free setting of frequency hopping , which can be based on a single synchronization event. Also included 16 shadow registers are used for fast frequency hopping applications. This stage shifts a portion of the available digital spectrum down to baseband.

15.3.2. Filtering stage

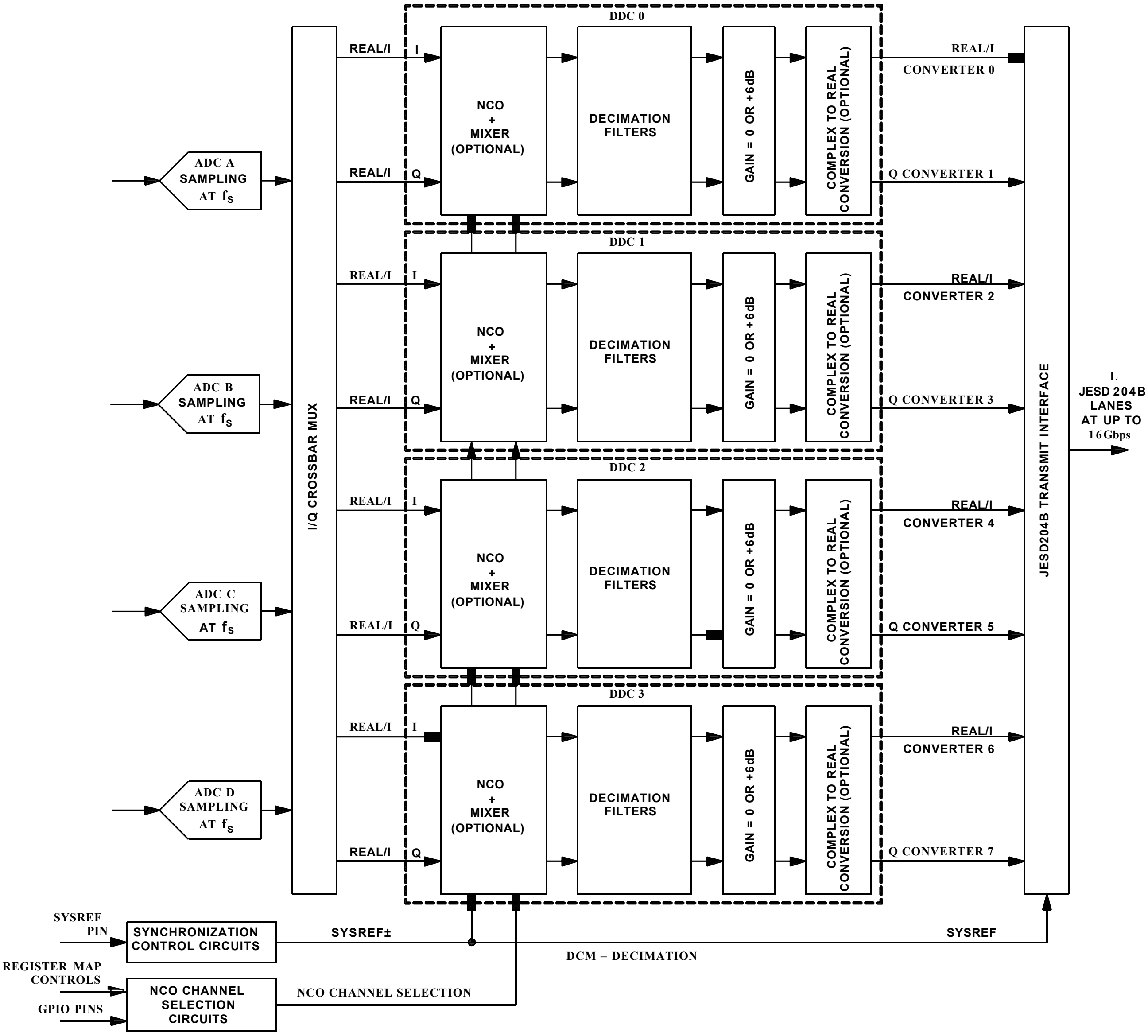
After moving down to baseband, The filtering stage uses multiple low-pass finite impulse response (FIR) filters for rate conversion. The decimation process reduces the output data rate, thereby reducing the output interface rate.

15.3.3. Gain Stage (Optional)

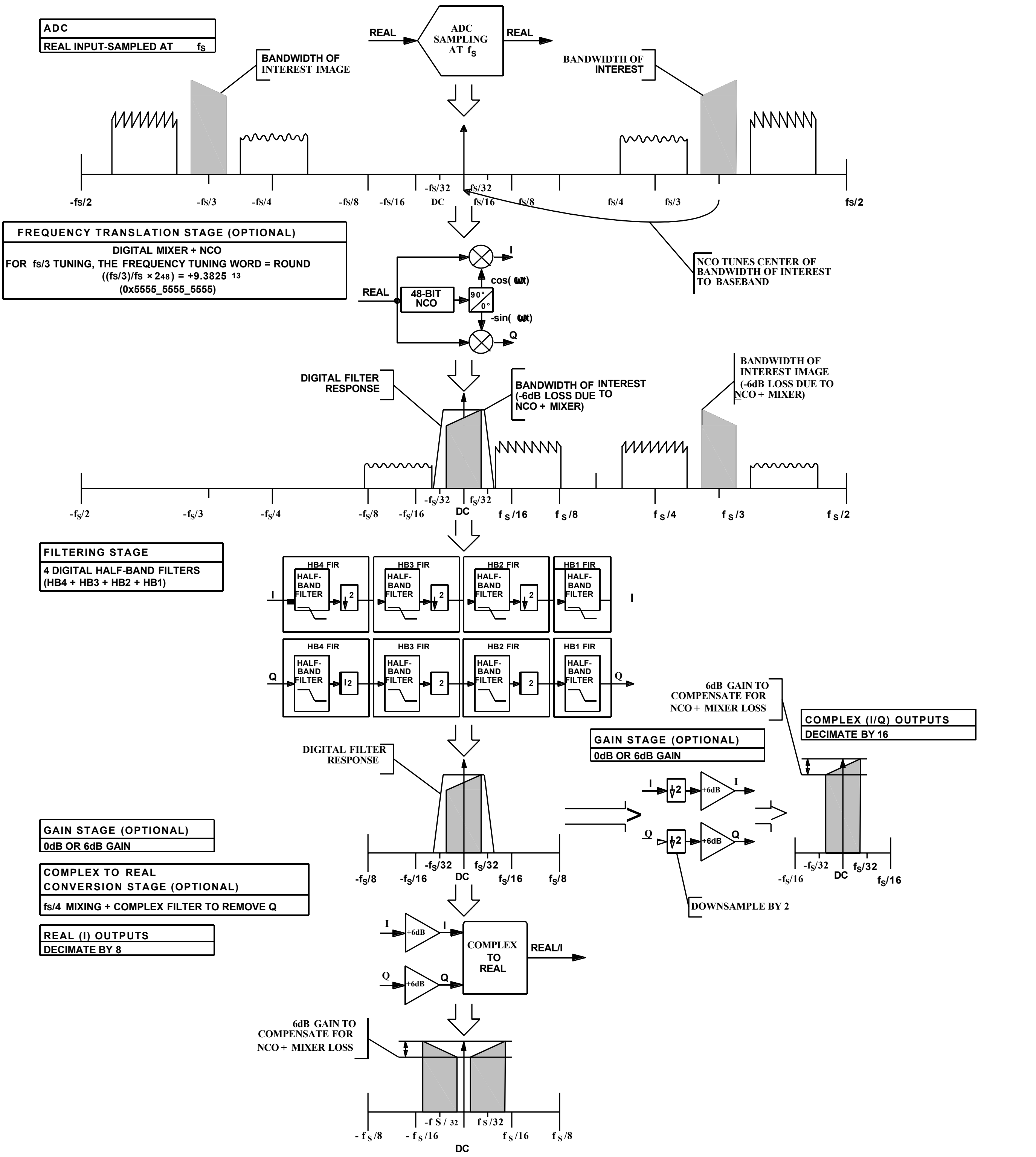
Since mixing a real input signal to baseband is lossy, the gain stage is added by adding an extra0 dB or6 dB The gain is compensated .

15.3.4. Complex to Real Conversion Stage (Optional)

When a real output is required, the complex-to-real conversion stage performs an fS/4 mixing operation and filters out the complex content of the signal, converting the complex output back to a real output. Figure 23 shows a detailed block diagram of the DDC implemented in the CW9689 . Figure 24 shows an example of the use of one of the DDC modules with a real input signal and four half-band filters (HB4 , HB3 , HB2 , and HB1). Both complex (decimation by 16) and real (decimation by 8) output options are shown.



picture23 DDC System Block Diagram



picture24 DDC Working principle example (real number input)

15.4 DDC Frequency Conversion

15.4.1. DDC Frequency Conversion Overview

accomplished using a 48 -bit complex NCO with digital quadrature mixers. Frequency translation converts a real or complex input signal from an intermediate frequency (IF) to a baseband complex digital output (carrier frequency = 0 Hz). Each DDC frequency translation stage can be individually controlled to support four different IF modes, which are selected using Bits [5:4] of the DDC control registers (Register 0x0310 , Register 0x0330 , Register 0x0350 , and Register 0x0370) .
These IF patterns are as follows:

- Variable IF mode
- 0 Hz IF or Zero IF (ZIF) mode
- fS /4 Hz IF Mode
- Test mode

15.4.1.1 . Variable IF Mode

NCO and mixer enable. NCO The output frequency can be used toIF The frequency is digitally modulated.

15.4.1.2 . 0 Hz IF or Zero IF (ZIF) mode

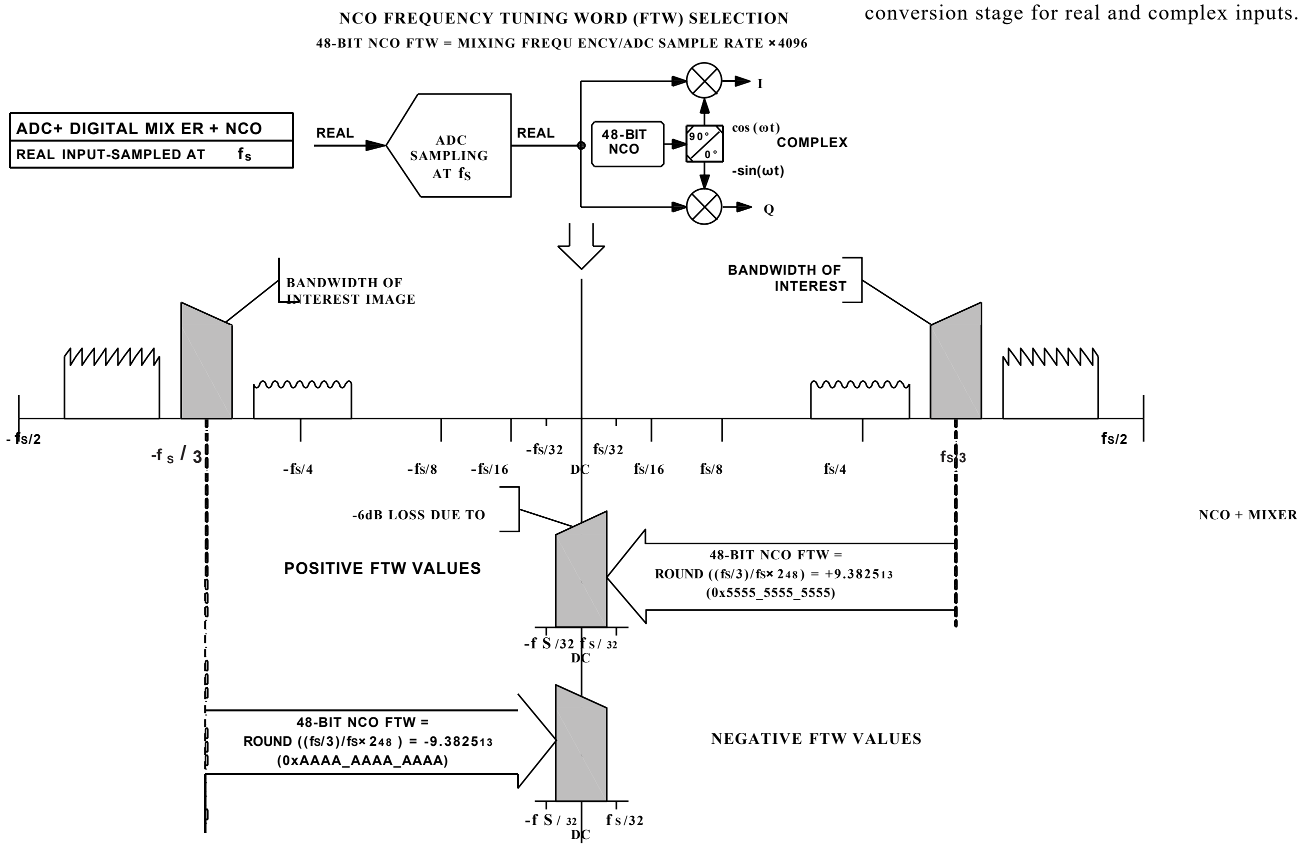
Mixer bypass, NCO Disabled.

15.4.1.3 . f s /4 Hz IF Mode

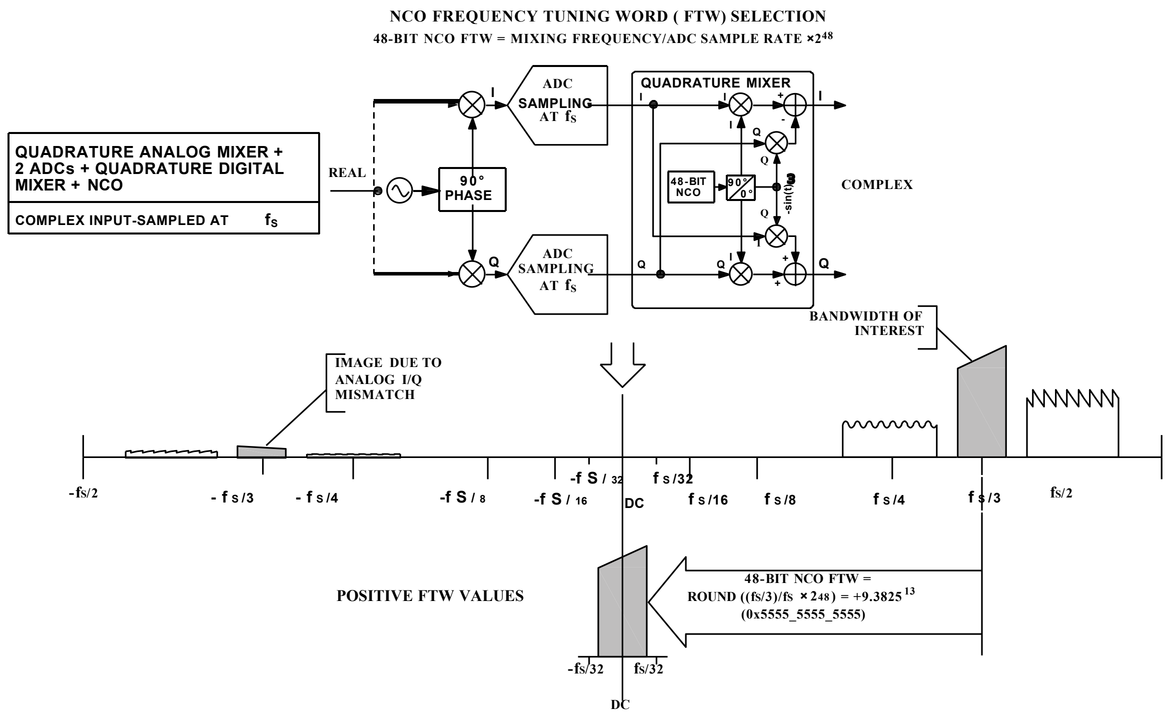
Mixer and NCO Working in special f s /4 down-mixing mode to save device power consumption.

15.4.1.4 Test Mode

Force the input sample to be ADC Full scale 0.999 times, and enable NCO, This test mode allows NCO The output goes directly to the decimation filter. Figure 25 and Figure 26 show shows an example of a frequency conversion stage for real and complex inputs.



picture 25 DDC NCO Frequency tuning word selection – real input



picture 26 DDC NCO Frequency tuning word selection – multiple inputs

15.4.2. DDC NCO Description

Each DDC Contains a NCO . Each NCO By outputting a complex exponential frequency (e−jω ct) to achieve the frequency conversion process, which can be mixed with the input frequency band, The frequency band of interest is moved to the baseband and can be subsequently filtered by a low-pass filter to prevent frequency aliasing.

When in a variableIF Mode,NCO Two different attach modes are supported.

15.4.2.1 . DDC NCO Programmable Mode

This mode supports more than48 -bit frequency tuning accuracy, suitable for applications requiring single carrier frequency synthesis applications. In this mode , the NCO The following scenarios can be set:

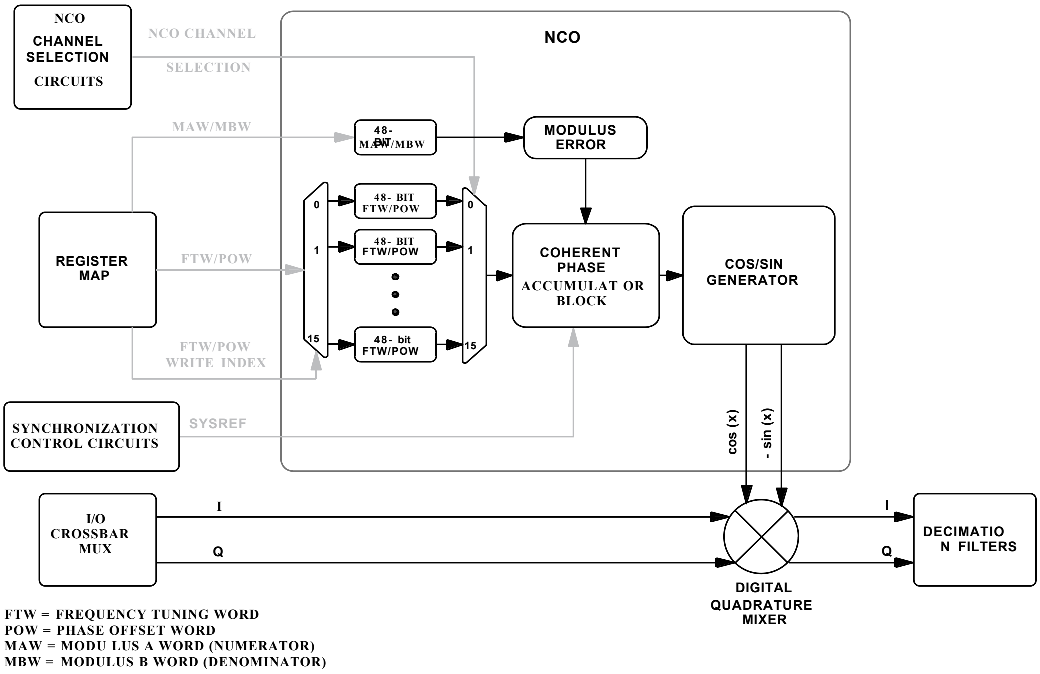
- ●48 -bit frequency tuning word (FTW)
- ● 48 -bit modeA -shaped (MAW)
- ●48 -bit modeB word (MBW)
- ● 48 -bit phase offset word (POW)

15.4.2.2 DDC NCO Phase Continuous Mode

This mode allows free frequency hopping where the phase is referenced to a single synchronization event at time 0. This mode is useful in applications where switching between different frequency bands requires phase continuity. In this mode, the user can switch to any tuned frequency without resetting the NCO . Although only one FTW is required , the NCO contains 16 shadow registers for fast switching applications. The shadow register selection is controlled by a CMOS GPIO pin or a register of the SPI . In this mode, the NCO can be set to the following scenarios:

- ●Max 1648 BitFTW .
- ●Max 1648 BitPOW .
- ●48 bitsMAW Must be set to zero in phase continuous mode .

Figure 27 shows aNCO The Phase Continuous Accumulator block contains the logic to allow free frequency hopping.



picture27 NCO + Mixer Block Diagram

15.4.3. NCO FTW/POW /MAW/MAB Description

The NCO frequency value is determined by the following settings:

- ●In FTW Entered in48 -bit two's complement number
- ●In MAW Entered in48 -bit unsigned number
- ●In MBW Entered in48 -bit unsigned number
- ●Frequencies between − f s/2 and + f s/2 (excludingf s/2) is expressed by the following values:
- ●FTW = 0x8000_0000_0000 andMAW = 0x0000_0000_0000 Indicates frequency - f s /2 .
- ●FTW = 0x0000_0000_0000 , M.A.W. = 0x0000_0000_0000 expressdc (Frequency is0 Hz ） .
- •FTW = 0x7 FFF_FFFF_FFFF andMAW = 0x0000_0000_0000 indicates the frequency is + f s/2 .

15.4.3.1 . NCO FTW / POW / MAW / MAB Programmable Mode

For programmable mode, MAW Must be set to a non-zero value (not equal to 0x0000_0000_0000). Only when the frequency accuracy requirement reaches greater than The mode is only required when the 48 -bit

A reasonable need greater than48 bits An example of frequency generation with high accuracy is: the carrier frequency is the sampling rate 1/3 . When the frequency accuracy is required to be ≤48 bits, the phase continuous mode must be used (see NCO FTW / POW / MAW / MAB phase continuous mode section).

In programmable modulus mode, FTW、 MAW and MBW The following must be met Four equations:

$$\frac{\mathrm{mod}(f_c, f_s)}{f_s} = \frac{M}{N} = \frac{FTW + \frac{MAW}{MBW}}{2^{48}} \qquad (1)$$

$$FTW = \mathrm{floor}\left(2^{48} \frac{\mathrm{mod}(f_c, f_s)}{f_s}\right) \qquad (2)$$

MAW = mod ($2^{48} \times$ M, N) (3)

MBW = N (4)

in:

f_C is the desired carrier frequency.

f_S forADC sampling rate.

M is an integer representing the rational numerator of the frequency ratio.

N is an integer representing the rational denominator of the frequency ratio.

FTW Yes meansNCO FTW of48 Bit two's complement.

MAW Yes meansNCO MAW of48 -bit unsigned number (must be less than 247).

MBW yes48 -bit unsigned number, indicatingNCO ofMBWMod (x) is the modulo function. For example, mod(110,100) = 10 , for negative numbers, mod(-32,10) = -2 . floor (x) is defined as less than or equal to x For example, floor (3.6)= 3 . Mode Equations (1) to (4) are applicable to the aliasing of digital domain signals (i.e., the aliasing introduced when analog signals are digitized).

M andN is the integer that reduces to the lowest term. MAW and MBW is the integer reduced to the lowest term.MAW When set to zero , the programmable modulo logic is automatically disabled.

For example, ADC Sampling frequencyf for2600 MSPS , carrier frequency f_C for1001.5 MHz , then:

$$\frac{\mathrm{mod}(1001.5,\ 2600)}{2600} = \frac{M}{N} = \frac{2003}{5200}$$

$$FTW = \mathrm{floor}\left(2^{48}\frac{\mathrm{mod}(1001.5,\ 2600)}{2600}\right)$$
$$= 0\mathrm{x}629\mathrm{B\_F}68\mathrm{C\_}3590$$
$$MAW = \mathrm{mod}(2^{48} \times 2003{,}5200)$$
$$= 0\mathrm{x}0000\_0000\_0300$$
$$MBW = 0\mathrm{x}0000\_0000\_1450$$

The actual carrier frequency can be calculated as follows:

$$f_{C\_ACTUAL} = \frac{FTW + \frac{MAW}{MBW} \times f_S}{2^{48}}$$

In the above example, the actual carrier frequency f_{C_ACTUAL} for:

$$f_{C\_ACTUAL} = \frac{0\mathrm{x}5590\_\mathrm{C}0\mathrm{AD}\_03\mathrm{D}9 + \frac{0\mathrm{x}0000\_0000\_0300}{0\mathrm{x}0000\_0000\_1450} \times f_S}{2^{48}}$$
$$= 1001.5MHz$$

EachNCO Available48 BitPOW To create multiple chips or a single DDC within a chip Known phase relationship between channels.

In programmable mode, FTW andPOW The register can be updated at any time . While still maintainingNCO However, to ensure thatNCO For normal operation, you must update according to the following process MAW and / orMBW register:

1. Write allDDC ofMAW andMBW register.

2. By SPI VisitDDC Soft reset or by Assertion of the SYSREF ± pins synchronizesNCO .

15.4.3.2 . NCO FTW / POW / MAW / MAB Phase Continuous Mode

For phase continuous mode, the NCO MAW Must be set to0. In this mode , the NCO ofFTW It can be calculated by the following formula:

$$FTW = \mathrm{round}\left(2^{48}\frac{\mathrm{mod}(f_c, f_s)}{f_s}\right)$$

in:

FTW for48 -bit two's complement number, representingNCO of FTW .

f forADC sampling frequency.

f_C is the desired carrier frequency.

Round() is a rounding function. For example,round(3.6) = 4 , and for negative numbers, round (-3.4) = -3 .

Note that the above formula applies to aliasing of digital domain signals (i.e., aliasing introduced when analog signals are digitized) . Must be set to zero to use phase continuous mode. When zero, the programmable module logic is automatically disabled.

For example, ADC Sampling frequencyf for2600 MSPS , carrier frequencyf_C for416.667 MHz , then:

$$NCO_{FTW} = \mathrm{round}\left(2^{48}\frac{\mathrm{mod}(416.667{,}2600)}{2600}\right)$$
$$= 0\mathrm{x}2906\_928\mathrm{F\_A}997$$

The actual carrier frequency can be calculated as follows:

$$f_{C\_ACTUAL} = \frac{FTW \times f_S}{2^{48}}$$

In the above example, the actual carrier frequency f_{C_ACTUAL} for:

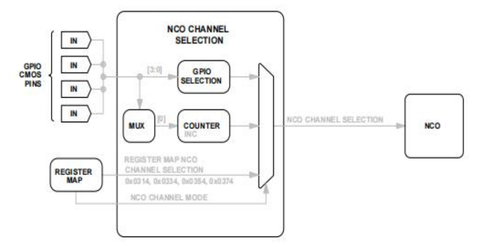
$$f_{C\_ACTUAL} = \frac{416.667 \times 2600}{2^{48}} = 416.66699MHz$$

EachNCO Available48 BitPOW To create a known phase relationship between multiple chips or individual DDC channels within a chip.

In phase continuous mode, FTW andPOW The register can be updated at any time . While still maintainingNCO Deterministic phase results in .

15.4.3.3. NCO Channel Selection

When configured in phase continuous mode, only one FTW is required in the NCO . In this mode, the user can switch to any tuning frequency without resetting the NCO by writing directly to the FTW . However, for fast switching applications, all FTWs are known in advance and or can queue up for the next set of FTWs . The NCO contains 16 additional shadow registers. These shadow registers are referred to as NCO channels below. Figure 28 shows a simplified block diagram of the NCO channel selection module. Only one NCO channel is active at a time, and the NCO channel selection is controlled by a CMOS GPIO pin or through a register. Each NCO channel selector supports three different modes, As described in Figure 28 .



picture28 NCO Channel Selection

15.4.3.4. GPIO level control mode

The GPIO pin determines the exact NCO channel selected .

NCO channel selection using GPIO level :

1. Configure one or more GPIO pins as NCO channel selection inputs. GPIO pins that are not configured as NCO channel selections are pulled low inside the chip.

a) To use GPIO_A0 , write Bits[2:0] in register 0x0040 to 0x6 and Bits[3:0] in register 0x0041 to 0x0 .

b) When using GPIO_B0 , write Bits[5:3] in register 0x0040 to 0x6 and Bits[7:4] in register 0x0041 to 0x0 .

2. Configure the NCO channel selector in GPIO level control mode by setting Bits[7:4] in the NCO control registers (Register 0x0314 , Register 0x0334 , Register 0x0354 , and Register 0x0374) to 0x1 to 0x6 , depending on the desired GPIO pin order.

3. Select the desired NCO channel via the GPIO pin .

15.4.3.5. GPIO edge control mode

a single GPIO pin determines the exact NCO channel selected. The internal channel select counter is reset by SYSREF ± or a DDC soft reset.

NCO channel selection using GPIO edge control :

1. Configure one or more GPIO pins as NCO channel selection inputs.

a) To use GPIO_A0 , write Bits[2:0] in register 0x0040 to 0x6 and Bits[3:0] in register 0x0041 to 0x0 .

b) When using GPIO_B0 , write Bits[5:3] in register 0x0040 to 0x6 , write Bits[7:4] in register 0x0041 to 0x0 .

2. Configure the NCO channel selector in GPIO edge control mode by setting Bits[7:4] in the NCO control registers (Register 0x0314 , Register 0x0334 , Register 0x0354 , and Register 0x0374) to 0x8 to 0xB , depending on the desired GPIO pin.

3. Configure the wrap of the NCO channel selection by setting Bits[3:0] in the NCO control registers (Register 0x0314 , Register 0x0334 , Register 0x0354 , and Register 0x0374) . If set to 4 , wrapping on NCO channel 4 is selected , that is, the NCO channel sequence is 0~4 and then returns to 0 , and so on.

4. Change the selected GPIO pin from low to high to increase the NCO channel selection.

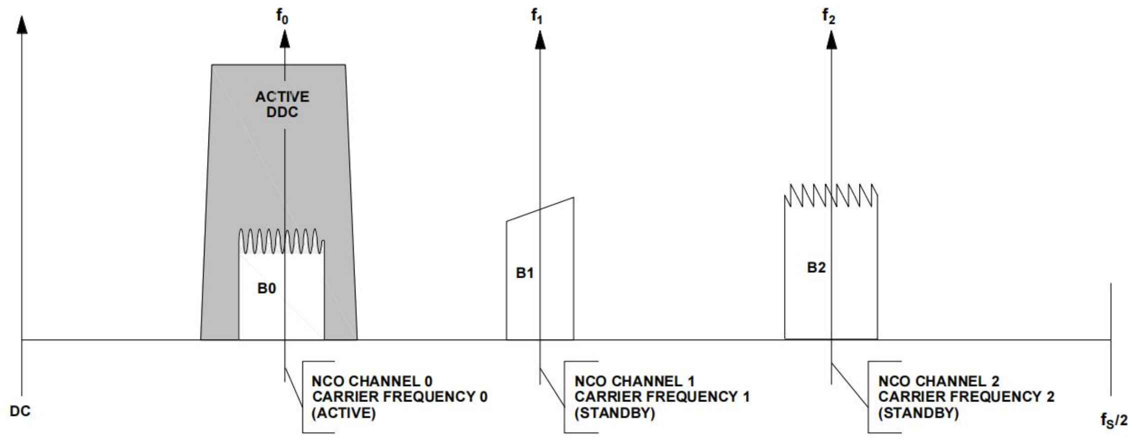
15.4.3.6. GPIO Register Mapping Mode

NCO channel selection is directly controlled through registers.

Figure 29 shows an example of phase continuous mode using three NCO channels. In this example, NCO channel 0 has an active downstream bandwidth of 0 (B0), while NCO channels 1 and Channel 2 is in standby mode, tuned to bandwidth 1 and bandwidth 2 (B1 and B2) respectively.

The phase-continuous feature of NCO switching allows for phase continuity during free frequency hopping. The initial phase of the NCO is established at t0 synchronized with SYSREF ± . Switching the FTW of the NCO does not affect the phase. With this feature, only one FTW is required to achieve seamless switching of NCO output carriers; however, the user may want to use all 16 channels to queue up for the next hop.

SYSREF ± synchronization at startup , All NCOs across multiple chips are inherently synchronized.



picture 29 three NCO Channel NCO Phase Continuous Mode (B0 choose)

15.4.3.7. Setting up multi-channel NCO function

in configuring a multi-channel NCO is to program the FTW . The CW9689 memory map has a FTW index register for each DDC . This index determines which NCO channel receives the FTW from the register map . The order of programming the FTW is shown below.

1. Write the FTW index register with the desired DDC channel.

2. Write FTW with the desired value . This value should be used for the NCO channel index mentioned in step 1 .

3. Settings for other NCO channels, Repeat steps 1 and 2 .

After configuration is complete, the user needs to select the master NCO channel. This selection can be done through the SPI registers or through an external GPIO pin. The following procedure describes how to use Method to select the main NCO channel using SPI .

1. Set the NCO channel selection mode (Bits[7:4]) in register 0x0314 , register 0x0334 , register 0x0354 , and register 0x0374 to 0x0 enables SPI selection .

2. Select the master NCO channel (Bits[3:0]) using registers 0x0314 , 0x0334 , 0x0354 , and 0x0374 .

The following sequence describes how to select the master NCO channel using the GPIO CMOS pins .

1. Set register 0x0314 , register 0x0334 , register 0x0354 and register The NCO channel selection mode (Bits[7:4]) in register 0x0374 is set to a non-zero value to enable GPIO pin selection.
2. Configure the GPIO pins as NCO channel select inputs by writing to Register 0x0040 , Register 0x0041 , and Register 0x0042 .
3. NCO switching is accomplished by externally controlling the GPIO CMOS pin.

15.4.3.8. NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW). The initial value of each PAW is set to zero and incremented at each clock cycle. The instantaneous phase of the NCO is calculated using the PAW , FTW , MAW , MBW , and POW . Due to this architecture, the FTW and POW registers can be updated at any time while still maintaining deterministic phase results in the NCO 's PAW .
PAWs within a chip :

●Use SPI . Use DDC soft reset in DDC synchronization control register bit (register 0x0300 , bit 4) resets all PAWs in the chip . This reset is achieved by setting the DDC soft reset bit high and then This is done by setting OUTPUT_SRC to low. Note that this method can only be used to synchronize DDC channels within the same chip .

●Using the SYSREF ± pins. When the SYSREF ± pins are enabled in the SYSREF control registers (Register 0x0120 and Register 0x0121), And the DDC synchronization control register (register 0x0300 , Bits[1:0]) When DDC synchronization is enabled in the SYSREF± event , any subsequent SYSREF ± event resets all PAWs in the chip . Note that this method can be used to synchronize DDC channels within one chip or DDC channels within different chips .

15.4.3.9. NCO Multi-Chip Synchronization

In some applications, it is necessary to synchronize all NCOs and Local Multi-Frame Clocks (LMFCs). For applications that require multiple NCO tuning frequencies in a system , designers need to generate a single SYSREF ± pulse on all devices simultaneously. For multiple systems, Due to the following factors, Generating or receiving a single SYSREF ± pulse on all devices is challenging:

●Enabling or disabling the SYSREF ± pulse is typically an asynchronous event.

●Not all clock generation chips support this function .

15.4.3.10. Mixer Description

DDC is enabled (0x200 ≠ 0x00), the digital quadrature mixer performs similar operations to the analog quadrature mixer. It performs down-conversion of the input signal (real or complex) by using the NCO frequency as the local oscillator. For real input signals, a real mixer operation (with two multipliers) is performed. For complex input signals, a real mixer operation (with two multipliers) is performed. The input signal is processed by a complex mixer operation (with four multipliers and two adders). The selection of real or complex input for each DDC block can be controlled individually using bit 7 of the DDC control registers (0x0310 , 0x0330 , 0x0350 , and 0x0370) .

15.4.3.11. NCO+ Mixer Losses and SFDR

When the real input signal is mixed to baseband, a −6 dB loss is introduced into the signal due to filtering of the negative image. The NCO adds an additional −0.05 dB loss. The total loss of a real input signal mixed to baseband is −6.05 dB . Therefore, it is recommended that the user This loss is compensated by enabling 6dB of gain in the DDC gain stage, This re-centers the dynamic range of the signal to within the full-scale range of the output bits.

When mixing a complex input signal (where the I and Q DDC inputs come from different ADCs) to baseband, The maximum value that each I/Q sample can reach after passing through the complex mixer is 1.414 times the full scale. In order to avoid the I/Q sampling range being too wide and to keep the data bit width consistent with the real mixer, the complex signal is introduced in the mixer. The NCO adds an additional −0.05 dB loss. The total loss of the complex input signal mixed to baseband is −3.11 dB .

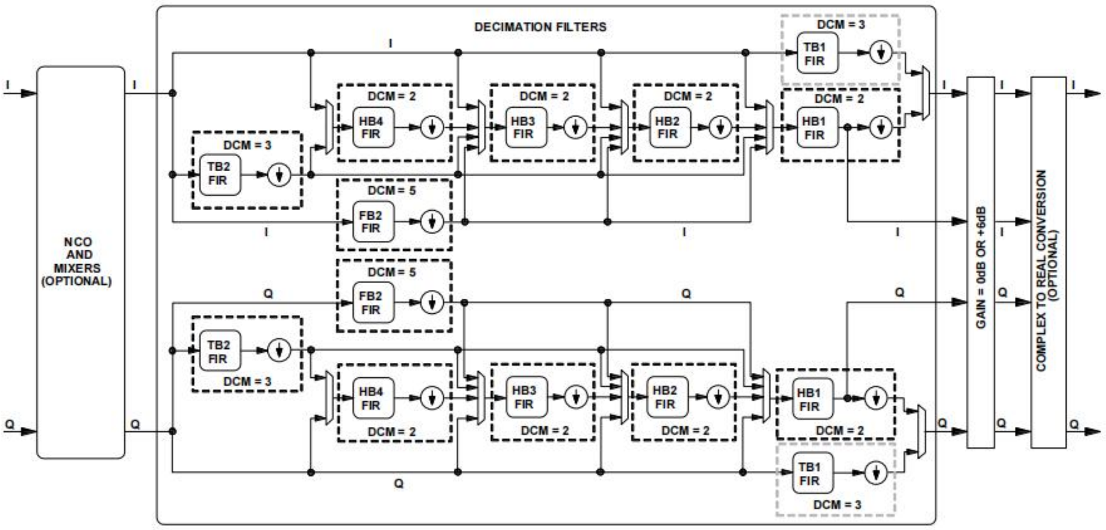
In the worst case, the SFDR of the spurious signals from the NCO is greater than 102 dBc at all output frequencies .

15.5 DDC Decimation Filter

After the frequency conversion stage, there are multiple decimation filter stages to reduce the output data rate.After DC (carrier frequency = 0 Hz), these filters effectively reduce the sample rate while providing sufficient alias rejection to prevent unwanted adjacent carriers around the band of interest from contaminating the signal.

Figure 30 shows a simplified block diagram of the decimation filter stage and Table 1 3 describes the differentFilter characteristics of the FIR filter block.

Table 14 shows the different options after including different half-band filters. In all cases , the DDC The filter stage provides 80% of available output bandwidth,<±0.005 dB The passband ripple and > 100db Stop-band aliasing suppression.



picture 30 DDC Decimation Filter Block Diagram

surface 13 DDC Decimation filter characteristics

Filter Name	Filter Type	Decimation Ratio	Pass Band (rad/sec)	Stop Band (rad/sec)	Pass-Band Ripple (dB)	Stop Band Attenuation (dB)
HB4	FIR low- pass	2	0.1 × π/2	1.9 × π/2	<±0.001	>100
HB3	FIR low- pass	2	0.2 × π/2	1.8 × π/2	<±0.001	>100
HB2	FIR low- pass	2	0.4 × π/2	1.6 × π/2	<±0.001	>100
HB1	FIR low- pass	2	0.8 × π/2	1.2 × π/2	<±0.001	>100
TB2	FIR low- pass	3	0.4 × π/3	1.6 × π/3	<±0.002	>100
TB1[1]	FIR low-pass	3	0.8 × π/3	1.2 × π/3	<±0.005	>100

1 only DDC 0 and DDC 1 support TB 1

surface 14 DDC Filter Configuration[1]

ADC Sample Rate	DDC Filter Configuration	Real (I) Output		Complex (I/Q) Outputs		Alias Protected Bandwidth	Ideal SNR Improvement (dB)[2]
		Decimation Ratio	Sample Rate	Decimation Ratio	Sample Rate		
fs	HB1	1	fs	2	fs/2(I) + fs/2(Q)	fs/2 ×80%	1
fs	TB1[3]	N/A	N/A	3	fs/3(I) + fs/3(Q)	fs/3 ×80%	2.7
fs	HB2 + HB1	2	fs/2	4	fs/4(I) + fs/4(Q)	fs/4 ×80%	4
fs	TB2 + HB1	3	fs/3	6	fs/6(I) + fs/6(Q)	fs/6 ×80%	5.7
fs	HB3 + HB2 + HB1	4	fs/4	8	fs/8(I) + fs/8(Q)	fs/8 ×80%	7
fs	FB2 + HB1	5	fs/5	10	fs/10(I) + fs/10(Q)	fs/10 ×80%	8
fs	TB2 + HB2 + HB1	6	fs/6	12	fs/12(I) + fs/12(Q)	fs/12 ×80%	8.8
fs	FB2 + TB1[3]	N/A	N/A	15	fs/15(I) + fs/15(Q)	fs/15 ×80%	9.7
fs	HB4 + HB3 + HB2 + HB1	8	fs/8	16	fs/16(I) + fs/16(Q)	fs/16 ×80%	10
fs	FB2 + HB2 + HB1	10	fs/10	20	fs/20(I) + fs/20(Q)	fs/20 ×80%	11
fs	TB2 + HB3 + HB2 + HB1	12	fs/12	24	fs/24(I) + fs/24(Q)	fs/24 ×80%	11.8
fs	HB2 + FB2 + TB1[3]	N/A	N/A	30	fs/30(I) + fs/30(Q)	fs/30 ×80%	12.7
fs	FB2 + HB3 + HB2 + HB1	20	fs/20	40	fs/40(I) + fs/40(Q)	fs/40 ×80%	14
fs	TB2 + HB4 + HB3 + HB2 + HB1	24	fs/24	48	fs/48(I) + fs/48(Q)	fs/48 ×80%	14.8

1 N/A means not applicable.

2 Desirable SNR improvement due to oversampling + filtering > 10 log (bandwidth / f s /2) .

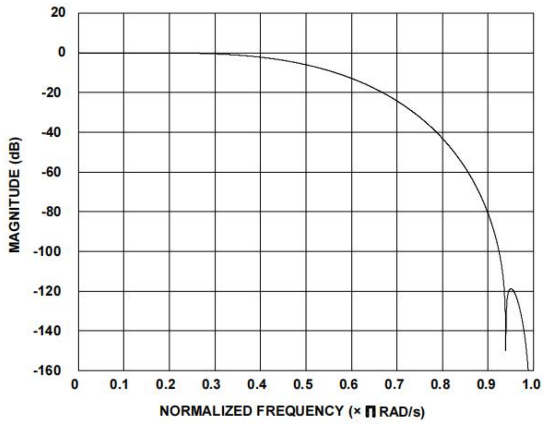
3 only DDC 0 and DDC 1 support TB 1 .

15.5.1. HB4 Filter Description

The first decimate-by -2 , half-band, low-pass FIR filter (HB4) uses an 11- tap, symmetrical, fixed coefficient filter scheme optimized for low power. The HB4 filter is only available on the complex output (decimation by 16) Table 15 and Figure 31 show the coefficients and response of the HB4 filter .

surface 15 HB 4 Filter coefficients

HB4 Coefficient Number	Normalized Coefficient	Decimal Coefficient (15-Bit)
C1, C11	+0.006042	+99
C2, C10	0	0
C3, C9	−0.049377	−809
C4, C8	0	0
C5, C7	+0.293335	+4806
C6	+0.5	+8192



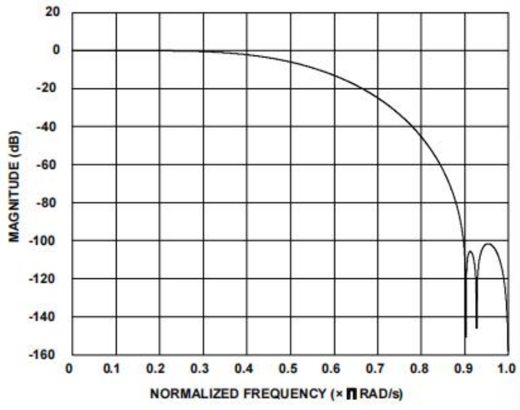
picture 31 HB 4 Filter Response

15.5.2. HB3 Filter Description

The second decimate-by -2 , half-band, low-pass FIR filter (HB3) uses an 11- tap, symmetrical, fixed coefficient filter scheme optimized for low power. The HB3 filter is used only when the complex output (decimation by 8 or 16) or real output (decimation by 4 or 8) is enabled and should be bypassed otherwise. Table 16 and Figure 32 show the coefficients and response of the HB3 filter.

surface 16 HB 3 Filter coefficients

HB3 Coefficient Number	Normalized Coefficient	Decimal Coefficient (17-Bit)
C1, C11	+0.006638	+435
C2, C10	0	0
C3, C9	−0.051056	−3346
C4, C8	0	0
C5, C7	+0.294418	+19295
C6	+0.500000	+32768



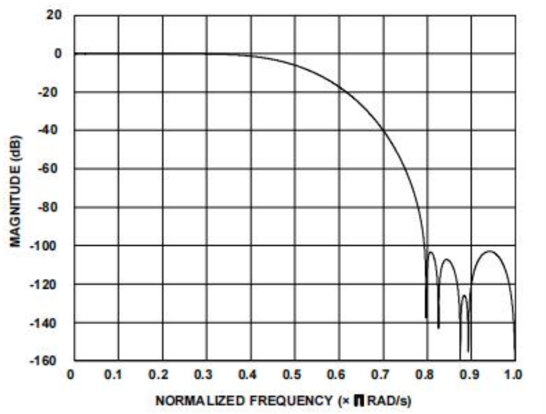
picture 32 HB 3 Filter Response

15.5.3. HB2 Filter Description

The third decimate-by- 2 , half-band, low-pass FIR filter (HB2) uses a 19- tap, symmetrical, fixed coefficient filter scheme optimized for low power.
HB2 filter is used only when complex output or real output (4x , 8x , or 16x decimation) is enabled and should be bypassed otherwise. Table 17 and Figure 33 show the coefficients and response of the HB2 filter.

surface 17 HB 2 Filter coefficients

HB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (18-Bit)
C1, C19	+0.000671	+88
C2, C18	0	0
C3, C17	−0.005325	−698
C4, C16	0	0
C5, C15	+0.022743	+2981
C6, C14	0	0
C7, C13	−0.074181	−9723
C8, C12	0	0
C9, C11	+0.306091	+40120
C10	+0.5	+65536



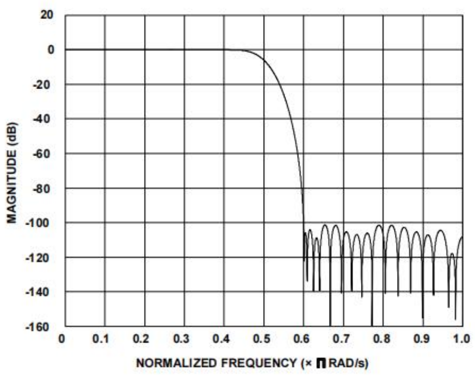
picture 33 HB 2 Filter Response

15.5.4. HB1 Filter Description

The fourth and final decimate-by -2 , half-band, low-pass FIR filter (HB1) Using a 63 -tap, symmetrical, fixed coefficient filter solution, Optimized for low power consumption.
HB1 filter is always enabled and cannot be bypassed. Table 18 and Figure 34 show the coefficients and response of the HB1 filter.

surface 18 HB 1 Filter coefficients

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (20-Bit)
C1, C63	−0.000019	−10
C2, C62	0	0
C3, C61	+0.000072	+38
C4, C60	0	0
C5, C59	−0.000195	−102
C6, C58	0	0
C7, C57	+0.000443	+232
C8, C56	0	0
C9, C55	−0.000891	−467
C10, C54	0	0
C11, C53	+0.001644	+862
C12, C52	0	0
C13, C51	−0.002840	−1489
C14, C50	0	0
C15, C49	+0.004654	+2440
C16, C48	0	0
C17, C47	−0.007311	−3833
C18, C46	0	0
C19, C45	+0.011122	+5831
C20, C44	0	0
C21, C43	-0.016554	-8679
C22, C42	0	0
C23, C41	0.024420	12803
C24, C40	0	0
C25, C39	-0.036404	-19086
C26, C38	0	0
C27, C37	+0.056866	+29814
C28, C36	0	0
C29, C35	-0.101892	-53421
C30, C34	0	0
C31, C33	+0.316883	+166138
C32	+0.5	+262144



picture 34 HB 1 Filter Response

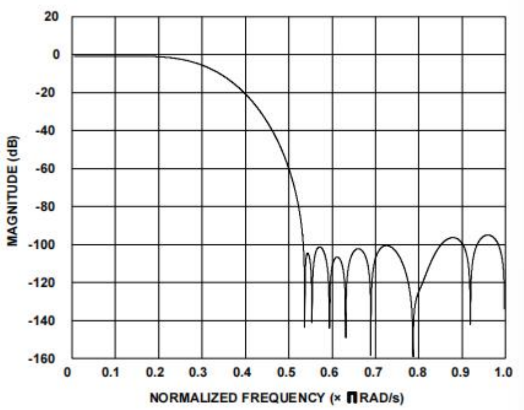
15.5.5. TB2 filter description

TB 2 uses a 26 -tap, symmetrical, fixed coefficient filter solution. Optimized for low power consumption .

TB 2 filters are only used when extraction ratios of6 times, 12 times orUsed at 24 times. Table 19 and Figure 35 are Coefficients and response of the TB 2 filter.

surface 19 TB 2 Filter coefficients

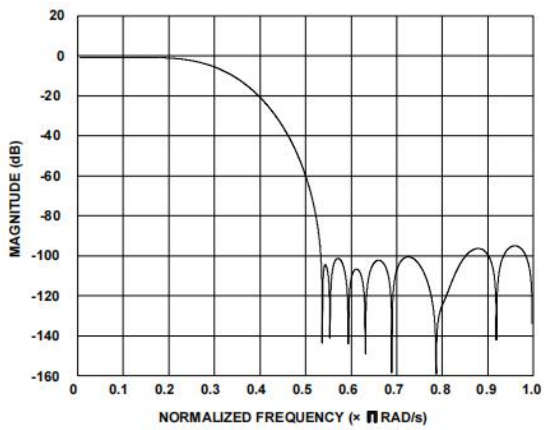
TB2 Coefficiency Number	Normalize d Coefficient	Decimal Coefficient (19 -Bit)
C1, C26	−0.000191	−50
C2, C25	−0.000793	+208
C3, C24	−0.001137	−298
C4, C23	+0.000916	+240
C5, C22	+0.006290	+1649
C6, C21	+0.009823	+2575
C7, C20	+0.000916	+240
C8, C19	−0.023483	−6156
C9, C18	−0.043152	−11312
C10, C17	−0.019318	−5064
C11, C16	+0.071327	+18698
C12, C15	+0.201172	+52736
C13, C14	+0.297756	+78055



picture 35 TB 2 Filter Response

15.5.6. TB1 filter description

TB 1 3x decimate, low pass, FIR The filter adopts a 76 -tap, symmetrical, fixed coefficient filter solution. Table 20 shows TB 1 The filter coefficients, Figure 36 is TB 1 filter response. Note that only DDC 0 and DDC 1 support TB 1 .



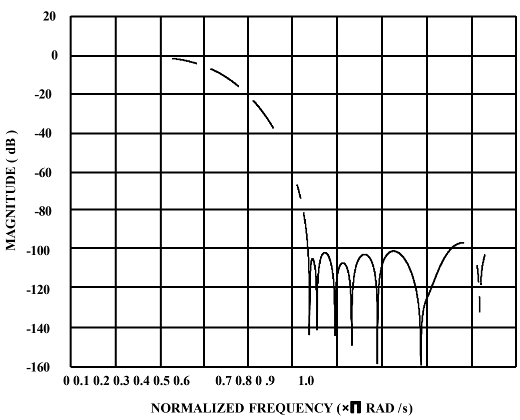
picture 36 TB 1 Filter Response

surface20 TB 1 Filter coefficients

TB1 Coefficiency Number	Normalize d Coefficient	Decimal Coefficient (22-Bit)
1, 76	−0.000023	−96
2, 75	−0.000053	−224
3, 74	−0.000037	−156
4, 73	+0.000090	+379
5, 72	+0.000291	+1220
6, 71	+0.000366	+1534
7, 70	+0.000095	+398
8, 69	−0.000463	−1940
9, 68	−0.000822	−3448
10, 67	−0.000412	−1729
11, 66	+0.000739	+3100
12, 65	+0.001665	+6984
13, 64	+0.001132	+4748
14, 63	−0.000981	−4114
15, 62	−0.002961	−12418
16, 61	−0.002438	−10226
17, 60	+0.001087	+4560
18, 59	+0.004833	+20272
19, 58	+0.004614	+19352
20, 57	−0.000871	−3652
21, 56	−0.007410	−31080
22, 55	−0.008039	−33718
23, 54	+0.000053	+222
24, 53	+0.010874	+45608
25, 52	+0.013313	+55840
26, 51	+0.001817	+7620
27, 50	−0.015579	−65344
28, 49	−0.021590	−90556
29, 48	−0.005603	−23502
30, 47	+0.022451	+94167
31, 46	+0.035774	+150046
32, 45	+0.013541	+56796
33, 44	−0.034655	−145352
34, 43	−0.066549	−279128
35, 42	−0.035213	−147694
36, 41	+0.071220	+298720
37, 40	+0.210777	+884064
38, 39	+0.309200	+1296880

15.5.7. FB2 filter description

FB 2 5x , low pass,FIR The filter adopts 48 taps, symmetrical, fixed coefficients Filter solution. Table 21 is FB 2 The filter coefficients, Figure 37 is FB 2 Filter Response answer.



picture37 FB 2 Filter Response

surface21 FB 2 Filter coefficients

FB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (21-Bit)
1, 48	+0.000007	7
2, 47	−0.000004	−4
3, 46	−0.000069	−72
4, 45	−0.000244	−256
5, 44	−0.000544	−570
6, 43	−0.000870	−912
7, 42	−0.000962	−1009
8, 41	−0.000448	−470
9, 40	+0.000977	+1024
10, 39	+0.003237	+3394
11, 38	+0.005614	+5887
12, 37	+0.006714	+7040
13, 36	+0.004871	+5108
14, 35	−0.001011	−1060
15, 34	−0.010456	−10964
16, 33	−0.020729	−21736
17, 32	−0.026978	−28288
18, 31	−0.023453	−24592
19, 30	−0.005608	−5880
20, 29	+0.027681	+29026
21, 28	+0.072720	+76252
22, 27	+0.121223	+127112
23, 26	+0.162346	+170232
24, 25	+0.185959	+194992

15.6 DDC Gain Stage

Each DDC contains an independently controlled gain stage. Gains of 0 dB or 6 dB can be selected . When mixing a real input signal down to baseband, it is recommended that the user enable 6 dB of gain to re-center the dynamic range of the signal to within the full scale of the output bits. When a complex input signal is mixed down to baseband, the mixer has already recentered the signal's dynamic range to within the full scale of the output bits, and no additional gain is required. However, an optional 6 dB gain can be used to compensate for lower strength signals. When the complex-to-real conversion stage is used, the 2x decimation portion of the HB1 FIR filter is bypassed, and the TB1 filter does not have a 6 dB gain stage.

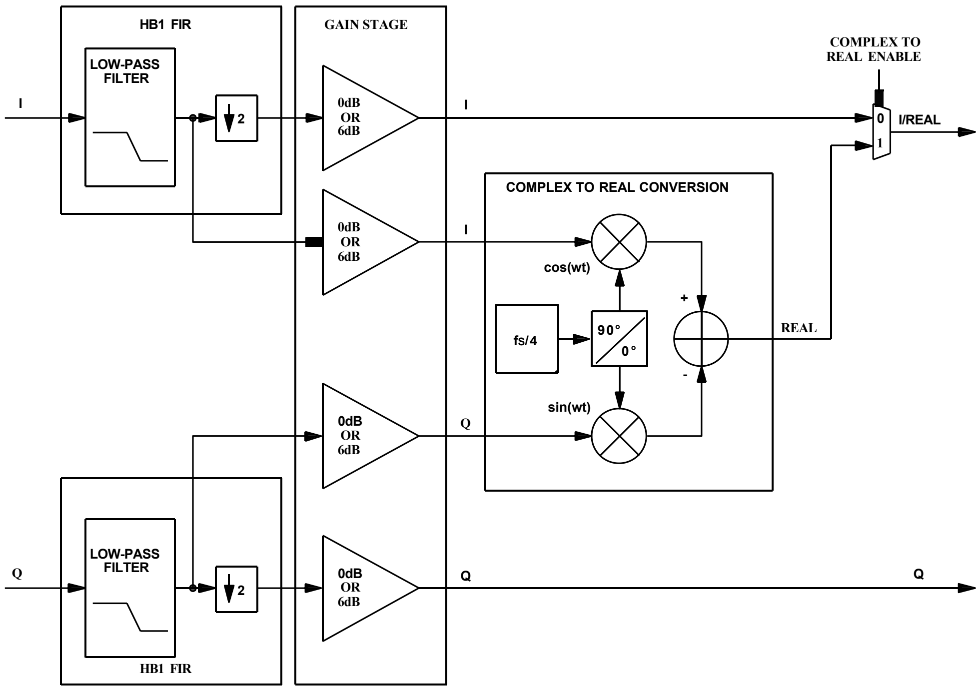
15.7 DDC Complex - Real Conversion

Each DDC contains an independently controlled complex-to-real conversion block. The complex-to-real conversion block reuses the last filter of the filter stage (HB1 FIR) together with an fS/4 complex mixer to up-convert the signal. After the signal is up-converted, The Q section of the complex mixer is no longer required. The TB1 filter does not support complex to real conversion. FIG38 is a schematic block diagram showing the conversion of complex numbers to real numbers.

15.8 DDC Hybrid Decimation Settings

CW9689 also supports DDCs with different decimation rates . In this case, The chip decimation rate must be set to the lowest decimation rate of all DDC channels. Repeat the sampling of high decimation rate DDCs to match the chip decimation sampling rate. Only mixed decimation ratios that are integer multiples of 2 are supported. For example, 1 , 2 , 4 , 8 , 16 can be mixed together, 3 , 6 , 12 , 24 , 48 can be mixed together, and 5 , 10 , 20 , 40 can be mixed together. Table 22 shows the DDC sample mapping when the chip decimation ratio is different from the DDC decimation ratio.

For example, if the chip decimation ratio is set to 4 times decimation, If DDC0 is set to use the HB2 + HB1 filter (complex output, 4x decimation), and DDC1 is set to use the HB4 + HB3 + HB2 + HB1 filter (real output, 8x decimation), then DDC1 repeats its output data twice for each DDC0 output . The resulting output examples are shown in Table 23 .



picture38 Complex to real conversion module block diagram

surface22 chip extraction ratio (DCM) with DDC DCM Sample mapping when there is no match

Sample Index	DDC DCM = Chip DCM	DDC DCM = 2 ×Chip DCM	DDC DCM = 4 ×Chip DCM	DDC DCM = 8 ×Chip DCM
0	N	N	N	N
1	N+ 1	N	N	N
2	N + 2	N+ 1	N	N
3	N+ 3	N+ 1	N	N
4	N + 4	N + 2	N+ 1	N
5	N+ 5	N + 2	N+ 1	N
6	N+ 6	N+ 3	N+ 1	N
7	N+ 7	N+ 3	N+ 1	N
8	N+ 8	N + 4	N + 2	N+ 1
9	N+ 9	N + 4	N + 2	N+ 1
10	N + 10	N+ 5	N + 2	N+ 1
11	N + 11	N+ 5	N + 2	N+ 1
12	N + 12	N+ 6	N+ 3	N+ 1
13	N + 13	N+ 6	N+ 3	N+ 1
14	N + 14	N+ 7	N+ 3	N+ 1
15	N + 15	N+ 7	N+ 3	N + 1
16	N + 16	N + 8	N + 4	N + 2
17	N + 17	N + 8	N + 4	N + 2
18	N + 18	N + 9	N + 4	N + 2
19	N + 19	N + 9	N + 4	N + 2
20	N + 20	N + 10	N + 5	N + 2
21	N + 21	N + 10	N + 5	N + 2
22	N + 22	N + 11	N+ 5	N + 2
23	N+ 23	N + 11	N+ 5	N + 2
24	N+ 24	N + 12	N+ 6	N+ 3
25	N+ 25	N + 12	N + 6	N + 3
26	N + 26	N + 13	N + 6	N + 3
27	N + 27	N + 13	N + 6	N + 3
28	N+ 28	N + 14	N+ 7	N+ 3
29	N+ 29	N + 14	N+ 7	N+ 3
30	N+ 30	N + 15	N+ 7	N+ 3
31	N+ 31	N + 15	N+ 7	N+ 3

surface23 chips DCM = 4 , DDC 0 DCM = 4 (complex), DDC 1 DCM = 8 (real number)[1]

DDC Input Samples	DDC0		DDC1	
	Output Port I	Output Port Q	Output Port I	Output Port Q
N	I0[N]	Q0[N]	I1[N]	Not applicable
N + 1	I0[N]	Q0[N]	I1[N]	Not applicable
N + 2	I0[N]	Q0[N]	I1[N]	Not applicable
N + 3	I0[N]	Q0[N]	I1[N]	Not applicable
N + 4	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 5	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 6	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 7	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 8	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 9	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 10	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 11	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 12	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable
N + 13	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable
N + 14	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable
N + 15	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable

[1] DCM Represents decimation.

15.9 DDC Configuration Example

Table 24 describes multipleDDC Register settings for example configuration . Bandwidths listed are for passband ripple <—0.005 dB and stopband aliasing rejection > 100 dB .

surface24 DDC Configuration Example

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Input Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
One DDC	2	Complex	Complex	40% ×fs	2	0x0200 = 0x01 (one DDC; I/Q selected) 0x0201 = 0x01 (chip decimate by 2) 0x0310 = 0x83 (complex mixer; 0 dB gain; variable IF;complex outputs; HB1 filter) 0x0311 = 0x04 (DDC I Input = ADC Channel A; DDC Qinput = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B,0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 =FTW and POW set as required by application for DDC0
Two DDCs	4	Complex	Complex	20% ×fs	4	0x0200 = 0x02 (two DDCs; I/Q selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x80 (complex mixer; 0 dB gain;variable IF; complex outputs; HB2+HB1 filters) 0x0311, 0x0331 = 0x04 (DDC I input = ADC Channel A;DDC Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B,0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 =FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B,0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 =FTW and POW set as required by application for DDC1
Two DDCs	4	Complex	Real	10% ×fs	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x89 (complex mixer; 0 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) 0x0311, 0x0331 = 0x04 (DDC I Input = ADC Channel A; DDC Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1
Two DDCs	4	Real	Real	10% ×fs	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x49 (real mixer; 6 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x05 (DDC1 I input = ADC Channel B; DDC1 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Input Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
Two DDCs	4	Real	Complex	20% $\times f_S$	4	0x0200 = 0x02 (two DDCs; I/Q selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x40 (real mixer; 6 dB gain; variable IF; complex output; HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x05 (DDC1 I input = ADC Channel B; DDC1 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1
Two DDCs	8	Real	Real	5% $\times f_S$	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x05 (DDC1 I input = ADC Channel B; DDC1 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1
Four DDCs	8	Real	Complex	10% $\times f_S$	8	0x0200 = 0x03 (four DDCs; I/Q selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330, 0x0350, 0x0370 = 0x41 (real mixer; 6 dB gain; variable IF; complex output; HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x00 (DDC1 I input = ADC Channel A; DDC1 Q input = ADC Channel A) 0x0351 = 0x05 (DDC2 I input = ADC Channel B; DDC2 Q input = ADC Channel B) 0x0371 = 0x05 (DDC3 I input = ADC Channel B; DDC3 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = FTW and POW set as required by application for DDC2 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x0380, 0x0381, 0x0382 = FTW and POW set as required by application for DDC3

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Input Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
Four DDCs	8	Real	Real	5% ×fs	4	0x0200 = 0x23 (four DDCs; I only selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330, 0x0350, 0x0370 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x00 (DDC1 I input = ADC Channel A; DDC1 Q input = ADC Channel A) 0x0351 = 0x05 (DDC2 I input = ADC Channel B; DDC2 Q input = ADC Channel B) 0x0371 = 0x05 (DDC3 I input = ADC Channel B; DDC3 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = FTW and POW set as required by application for DDC2 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x0380, 0x0381, 0x0382 = FTW and POW set as required by application for DDC3
Four DDCs	16	Real	Complex	5% ×fs	8	0x0200 = 0x03 (four DDCs; I/Q selected) 0x0201 = 0x04 (chip decimate by 16) 0x0310, 0x0330, 0x0350, 0x0370 = 0x42 (real mixer; 6 dB gain; variable IF; complex output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x00 (DDC1 I input = ADC Channel A; DDC1 Q input = ADC Channel A) 0x0351 = 0x05 (DDC2 I input = ADC Channel B; DDC2 Q input = ADC Channel B) 0x0371 = 0x05 (DDC3 I input = ADC Channel B; DDC3 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = FTW and POW set as required by application for DDC2 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x0380, 0x0381, 0x0382 = FTW and POW set as required by application for DDC3

[1] fs represents the sampling rate of the ADC.

16. signal monitoring

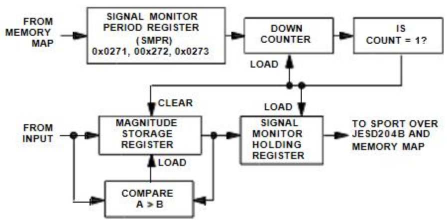
The signal monitoring module provides additional information about the signal digitized by the ADC . The signal monitoring module calculates the peak amplitude of the digitized signal. The same configuration is used for both channels. This information can be used to drive the AGC loop to optimize the signal amplitude to the ADC .

The monitoring results of the signal monitoring module can be read back through the SPI register and can also be integrated into the control bit of JESD204B for real-time transmission. A global, 24 -bit programmable period controls the duration of the measurement. Figure 39 is a simplified block diagram of the signal monitoring module.

The peak detector captures the largest signal during the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is 13 bits and the observation period is 24 bits, which represents the converter output result. The peak magnitude can be derived as follows:

Peak amplitude (dBFS) = 20log(peak detection value $/2^{13}$)

The amplitude of the input port signal is monitored for a programmable period of time determined by the Signal Monitor Period Register (SMPR). The peak detect function is enabled by setting Bit 1 of Register 0x0270 in the Signal Monitor Control Register . Before activating this mode, The 24- bit SMPR must be programmed.



picture39 Signal monitoring module block diagram

When the peak detect mode is enabled, the value in the SMPR is loaded into the monitor cycle timer, which decrements at the sampling clock rate. The configured monitoring period is also in units of sampling clock cycles. The amplitude of the input signal is compared with the value in the internal amplitude storage register (not accessible by the user), and the larger of the two is updated as the current peak level. The initial value of the amplitude storage register is set to the amplitude of the current ADC input signal. This comparison continues until the monitor cycle timer counts to 1 .

When the monitor cycle timer reaches 1 , the 13 -bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT on the JESD204B interface . The monitor cycle timer is reloaded with the value in the SMPR and the countdown begins again. In addition, the amplitude of the first input sample is updated in the amplitude storage register and the comparison and update process continues as previously described.

16.1 Monitoring Results Transmitted via JESD204B

Signal monitoring data can also be serialized and sent as control bits over the JESD204B interface. These control bits must be deserialized from the samples to reconstruct the statistics.

The signal control monitoring feature is enabled by setting Bits [1:0] of Register 0x0279 and Bit 1 of Register 0x027A . Figure 40 shows two different example configurations of the location of the signal monitoring control bits in the JESD204B sample. Up to three control bits can be inserted in the JESD204B sample; However, signal monitoring requires only one control bit.

The control bits are inserted from MSB to LSB . If only one control bit is inserted (CS = 1), only the most significant bit of the control bit is used (see Example Configuration 1 and 2 in Figure 40) . Example Configuration 2). To select the SPORT option for JESD204B , control registers 0x0559 , 0x055A , and 0x058F are required . See the register map table for more information on setting these bits.

Figure 41 shows a 25 -bit data frame for peak detection values. The data frame is transmitted with five 5 - bit subframes MSB first . Each subframe contains a start bit that the receiver can use to verify the deserialized data.

Figure 42 shows the SPORT signal monitor data for JESD204B with the monitor cycle timer set to 80 samples.

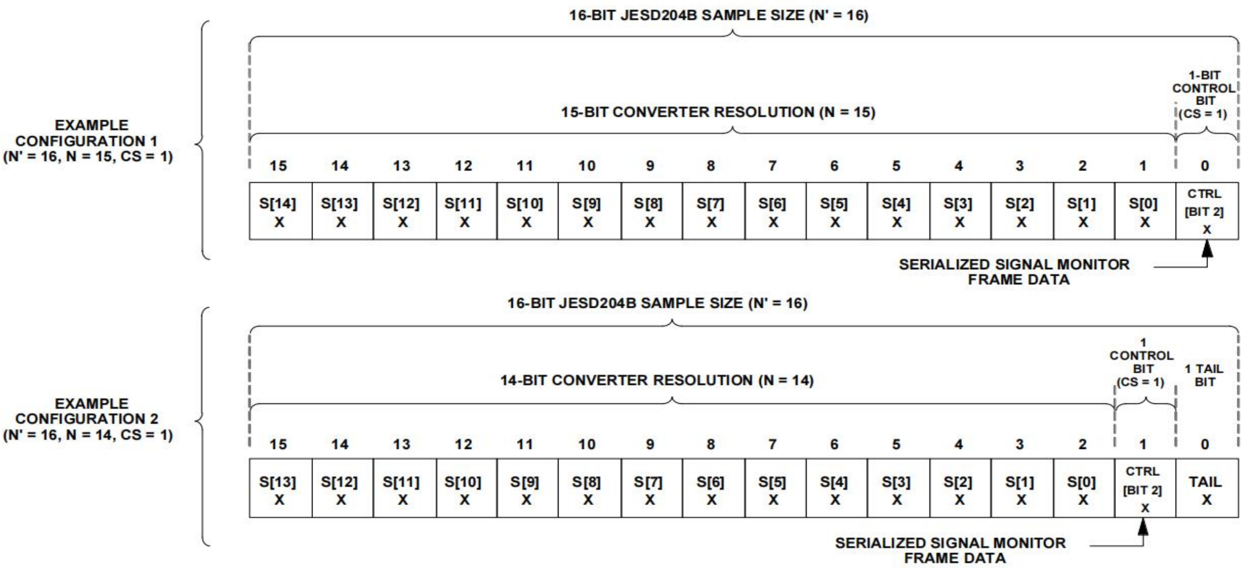
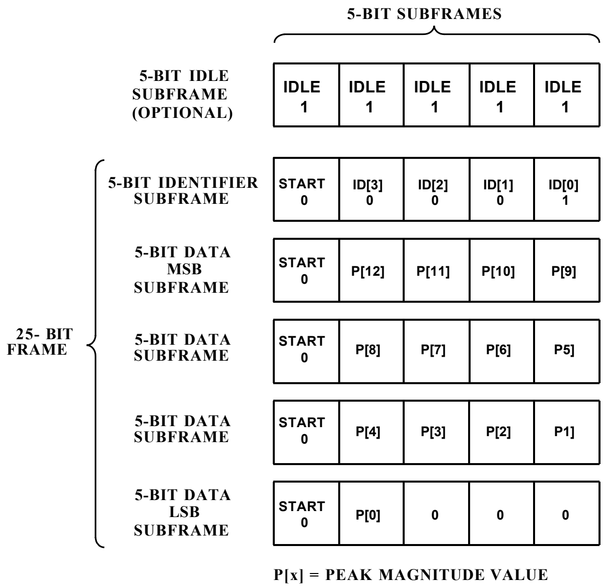
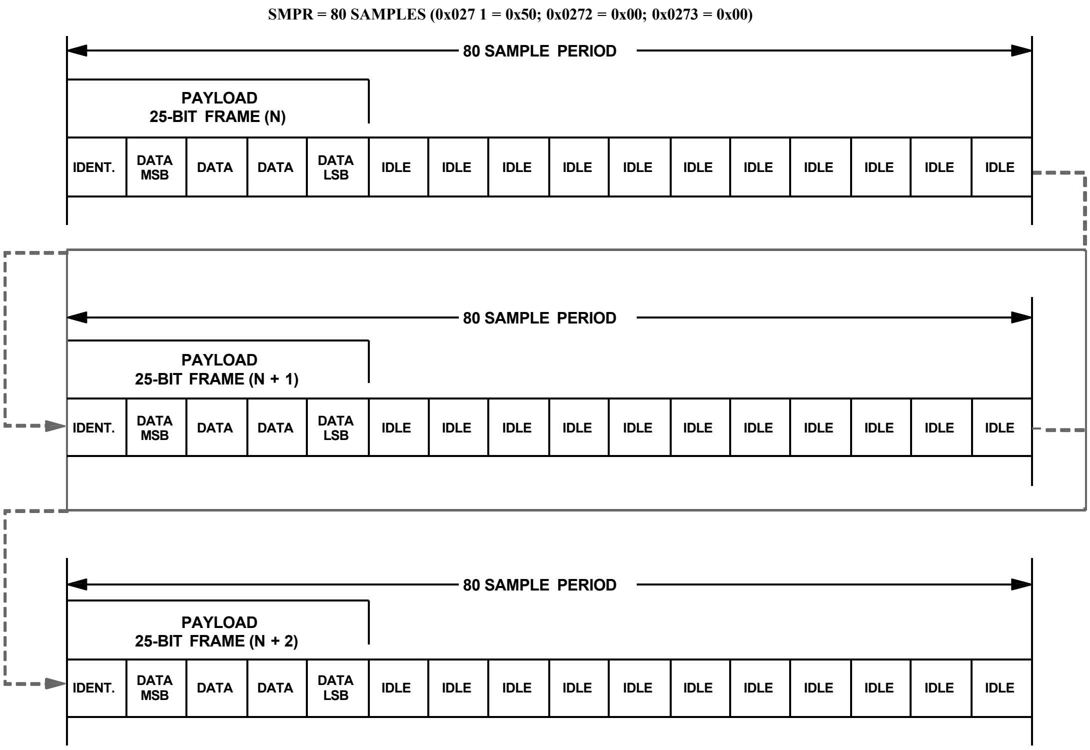


Figure 40 Signal monitoring control bit position



picture 41 JESD 204B ofSPORT Signal monitoring data frame



picture42 JESD 204B ofSPORT Signal Monitoring Example

17. Digital Output

17.1 Introduction to the JESD204B Interface

The CW9689 digital output is designed according to the JEDEC standard JESD204B (" Serial Interface for Data Converters "). JESD204B is the CW9689 serial interface (lane rates up to 16 Gbps) A protocol for connecting digital processing devices. Advantages of the JESD204B interface over LVDS include less board space required for data interface routing and smaller packages for converters and logic devices.

17.2 JESD204B Overview

The JESD204B data transfer block combines the parallel data from the ADC into a data frame and uses 8B/10B encoding and optional data scrambling technology. Outputs serial data. During the initial establishment of the link, channel synchronization is supported by using special control characters; subsequent synchronization is maintained by embedding additional control characters in the data stream. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The CW9689 JESD204B data transmitter block maps up to 2 real ADCs or 8 virtual converters (when DDC is enabled) on one link . A link Can be configured to use 1 , 2 , or 4 JESD204B lanes. JESD204B Specification lead use It's May many Ginseng number Come Certainly righteous chain road , and And JESD204B transmitter (CW9689 output) and JESD204B receiver (logic device input) These parameters must match.

JESD204B link can be described by the following parameters:

- L is the number of data lanes (CW9689 value = 1 , 2 , 4 , or 8)
- M is the number of converters (number of virtual converters) (CW9689 value = 1 , 2 , 4 or 8)
- F is the number of bytes per frame (CW9689 value = 1 , 2 , 4 , 8 or 16)

N9 is the number of bits required to transmit 1 sample (JESD204B word length) (CW9689 value = 8 or 16)

- N is the converter resolution (CW9689 value = 7 ~ 16)

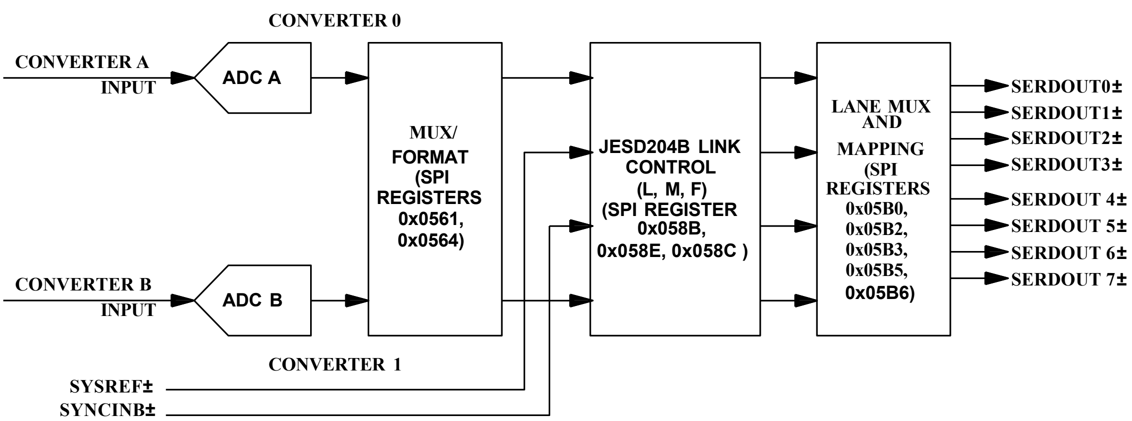
- CS is the control bit / sample number (CW9689 value = 0 , 1 , 2 or 3)
- K is the number of frames per multiframe (value for CW9689 = 4 , 8 , 12 , 16 , 20 , 24 , 28 , or 32)
- S is the number of samples of a single converter in a single frame (the CW9689 value is automatically set based on L , M , F , N9)
- HD is high density mode (CW9689 automatically selects the mode according to L , M , F , N9 set up)
- CF is the number of control words for a single converter in a single frame (CW9689 value = 0)

Figure 43 shows a simplified block diagram of the CW9689 JESD204B link. By default, the CW9689 is configured for two converters and eight data lanes. Converter A data outputs are SERDOUT0 ± , SERDOUT1 ± , SERDOUT2 ± , and SERDOUT3 ± , and Converter B data outputs are SERDOUT4 ± , SERDOUT5 ± , SERDOUT6 ± , and SERDOUT7 ± . The CW9689 supports other configurations, such as combining the outputs of two converters onto a single lane, or changing the mapping of the A and B digital output paths. These modes can be set using the quick configuration registers in the SPI register map. register to set.

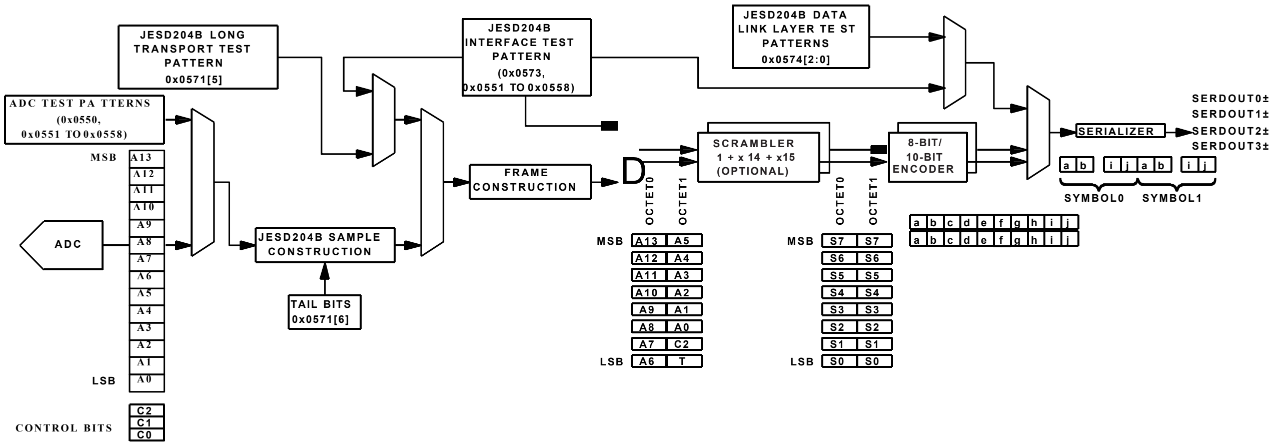
In CW9689 , by default, the 14 -bit data from each converter is split into two octets (8 bits for data) The first octet consists of bits 13 (MSB) through 6. The second octet consists of bits 5 through 0 (LSB) and two tail bits. The tail bits can be configured to be 0 or a pseudo-random number sequence. The tail bits can also be replaced by control bits indicating overrange, SYSREF ± , or fast detect output.

The two generated 8- bit words can be scrambled. Scrambling is optional, but recommended to avoid spectral spikes when transmitting similar digital data patterns. The scrambler uses a self-synchronizing, polynomial-based algorithm defined by equation $1 + x14 + x15$. The descrambler in the receiver is a self-synchronizing version of the scrambler polynomial.

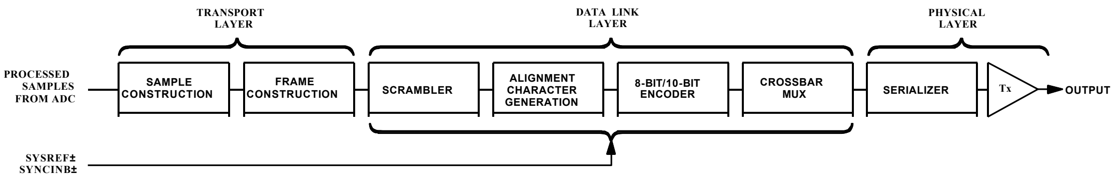
8 -bit bytes are then encoded using the 8B/10B encoder . The 8B/10B encoder works by encoding 8 bits of data (1 8- bit word) into a 10- bit symbol. Figure 44 shows how to get 14 bits of data from the ADC , how to add the stop bit, how to scramble the two 8 -bit words, and how to encode the 8 bits into two 10- bit symbols. Figure 45 shows the default data format.



picture43 Simplified block diagram of the transmit link in full bandwidth mode (0x200=0x00)



picture44 Simplified block diagram of the transmit link in full bandwidth mode (0x200=0x00)



picture45 Data Flow

17.3 Functional Overview

Figure 45 shows the JESD204B hardware data flow from sample input to physical output. Based on the OSI (Open Source Initiative) model, which is widely used to describe the abstraction layers of communication systems, the processing can be divided into multiple layers: transport layer, data link layer, and physical layer (serializer and output driver). .

17.3.1. Transport layer

The transport layer is responsible for packing the data (consisting of samples and optional control bits) into JESD204B frames mapped as 8 -bit words . These 8 -bit words are sent to the data link layer. Transport layer matching is controlled by the rules followed by the link parameters. Stop bits are added as needed to fill the gaps. The number of stop bits in a sample (JESD204B word) can be determined using the following formula :

$$T = N' - N - CS$$

17.3.2. Data Link Layer

The data link layer is responsible for the low-level functions of transmitting data over the link. This includes data scrambling, inserting control characters during the initial lane alignment sequence (ILAS) for frame and multiframe synchronization monitoring, and encoding 8 -bit words into 10 -bit symbols. The data link layer is also responsible for sending the ILAS , which contains link configuration data used by the receiver to verify the transport layer settings.

17.3.3 Physical Layer

The physical layer consists of high-speed circuits that are clocked at the serial clock rate. In this layer, parallel data is converted into 1 , 2 , 4 , or 8 channels of high-speed differential serial data.

17.4 JESD204B Link Establishment

CW9689 JESD204B transmitter (Tx) interface operates in Subclass 0 or Subclass 1 as defined in the JEDEC standard JESD204B (July 2011 specification) . The link establishment process is divided into the following steps: code group synchronization, initial channel alignment sequence, User data and error correction.

17.4.1. Code Group Synchronization (CGS)

CGS is the process by which the JESD204B receiver fins the boundaries between 10 -bit symbols in the data stream . During the CGS phase, the JESD204B transmitter blocks transmit /K28.5/ characters. The receiver must use clock and data recovery (CDR) techniques to locate the /K28.5/ character in its incoming data stream .

The receiver sets the SYNCINB ± pin of the CW9689 low to issue a synchronization request. Then JESD204BTx starts sending /K/ characters. Once the receiver is synchronized, It then waits for at least four consecutive /K/ symbols to be correctly received and then deasserts SYNCINB ± . The CW9689 then sends an ILAS on the next Local Multiframe Clock (LMFC) boundary .

For more information about the code group synchronization phase, See { JEDEC Standard JESD204B , July 2011 , Section 5.3.3.1 } .

The SYNCINB ± pin operation can also be controlled by the SPI . By default, the SYNCINB ± signal is a differential, DC-coupled LVDS signal, but can also be driven single-ended. See Register 0x572 for more information on configuring the SYNCINB ± pin operation .

The SYNCINB ± pins can also be configured to operate in CMOS (single-ended) mode by setting Bit 4 in Register 0x572 . When operating SYNCINB ± in CMOS mode , Set the CMOS SYNCINB signal Number even catch arrive lead Pin 21 (SYNCINB+) is connected and Pin 20 (SYNCINB—) is disconnected.

17.4.2. Initial Lane Alignment Sequence (ILAS)

ILAS phase follows the CGS phase and begins at the lower limit after SYNCINB ± is asserted. A LMFC boundary. ILAS consists of four multiframes, starting with an /R/ character mark and ending with an /A/ character mark. ILAS first sends an /R/ character, This is followed by a multiframe of 0 to 255 ramp data. The link configuration data is sent starting with the third character on the second multiframe. The second character is a /Q/ character that acknowledges the link configuration data. All undefined data slots are filled with ramp data. The ILAS sequence is never repeated. Disturbance.

ILAS sequence construction is shown in Figure 46. The four multi-frames include:

●Multiframe 1 starts with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

● Multiframe 2 , starts with an /R/ character followed by a /Q/ character (/K28.4/), Then there are 14 8 -bit words of link configuration parameters (see Table 17.1). with a /A/ character. Many parameter values are represented by -1 .
● Multiframe 3 , starts with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/) Finish.
● Multiframe 4 , starts with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/) Finish.

17.4.3. User Data and Error Detection

After the initial channel alignment sequence is completed, the user data (ADC samples) are sent. During the user data transmission process, A mechanism called character replacement is used to monitor the frame clock When the data meets certain conditions, the mechanism uses /F/ or /A/ to align The character replaces the last octet of a frame or multiframe. These conditions are different for unscrambled and scrambled data. Scrambling is enabled by default, but can be disabled by SPI disabled .

For scrambled data, any 0xFC characters at the end of a frame are replaced by /F/ , and any 0x7C characters at the end of a multiframe are replaced by /A/ . The JESD204B receiver (Rx) checks the received data stream for /F/ and /A/ characters and verifies that they appear only in expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic adjustments or asserting the SYNCINB ± signal for more than four frames to initiate resynchronization. For unscrambled data, if the last octet of two consecutive frames is equal, the second octet is at the end of the frame. Then use the /F/ symbol to replace it. If it is at the end of a multiframe, it is replaced with an /A/ symbol.

can be modified using the SPI . By default, the frame alignment character insertion feature (FACI) is enabled. For more information on link control, see Register 0x571 in the Register Map Table section .

17.4.4. 8B/10B Encoder

8B/10B encoder converts 8 -bit words into 10- bit symbols and inserts control characters into the data stream when required. The control characters used in JESD204B are shown in Table 25. 8B/10B encoding ensures that the signal is DC balanced by using an equal number of 1s and 0s across multiple symbols .

8B/10B interface has controllable operations. These operations include bypass and inversion. These options are used as a troubleshooting tool for Digital Front End (DFE) verification. For information on configuring the 8B/10B encoder, Refer to Register 0x572[2:1] in the Register Map Table section .

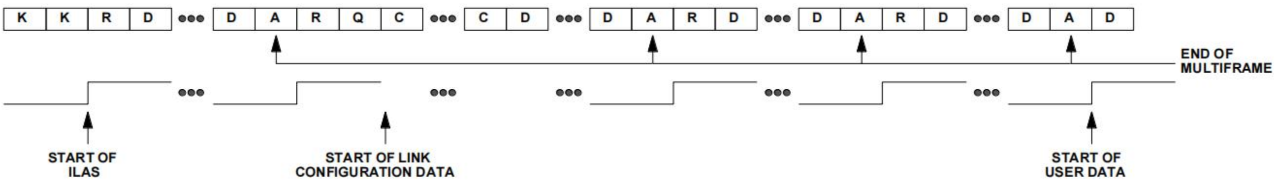


Figure 46 Initial channel alignment sequence

surface25 CW9689 UsedJESD 204B Control Characters

abbreviation	Control Symbols	8 Place value	10 -bit value, RD [1] = -1	10 -bit value, RD [1] = +1	illustrate
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Multi-frame start
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Channel Alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Link configuration data starts
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group Synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame Alignment

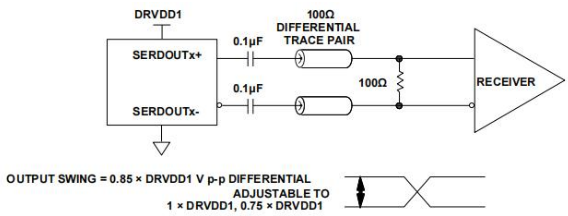
[1] RD Represents running differences

17.5 Physical layer (driver) output

The CW9689 physical layer consists of drivers specified in JEDEC standard JESD204B (July 2011). The default power - up is differential digital output. The driver uses a 100 Ω dynamic internal termination resistor to reduce reflection interference.
100 Ω differential termination resistor is placed at each receiver input to produce a nominal swing of 0.85 × DRVDD1 Vp-p at the receiver (see Figure 47). The swing can be adjusted through the SPI register. It is recommended to connect the receiver using AC coupling. For more details, refer to the register map table section (registers 0x05c50~0x05C3) for more details.
CW9689 digital output can be interfaced with custom ASIC and FPGA receivers to achieve excellent switching performance in high noise environments. A single point-to-point network topology is recommended. Place a single 100 Ω differential termination resistor as close to the receiver input as possible.

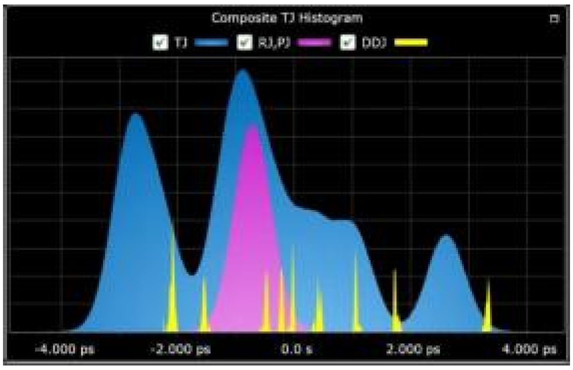
If there is no far-end receiver termination resistor or the differential traces are poorly laid out, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than 6 inches and the differential output traces should be as close to each other as possible and of equal length.

Figure 48 , Figure 49 , and Figure 50 show examples of the digital output data eye diagram, jitter histogram, and bathtub curve for a CW9689 channel operating at 16 Gbps . By default, the output data is formatted in two's complement. To change the output data format, see the Register Map section (Register 0x0561).

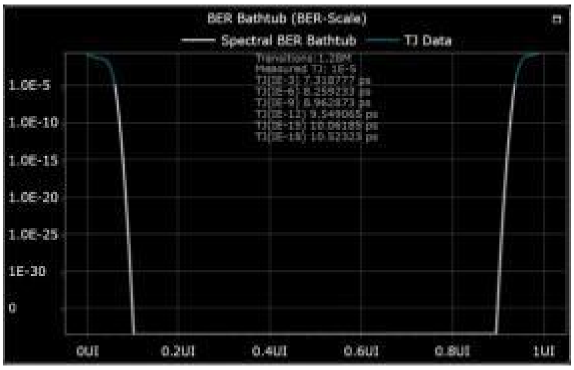


picture47 AC Coupled Digital Output Termination Example

picture48 Digital Output Eye Diagrams (16 Gbps External Termination 100Ω)



picture49 Digital Output Jitter Histogram (16 Gbps External Termination 100Ω)



picture50 Digital Output Bathtub Curve (16 Gbps External Termination 100Ω)

17.5.1. De-aggravation

De-emphasis can be used when the interconnect insertion loss does not meet the JESD204B specification Meet the receiver eye mask. De-emphasis is used only when the receiver cannot recover the clock due to excessive insertion loss. Normally, this feature is disabled to save power. In addition, enabling and setting too high a de-emphasis value on a short link may cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it can increase electromagnetic interference (EMI). Refer to the Register Map section (registers 0x05C4 to 0x05CA in Table 38) for more details.

17.5.2. Phase-Locked Loop

A phase-locked loop (PLL) is used to generate the serial clock, It operates at JESD204B lane rates The lock status of the PLL can be viewed in the PLL Lock Status bit (Bit 7 of Register 0x056F) . This read-only bit informs the user whether PLL lock has been achieved for a particular setup. Register 0x056F also has a Loss of Lock Hold bit (Bit 3) which informs the user that a PLL loss of lock has been detected . This can be reset by issuing a JESD204B Link Restart (Register 0x0571 , Bit 0 = 0x1 , followed by Register 0x0571 , Bit 0 = 0x0). Reset the lock hold bit.

JESD204B lane rate control, Bits[7:4] of Register 0x056E must be set to correspond to the lane rate. Table 26 shows the lane rates supported by the CW9689 using Register 0x056E .

surface26 CW9689 register0x56E Supported channel rate

Value	Lane Rate
0x00	Lane rate = 6.75 Gbps to 13.5
0x10	Lane rate = 3.375 Gbps to 6.75 Gbps (default)
0x30	Lane rate = 13.5 Gbps to 16 Gbps
0x50	Lane rate = 1.6875 Gbps to 3.375 Gbps

17.6 CW9689 Digital Interface Settings

To ensure that the CW9689 works properly at startup, some SPI write operations are required to initialize the link. In addition, the ADC must be written every time it is reset. These registers. Any of the following resets guarantees the initialization routine of the digital interface:

●Hard reset, just like a power-on.
●Use the PDWN pin to power on.
●Power on using the SPI via Register 0x0002 , Bits [1:0] .
● SPI soft reset by setting register 0x0000 = 0x81 .
● A datapath soft reset is accomplished by setting Register 0x0001 = 0x02 .
● The JESD204B link is powered up and down by setting Register 0x0571 , Bit 0 = 0x1 and then 0x0 .

CW9689 has one JESD204B chains road . string OK lose The outputs (SERDOUT0 ± to SERDOUT3 ±) are considered part of a JESD204B link. The basic parameters that determine the link setup are

●Number of data paths per link (L)
● Number of converters per link (M)
● Number of 8 -bit bytes per frame (F)

If the internal DDCs are used for on-chip digital processing, M represents the number of virtual converters.

In CW9689 , by default, 14 bits from each converter are The converter word is divided into 2 octets (8 -bit data). Bits 13 (MSB) to Bit 6 is located in the first octet. The second octet contains bits 5 to 0 (LSB) and two stop bits. The stop bits can be configured to be zero or a pseudo-random sequence. Replaced with control bits, Indicates overrange, SYSREF ± , or fast detect output. The control bits are populated and inserted MSB first , enabling CS = 1 activates Control Bit 2 , enabling CS = 2 activates Control Bit 2 and Control Bit 1 , and enabling CS = 3 activates Control Bit 2 , Control Bit 1 , and Control Bit 0 .

The maximum channel rate allowed by CW9689 is 16Gbps .

lane rate and JESD204B parameters is as follows:

$$Lane\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

$$f_{OUT} = \frac{f_{ADC\_CLOCK}}{Decimation\ Ratio}$$

The decimation ratio (DCM) is a parameter written to register 0x0201 .

The output can be configured using the following steps:

1. Shut down the link.
2. Select the JESD204B Link Configuration option.
3. Configure detailed options.
4. Set output channel mapping (optional).
5. Set other drive configuration options (optional).
6. Power on the link.
7. Initialize the JESD204B link.

Register 0x056E must be written according to the calculated Lane rate. Refer to the Phase-Locked Loop (PLL) section for more details.

Table 27 , Table 28 , and Table 29 show the supported JESD204B output configurations for a given number of virtual converters for N′ = 16 , N' = 12 , and N′ = 8. Care should be taken to ensure that the serial lane rate for a given configuration is within the supported range of 1.6875 Gbps to 16 Gbps .

surface27 N, = 16 [1] ofJESD 204B Output Configuration

Number of Virtual Converters Supported (Same as M)	JESD204B Serial Lane Rate[2]	Supported Decimation Rates: Lane Rate = 1.6875 Gbps to 3.375 Gbps	Lane Rate = 3.375 Gbps to 6.75 Gbps	Lane Rate = 6.75 Gbps to 13.5 Gbps	Lane Rate = 13.5 Gbps to 16 Gbps	JESD204B Transport Layer Settings[3]: L	M	F	S	HD	N	N,	CS	K
1	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	1	2	1	0	8 to 16	16	0 to 3	lake Grade 4
	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	1	4	2	0	8 to 16	16	0 to 3	lake Grade 4
	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	2	1	1	1	1	8 to 16	16	0 to 3	lake Grade 4
	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	2	1	2	2	0	8 to 16	16	0 to 3	lake Grade 4
	5 × f_{OUT}	1, 2, 3, 4	1, 2	1		4	1	1	2	1	8 to 16	16	0 to 3	lake Grade 4
	5 × f_{OUT}	1, 2, 3, 4	1, 2	1		4	1	2	4	0	8 to 16	16	0 to 3	lake Grade 4
2	40 × f_{OUT}	4, 8, 10, 12, 15, 16, 20, 24, 30	2, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1	2	4	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12, 15, 16, 20, 24, 30	2, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1	2	8	2	0	8 to 16	16	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	2	2	2	1	0	8 to 16	16	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	2	2	4	2	0	8 to 16	16	0 to 3	See Note 4
	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	4	2	1	1	1	8 to 16	16	0 to 3	See Note 4
	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	4	2	2	2	0	8 to 16	16	0 to 3	See Note 4
4	80 × f_{OUT}	8, 16, 20, 24, 30, 40, 48	4, 8, 10, 12, 16, 20, 24, 30	2, 4, 6, 8, 10, 12, 16	2, 4, 6, 8	1	4	8	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12, 15, 16, 20, 24, 30	2, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	2	4	4	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12, 15, 16, 20, 24, 30	2, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	2	4	8	2	0	8 to 16	16	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	4	4	2	1	0	8 to 16	16	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	4	4	4	2	0	8 to 16	16	0 to 3	See Note 4
	80 × f_{OUT}	8, 16, 20, 24, 30, 40, 48	4, 8, 10, 12, 16, 20, 24, 30	2, 4, 6, 8, 10, 12, 16	2, 4, 6, 8	1	4	8	1	0	8 to 16	16	0 to 3	See Note 4
8	160 × f_{OUT}	16, 40, 48	8, 16, 20, 24, 40, 48	4, 8, 12, 16, 20, 24	4, 8, 12, 16	1	8	16	1	0	8 to 16	16	0 to 3	See Note 4
	80 × f_{OUT}	8, 16, 20, 24, 40, 48	4, 8, 10, 12, 16, 20, 24	2, 4, 6, 8, 10, 12, 16	2, 4, 6, 8	2	8	8	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12, 16, 20, 24	2, 4, 6, 8, 10, 12, 16	2, 4, 6, 8	2, 4	4	8	4	1	0	8 to 16	16	0 to 3	See Note 4
	40 × f_{OUT}	4, 8, 10, 12, 16, 20, 24	2, 4, 6, 8, 10, 12, 16	2, 4, 6, 8	2, 4	4	8	8	2	0	8 to 16	16	0 to 3	See Note 4

[1] Due to internal clock requirements, some link parameters only support specific decimation rates.

2 .The JESD204B transport layer is described as follows: L is the number of data lanes; M is the number of converters (number of virtual converters); F is the number of bytes per frame; S is the number of samples per converter in a single frame; HD is high density mode; N is the converter resolution in bits ; N' is the number of bits required to transmit one sample (JESD204B word length) ; CS is the number of control bits / samples; K is the number of frames in each multiframe.
3.f_{ADC_CLK} is the ADC sampling rate; DCM = chip decimation rate; f_{OUT} Output sampling rate = $f_{ADC\_CLK / DCM}$; SLR is the JESD204B serial lane rate. Due to the requirements of the internal clock divider, the following equations must be met: Line rate ≥ 1.6875 Gbps , line rate ≤ 15.5 Gbps ; SLR / 40 ≤ f_{ADC_CLK} ; Least common multiple (20 × DCM × f_{OUT} / line rate, DCM) ≤ 64. When the SLR rate is ≤ 16000Mbps and > 13500Mbps , Register 0x056E must be set to 0x30. When the line rate is ≤ 13500Mbps and ≥ 6750Mbps, Register 0x056E must be set to 0x00 . When the line rate is < 6750Mbps and ≥ 3375Mbps , Register 0x056E must be set to 0x10 . When the line rate is <3375Mbps and ≥1687.5Mbps , Register 0x056E must be set to 0x50 .
4. Only valid K × F values divisible by 4 are supported : for F=1 , K=20 , 24 , 28 , 32 ; for F=2 , K=12 , 16 , 20 , 24 , 28 , 32 ; for F=4 , K=8 , 12 , 16 ,
20 , 24 , 28 , 32 ; for F=8 , K=4 , 8 , 12 , 16 , 20 , 24 , 28 , 32 ; for F=16 , K = 4 , 8 , 12 , 16 , 20 , 24 , 28 , 32 .

surface28 N, = 12 [1] ofJESD 204B Output Configuration

Number of Virtual Converters Supported (Same as M)	JESD204B Serial Lane Rate[2]	Supported Decimation Rates				JESD204B Transport Layer Settings[3]								
		Lane Rate = 1.6875 Gbps to 3.375 Gbps	Lane Rate = 3.375 Gbps to 6.75 Gbps	Lane Rate = 6.75 Gbps to 13.5 Gbps	Lane Rate = 13.5 Gbps to 16 Gbps	L	M	F	S	HD	N	N,	CS	K
1	15 × f_{OUT}	3, 6, 12	3, 6	3		1	1	3	2	0	8 to 12	12	0 to 3	See Note 4
	7.5 × f_{OUT}	3, 6	3			2	1	3	4	1	8 to 12	12	0 to 3	See Note 4
	7.5 × f_{OUT}	3, 6	3			2	1	6	8	0	8 to 12	12	0 to 3	See Note 4
	5 × f_{OUT}	1, 2, 3, 4	1, 2	1		3	1	1	2	1	8 to 12	12	0 to 3	See Note 4
2	30 × f_{OUT}	3, 6, 12, 24	3, 6, 12	3, 6		1	2	3	1	0	8 to 12	12	0 to 3	lake note 4
	15 × f_{OUT}	3, 6, 12	3, 6	3		2	2	3	2	0	8 to 12	12	0 to 3	lake note 4
	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	3	2	1	1	1	8 to 12	12	0 to 3	lake note 4
	7.5 × f_{OUT}	3, 6	3			4	2	3	4	0	8 to 12	12	0 to 3	lake note 4
4	60 × f_{OUT}	6, 12, 24, 48	3, 6, 12, 24	3, 6, 12		1	4	6	1	0	8 to 12	12	0 to 3	lake note 4
	30 × f_{OUT}	3, 6, 12, 24	3, 6, 12	3, 6		2	4	3	1	0	8 to 12	12	0 to 3	lake note 4
	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	3	4	2	1	1	8 to 12	12	0 to 3	lake note 4
	15 × f_{OUT}	3, 6	3	3		4	4	3	2	0	8 to 12	12	0 to 3	lake note 4
8	60 × f_{OUT}	6, 12, 24, 48	6, 12, 24	6, 12		2	8	6	1	0	8 to 12	12	0 to 3	See Note 4
	30 × f_{OUT}	6, 12, 24	6, 12	6		4	8	3	1	0	8 to 12	12	0 to 3	See Note 4

[1] Due to internal clock requirements, some link parameters only support specific decimation rates.
[2] The JESD204B transport layer is described as follows: L is the number of data lanes; M is the number of converters (number of virtual converters); F is the number of bytes per frame; S is the number of samples per converter in a single frame; HD is high density mode; N is the converter resolution in bits ; N' is the number of bits required to transmit one sample (JESD204B word length) ; CS is the number of control bits / samples; K is the number of frames in each multiframe.
[3] fADC_CLK is the ADC sampling rate; DCM = chip decimation rate ; fOUT Output sampling rate = $f_{ADC\_CLK / DCM}$; SLR is the JESD204B serial lane rate. Due to the requirements of the internal clock divider, the following equations must be met: Line rate ≥ 1.6875 Gbps , line rate ≤ 15.5 Gbps ; SLR / 40 ≤ f_{ADC_CLK} ; Least common multiple (20 × DCM × f_{OUT} / line rate, DCM) ≤ 64. When the SLR rate is ≤ 16000Mbps and > 13500Mbps , Register 0x056E must be set to 0x30. When the line rate is ≤ 13500Mbps and ≥ 6750Mbps, Register 0x056E must be set to 0x00 . When the line rate is < 6750Mbps and ≥ 3375Mbps , Register 0x056E must be set to 0x10 . When the line rate is <3375Mbps and ≥1687.5Mbps , Register 0x056E must be set to 0x50 .
[4] Only valid K × F values that are divisible by 4 are supported : for F=1 , K=20 , 24 , 28 , 32 ; for F=2 , K=12 , 16 , 20 , 24 , 28 , 32 ; for F=4 , K=8 , 12 , 16 , 20 , 24 , 28 , 32 ; for F=8 , K=4 , 8 , 12 , 16 , 20 , 24 , 28 , 32 ; for F=16 , K = 4 , 8 , 12 , 16 , 20 , 24 , 28 , 32 .

surface 29 N, = 8 [1] of JESD 204B Output Configuration

Number of Virtual Converters Supported (Same as M)	JESD204B Serial Lane Rate [2]	Supported Decimati on Rates				JESD204B Transport Layer Settings[3]								
		Lane Rate = 1.6875 Gbps to 3.375 Gbps	Lane Rate = 3.375 Gbps to 6.75 Gbps	Lane Rate = 6.75 Gbps to 13.5 Gbps	Lane Rate = 13.5 Gbps to 16 Gbps	L	M	F	S	HD	N	N,	CS	K
1	10 × f_{OUT}	1,2,3,4,5,6,8	1,2,3,4	1,2	1	1	1	1	1	0	7 to 8	8	0 to 1	See Note 4
1	10 × f_{OUT}	1,2,3,4,5,6,8	1,2,3,4	1.2	1	1	1	2	2	0	7 this 8	8	0 this 1	This Note 4
1	5 × f_{OUT}	1,2,3,4	1.2	1		2	1	1	2	0	7 this 8	8	0 this 1	This Note 4
1	5 × f_{OUT}	1,2,3,4	1.2	1		2	1	2	4	0	7 this 8	8	0 this 1	This Note 4
1	5 × f_{OUT}	1,2,3,4	1.2	1		2	1	4	8	0	7 this 8	8	0 this 1	This Note 4
1	2.5 × f_{OUT}	1.2	1			4	1	1	4	0	7 this 8	8	0 this 1	This Note 4
1	2.5 × f_{OUT}	1.2	1			4	1	2	8	0	7 this 8	8	0 this 1	This Note 4
2	20 × f_{OUT}	2,4,5,6,8, 10, 12,15,16	1,2,3,4,5,6,8	1,2,3,4	1.2	1	2	2	1	0	7 this 8	8	0 this 1	This Note 4
2	10 × f_{OUT}	1,2,3,4,5,6,8	1,2,3,4	1.2	1	2	2	1	1	0	7 this 8	8	0 this 1	This Note 4
2	10 × f_{OUT}	1,2,3,4,5,6,8	1,2,3,4	1.2	1	2	2	2	2	0	7 this 8	8	0 this 1	This Note 4
2	5 × f_{OUT}	1,2,3,4	1.2	1		4	2	1	2	0	7 this 8	8	0 this 1	This Note 4
2	5 × f_{OUT}	1,2,3,4	1.2	1		4	2	2	4	0	7 this 8	8	0 to 1	See Note 4
2	5 × fOUT	1,2,3,4	1,2	1		4	2	4	8	0	7 to 8	8	0 to 1	See Note 4

1Some link parameters only support certain decimation rates due to internal clock requirements.
2 The JESD204B transport layer is described as follows: L is the number of data lanes; M is the number of converters (number of virtual converters); F is the number of bytes per frame; S is the number of samples per converter in a single frame; HD is high density mode; N is the converter resolution in bits ; N' is the number of bits required to transmit one sample (JESD204B word length) ; CS is the number of control bits / samples; K is the number of frames in each multiframe.
3f_{ADC_CLK} is the ADC sampling rate; DCM = chip decimation rate; f_{OUT} is the output sampling rate = $f_{ADC\_CLK/DCM}$; SLR is the JESD204B serial lane rate. Due to the requirements of the internal clock divider, the following equations must be met: Line rate ≥ 1.6875 Gbps , line rate ≤ 15.5 Gbps ; SLR /40 ≤ f_{ADC_CLK} ; the lowest common multiple (20 × DCM × f_{OUT} / line rate, DCM) ≤ 64. When the SLR rate is ≤ 16000Mbps and > 13500Mbps , Register 0x056E must be set to 0x30 . When the line rate is ≤ 13500Mbps and ≥ 6750Mbps , " Register 0x056E" must be set to 0x00 . When the line rate is < 6750Mbps and ≥ 3375Mbps , Register 0x056E must be set to 0x10 . When the line rate is <3375Mbps and ≥1687.5Mbps , Register 0x056E must be set to 0x50 .
4 Only valid K × F values divisible by 4 are supported : for F=1 , K=20 , 24 , 28 , 32 ; for F=2 , K=12 , 16 , 20 , 24 , 28 , 32 ; for F=4 , K=8 , 12 , 16 ,
20 , 24 , 28 , 32 ; for F=8 , K=4 , 8 , 12 , 16 , 20 , 24 , 28 , 32 ; for F=16 , K = 4 , 8 , 12 , 16 , 20 , 24 , 28 , 32 .

18.Multi -chip synchronization

FIG. 51 describesCW9689 Internal synchronization of multiple chips

There are two ways to achieve multi-chip synchronization, which are determined by the chip synchronization mode bit. (Register 0x1 FF , Bit 0) determines which method is used . Each method involves Different applications of the SYSREF ± signal.

18.1 Normal Mode

The default value of the chip synchronization mode bit is0 , indicatingCW9689 Perform normal mode Chip synchronization.

The JESD 204B standard specifies the use of SYSREF ± to provide deterministic The same concept, when applied to a system with multiple converters and logic devices In Figure 51 , this synchronization mode is called normal mode. Following the process shown in the flowchart can ensure CW9689 The configuration is correct. Please consult the Intellectual Property (IP) Guide for Logic Device Users to ensure JESD 204B catch The receiving end is configured correctly.

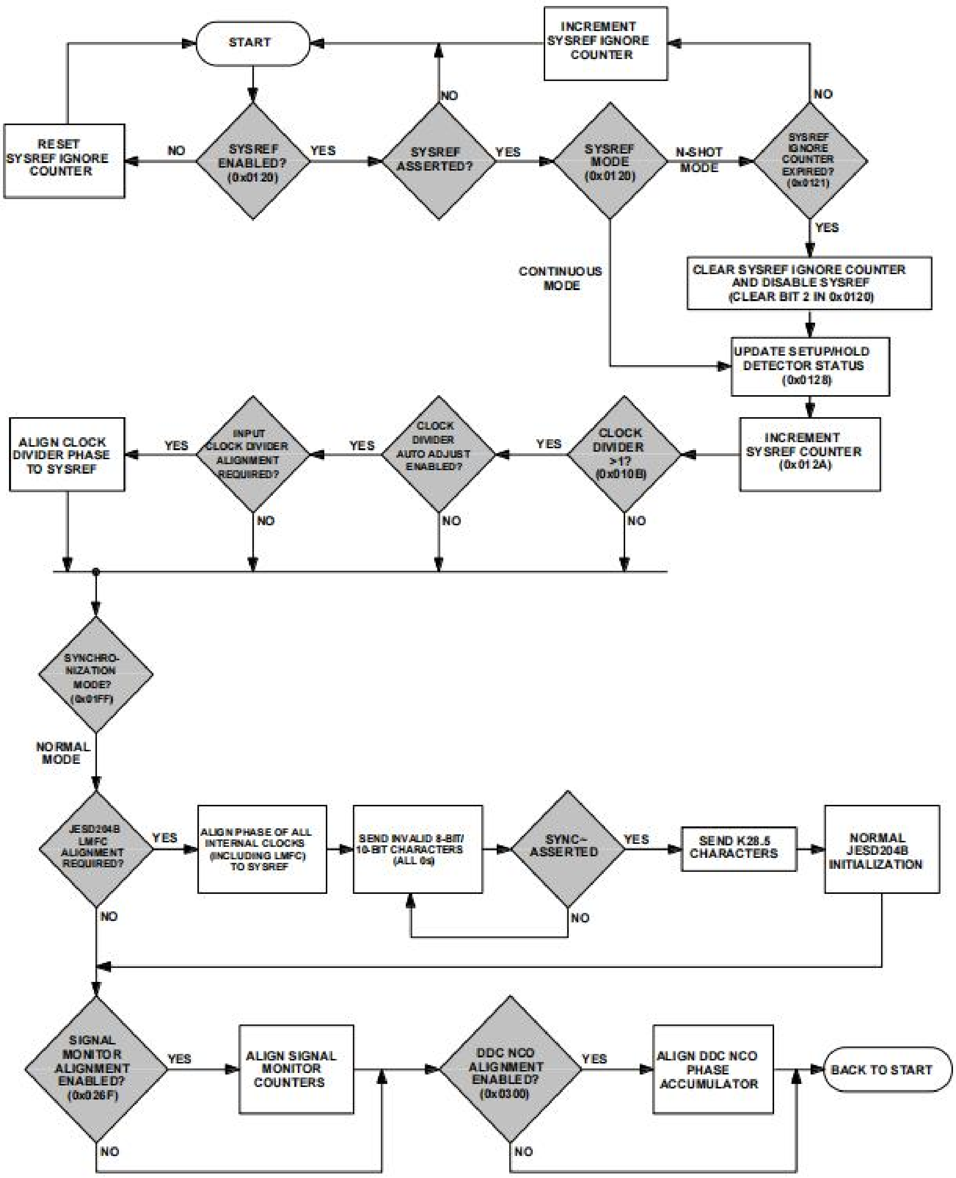


Figure 51 SYSREF ± capture scenario and multi-chip synchronization

18.2 SYSREF ± Input

The SYSREF ± input signal is a high-precision system reference used for deterministic delay and multichip synchronization.
The CW9689 accepts either single-shot or periodic input signals. The SYSREF ± mode select bits (Register 0x0120 , bits[2:1]) select the input signal type and activate the SYSREF ± state machine when set . If in single-shot or N -shot pulse mode (Register 0x0120 , Bits[2:1] = 2) The SYSREF ± mode select bit is automatically cleared after the corresponding SYSREF ± transition is detected . The minimum pulse width must be two CLK ± If the clock divider (Register 0x010B , Bits[3:0]) is set to a value other than 1x , multiply this minimum pulse width requirement by the divide ratio (for example, If divide-by- 8 is set , the minimum pulse width is 16 CLK ± cycles . When using a continuous SYSREF ± signal (Register 0x0120 , Bits[2:1] = 1), SYSREF ± The period of the signal must be an integer multiple of LMFC . Use the following formula to derive LMFC :

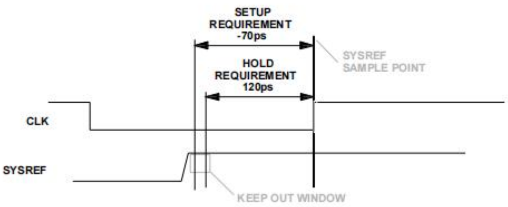
LMFC = ADC Clock/S × K

in:
S is a JESD204B parameter representing the number of samples per converter.
K is a JESD204B parameter representing the number of frames per multiframe.

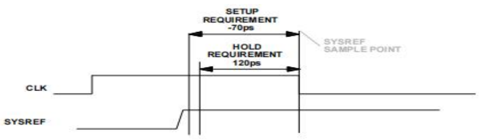
In normal synchronous mode (register 0x01FF , Bits[1:0] = 0), the input The clock divider, DDC , signal monitor block, and JESD204B link all use
The SYSREF ± inputs can also be used to time - stamp the ADC samples, which can provide a synchronization mechanism for multiple CW9689 devices are synchronized. For the highest level of timing accuracy, SYSREF ± must meet setup and hold requirements relative to the CLK ± inputs. There are several features in the CW9689 to ensure that these requirements are met (see the SYSREF ± Control Characteristics section).

18.2.1. SYSREF ± Control Characteristics

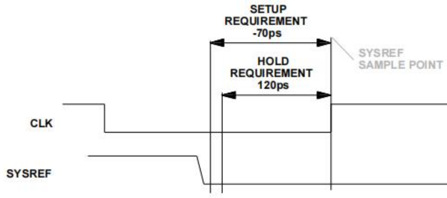
SYSREF ± is used with the input clock (CLK ±) as part of a source synchronous timing interface and requires setup and hold timing requirements of 117 ps and -96 ps , respectively, relative to the input clock (see Figure 52). The CW9689 has several features to meet these requirements . First, the SYSREF ± sampling event can be defined as either a synchronous low-to-high transition or a synchronous high-to-low transition. Second, the CW9689 allows the SYSREF ± signal to be sampled using either the rising or falling edge of the input clock . Figure 52 , Figure 53 , Figure 54 , and Figure 55 show all four possible combinations. The third available SYSREF ± -related feature is the ability to ignore a programmable number (up to 16) of SYSREF ± event.



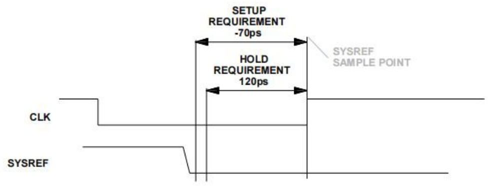
picture52 SYSREF ± setup and hold time requirements ; SYSREF ± low-to-high transitions enable
Use rising edge clock (default)



picture53 The low-to-high transition of SYSREF ± is captured using the falling edge of the clock (0x0120 ,
Bit 4 = 1'b0 and0x0120 , Bit 3 = 1'b 1 ）



picture54 The high-to-low transition of SYSREF ± is captured using the rising edge of the clock (0x0120 ,
Bit 4 = 1'b1 and0x0120 , Bit 3 = 1'b0 ）



picture55 The high-to-low transition of SYSREF ± is captured using the falling edge of the clock (0x0120 ,
Bit 4=1'b1 and0x0120 , Bit 3 = 1' b1 ）

The SYSREF ± ignore feature is enabled by setting the SYSREF ± mode register (Register 0x0120 , Bits[2:1]) to 2'b10 , which is referred to as N-shot mode. The CW9689 is able to ignore N SYSREF ± events, which is useful for handling periodic SYSREF ± signals that require time to settle after startup. Ignoring SYSREF ± until the clock in the system has stabilized can avoid inaccurate SYSREF ± triggering. Figure 56 shows an example of the SYSREF ± ignore feature when three SYSREF ± events are ignored .
When in continuous SYSREF ± mode (Register 0x0120 , Bits[2:1] = 1), the CW9689 monitors the position of the SYSREF ± edge compared to the internal LMFC . If the SYSREF ± edge is captured by a clock edge that is not aligned with the LMFC ,
CW9689 will initiate a link re-establishment. Since the input clock rate of CW9689 can be as high as 2.6GHz , CW9689 provides another The CW9689 has a programmable SYSREF ± tilt window to accommodate periodic SYSREF ± signals in situations where cycle-accurate capture is not feasible or desired . Allows the internal divider to be undisturbed, Unless SYSREF ± occurs outside the skew window. The resolution of the SYSREF ± skew window is set in sample clock cycles. If the SYSREF ± negative skew window is 1 and the positive skew window is 1 , the total skew window is ± 1 sample clock cycle, which means that as long as SYSREF ± is captured within ± 1 sample clock cycle of the clock aligned to the LMFC , the link will continue to operate normally. If SYSREF ± has jitter, which can cause misalignment between SYSREF ± and LMFC , the system continues to operate without the need for resynchronization while still allowing the device to monitor larger errors caused by jitter.
For the CW9689 , the positive and negative skew windows are controlled by the SYSREF ± Window Negative Bit Register (0x0122 , bits[3:2]) and the SYSREF ± Window Positive Bit Register (0x0122 , bits[1:0]). Figure 57 shows the position information of the skew window settings relative to the internal divider phase 0. Negative skew is defined as occurring before the internal divider reaches phase 0 , Positive bias is defined as occurring after the internal divider reaches phase 0 .

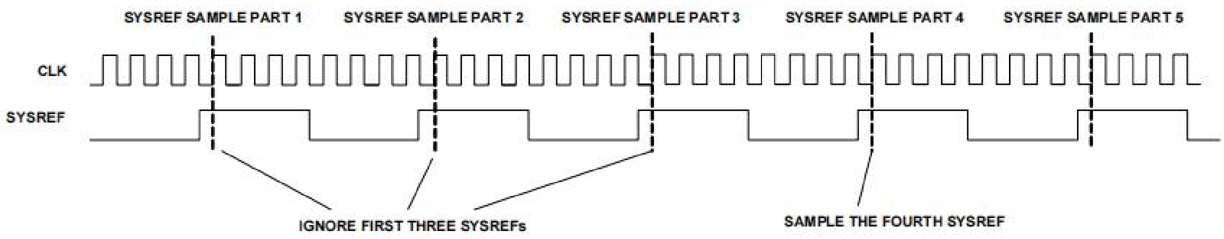


Figure 56. SYSREF ± Ignore Example ; SYSREF ± Ignore Count Bits (Register 0x0121Bits[3:0]) = 3

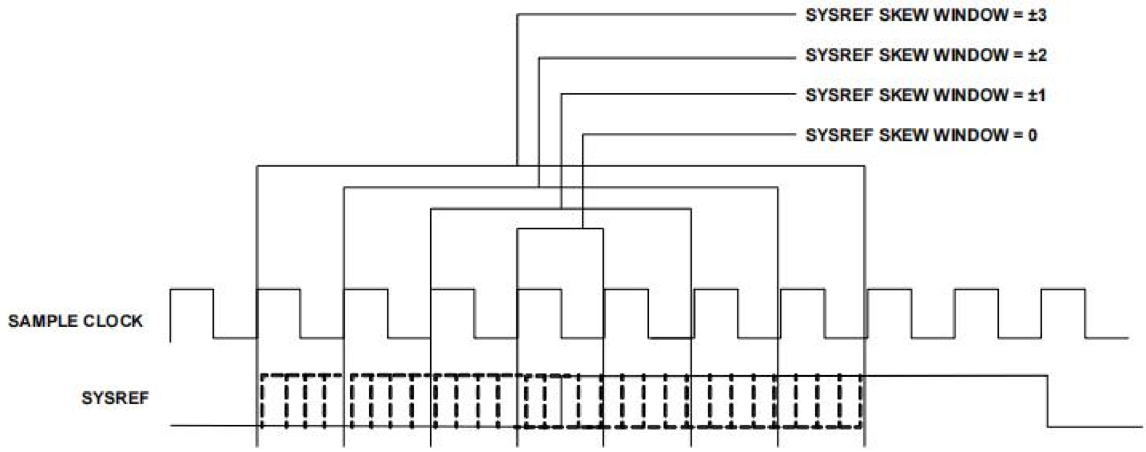


Figure 57 SYSREF ± Tilt Window

18.3 SYSREF+ Create / Hold Window Monitor

To ensure valid SYSREF+ signal capture, CW9689 has a SYSREF+ setup / hold window monitor : This feature allows system designers to determine the location of the SYSREF master signal relative to the CLK signal by reading the setup / hold margin on the interface through memory mapping. Figure 58 and Figure 59 show the setup and hold status values of SYSREF at different stages. The setup detector returns the state of the SYSREF+ signal before the CLK+ edge , and the hold detector returns the state of the SYSREF signal after the CLK+ edge . Register 0x0128 stores the state of SYSREF+ and lets the user know whether the SYSREF signal is captured by the ADC : Table 30 describes the contents of register 0x0128 and the corresponding description.

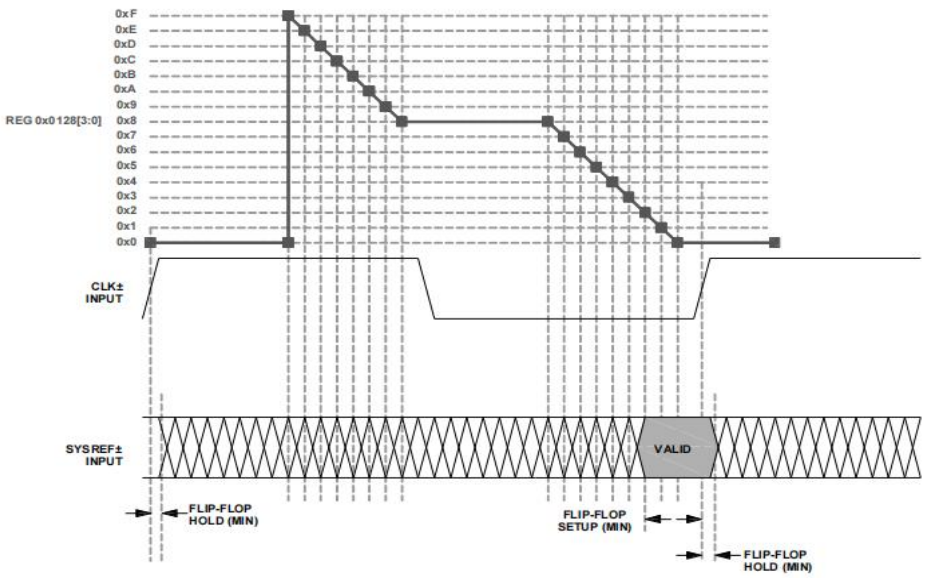
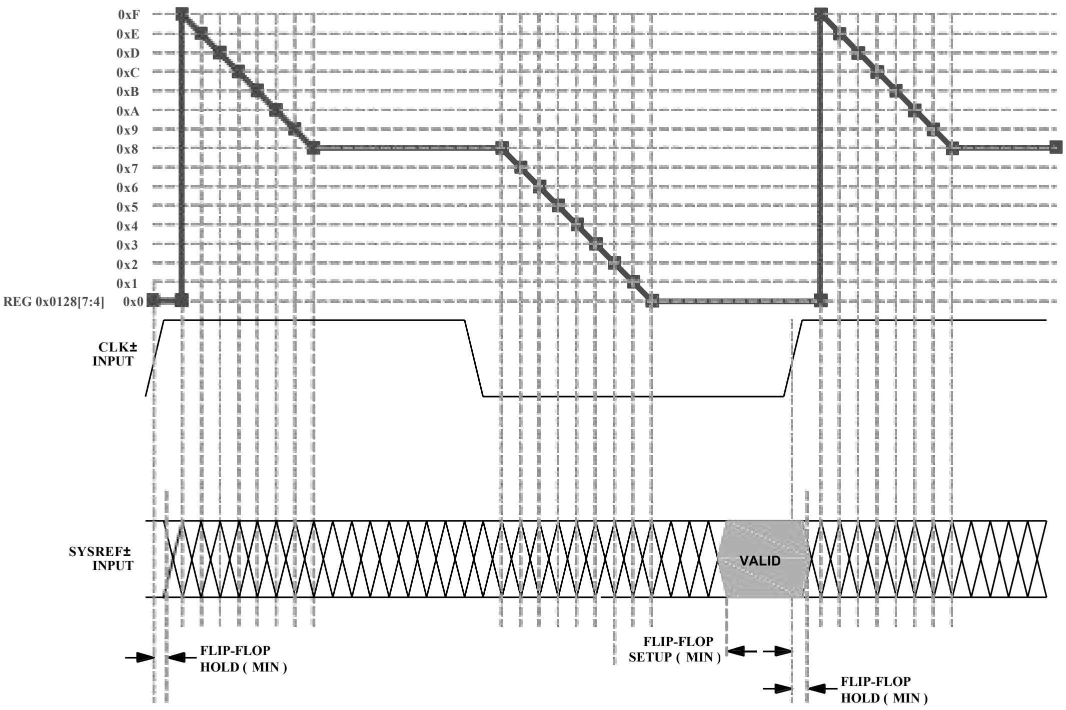


Figure 58 SYSREF ± setup detector



picture 59 SYSREF ± hold detector

surface 30 SYSREF ± Setup / Hold Monitor, Register 0x0128

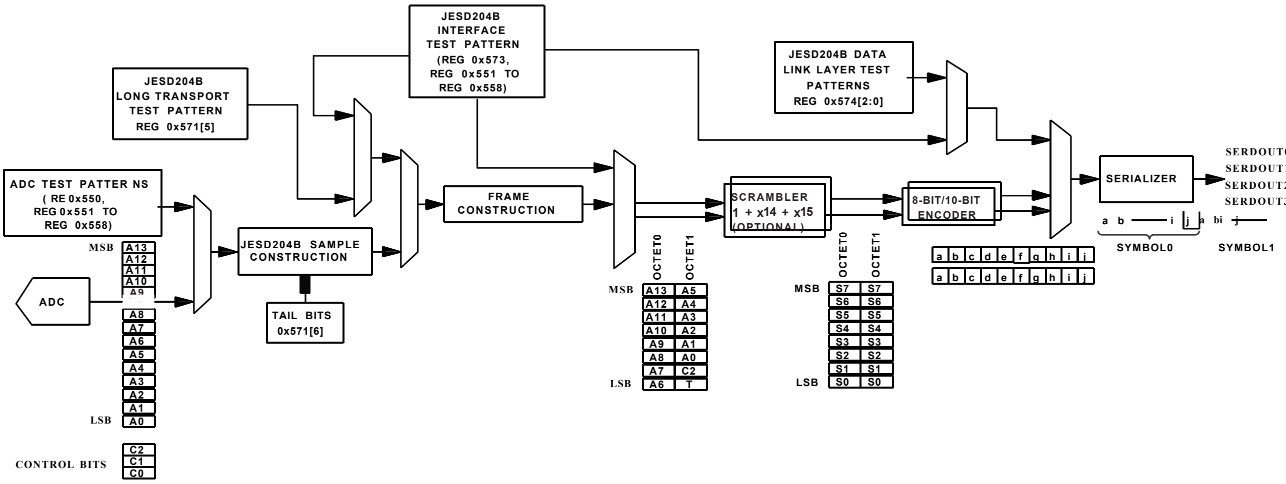
Register 0x0128, Bits[7:4] Hold Status	Register 0x0128, Bits[3:0] Setup Status	Description
0x0	0x0 to 0x7	Possible setup error. The smaller this number, the smaller the setup margin.
0x0 to 0x8	0x8	No setup or hold error (best hold margin).
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin).
0x8	0x0	No setup or hold error (best setup margin).
0x9 to 0xF	0x0	Possible hold error. The larger this number, the smaller the hold margin.
0x0	0x0	Possible setup or hold error.

19. Test Mode

19.1 ADC Test Mode

CW9689 has various test options item , Helpful for system-level applications.
The CW9689 has ADC test modes that can be set in register 0x0550 . Table 31 describes these test modes. When the output test mode is enabled, the analog portion of the ADC is disconnected from the digital backend block and the test mode is run through the output formatting module. Some test modes are affected by the output format, while others are not. The pseudo-random number (PN) generator in the PN sequence test can be reset by setting Bit 4 or Bit 5 of Register 0x0550 . These tests can be run with or without an analog signal. However, these tests require an encode clock.

If the application mode is set to select DDC operating mode, the test mode must be enabled for each enabled DDC . Test mode can be enabled by bits 2 and 0 of registers 0x0327 , 0x0347 , and 0x0367 , depending on the selected DDC . The I channel is used for the test mode selected for channel A , and the Q channel is used for the test mode selected for channel B. For DDC3 only , the I channel is used for the test mode from channel A , and the Q channel does not output the test mode. Bit 0 of register 0x0387 selects the channel A test mode for I data .



picture 60 With data frameADC Output data path

surface 31 ADC Test Mode [1]

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/ Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	N/A	N/A	N/A
0001	Midscale short	0000 0000 0000	N/A	N/A
0010	Positive full-scale short	01 1111 1111 1111	N/A	N/A
0011	Negative full-scale short	10 0000 0000 0000	N/A	N/A
0100	Checkerboard	10 1010 1010 1010	N/A	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	$x23 + x18 + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	$x9 + x5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0C65, 0x0697
0111	One-/zero-word toggle	11 1111 1111 1111	N/A	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x0551 to Register 0x0558	N/A	User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2] … for repeat mode. User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000 … for single mode.
1111	Ramp output	(x) % 214	N/A	$(x) \% 2^{14}$, $(x+1) \% 2^{14}$, $(x+2) \% 2^{14}$, $(x+3) \% 2^{14}$

[1] N/A means not applicable.

19.2 JESD204B Module Test Mode

In addition to the ADC pipeline test modes, the CW9689 also has flexible test modes in the JESD204B block. These test modes can be set in Register 0x0573 and Register 0x0574 . These test patterns can be injected at different locations in the output data path. The test injection points are shown in Figure 60. Table 32 describes the JESD204B block For the CW9689 , transitioning from test mode (register 0x0573 ≠ 0x00) to normal mode (register 0x0573 = 0x00) requires an SPI soft reset, which can be done by writing 0x81 to register 0x0000 (self-clearing). To perform the Bit.

19.2.1. Transport layer sample test mode

The CW9689 implements the transport layer test mode defined in Section 5.1.6.3 of the {JEDEC JESD204B specification}. This test is controlled by register 0x571 [5] . The test sequence is equivalent to the raw sample points from the ADC .

19.2.2. Interface Test Mode

The interface test modes are defined in Register 0x0573 , Bits[3:0] . Table 33 also describes these test modes. Interface tests can be injected at different points in the data . See Figure 60 for more information on the test injection points . Register0x0573 , Bits [5:4] show the injection locations for these test sequences.

Table 34 and Table 35 show some examples of test patterns when JESD204B sample input, physical layer (PHY) 10 -bit input, and scrambler 8 -bit input are injected. UPx in the table indicates a user-defined test sequence.

19.2.3. Data Link Layer Test Mode

The CW9689 data link layer test mode is implemented based on the JEDEC JESD204B specification section 5.3.3.8.2 definition. These tests are defined in register 0x0574 , Bits[2:0] . The inserted test mode is very useful for verifying the functionality of the data link layer. When the data link layer test mode is turned on, Turn SYNCINB ± off by writing 0xC0 to Register 0x0572 .

surface32 JESD 204B interface test mode

Output Test Mode Bit Sequence	Pattern Name	Expression	Default
0000	Off (default)	Not applicable	Not applicable
0001	Alternating checker board	0x5555, 0xAAAA, 0x5555, …	Not applicable
0010	1/0 word toggle	0x0000, 0xFFFF, 0x0000, …	Not applicable
0011	31-bit PN sequence	x31 + x28 + 1	0x0003AFFF
0100	23-bit PN sequence	x23 + x18 + 1	0x003AFF
0101	15-bit PN sequence	x15 + x14 + 1	0x03AF
0110	9-bit PN sequence	x9 + x5 + 1	0x092
0111	7-bit PN sequence	x7 + x6 + 1	0x07
1000	Ramp output	(x) % 216	Ramp size depends on test injection point
1110	Continuous/repeat user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then zeros

surface33 InputM=2 , S=2 , N'=16 (Register0x0573, Bits [5:4] = 'b00)

Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	0	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
1	0	0	0xAAAA	0xFFFF	$(x+1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	0	1	0xAAAA	0xFFFF	$(x+1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	0	0xAAAA	0xFFFF	$(x+1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	1	0xAAAA	0xFFFF	$(x+1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
2	0	0	0x5555	0x0000	$(x+2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	0	1	0x5555	0x0000	$(x+2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	0	0x5555	0x0000	$(x+2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	1	0x5555	0x0000	$(x+2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
3	0	0	0xAAAA	0xFFFF	$(x+3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	0	1	0xAAAA	0xFFFF	$(x+3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	0	0xAAAA	0xFFFF	$(x+3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	1	0xAAAA	0xFFFF	$(x+3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
4	0	0	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	0	1	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	0	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	1	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000

surface34 Physical Layer 10 -bit input (register0x0573 , Bits [5:4] = 'b01)

10-Bit Symbol Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x155	0x000	$(x) \% 2^{10}$	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	$(x + 1) \% 2^{10}$	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	$(x + 2) \% 2^{10}$	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	$(x + 3) \% 2^{10}$	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	$(x + 4) \% 2^{10}$	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	$(x + 5) \% 2^{10}$	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	$(x + 6) \% 2^{10}$	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	$(x + 7) \% 2^{10}$	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	$(x + 8) \% 2^{10}$	0x18E	0x10F	UP1[15:6]	0x000
9	0x2AA	0x3FF	$(x + 9) \% 2^{10}$	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	$(x + 10) \% 2^{10}$	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	$(x + 11) \% 2^{10}$	0x3DD	0x008	UP4[15:6]	0x000

surface35 Scrambler8 -bit input (register0x0573 , Bits [5:4] = 'b10)

8-Bit Octet Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x55	0x00	$(x) \% 2^8$	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	$(x + 1) \% 2^8$	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	$(x + 2) \% 2^8$	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	$(x + 3) \% 2^8$	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	$(x + 4) \% 2^8$	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	$(x + 5) \% 2^8$	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	$(x + 6) \% 2^8$	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	$(x + 7) \% 2^8$	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	$(x + 8) \% 2^8$	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	$(x + 9) \% 2^8$	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	$(x + 10) \% 2^8$	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	$(x + 11) \% 2^8$	0xAC	0xFF	UP4[15:9]	0x00

Table 37 Functional features accessible via SPI

20.Serial interface (SPI)
SPI interface of CW9689 allows the user to configure the converter through the structured register space provided inside the ADC to meet specific functions or operations. SPI is flexible and can be customized according to specific applications. The address space can be accessed and read and written through the serial port. The register space is in bytes and can be further divided into multiple areas. The description of each area is shown in the register map table section.

20.1 Configuration using SPI
The SPI of CW9689 ADC consists of three pins: SCLK pin, SDIO pin and CSB pin (see Table 36). SCLK (Serial Clock) The pin is used to synchronize the data read from the ADC and the data written to the ADC . The SDIO (Serial Data Input / Output) pin is a dual-function pin that can be used to send data to the ADC internal register or read data from the register. The CSB (Chip Select Signal) pin is active low and can enable or disable read and write cycles.

Table 36 Serial port interface pins

Pins	Functional Description
SCLK	Serial Clock. Serial shift clock input,Used for synchronous serial interface read and write operations.
SDIO	Serial data input / output. Dual function pin, usually used as input or output, depending on the instruction sent and the relative position in the timing frame.
CSB	Chip select signal. Low level is effective and is used to select the read and write cycles.

CSB and the rising edge of SCLK together determine the start of the frame. Figure 6 is an example of a serial timing diagram, and the corresponding definitions are shown in Table 5 .
The CSB pin can operate in multiple modes. CSB can be maintained in a low state, so that the device is always enabled; it can also stay in a high level between bytes, which allows other external timing; when the CSB pin is pulled high, the SPI function is in high impedance mode, in which mode, the second function of the SPI pin can be enabled.

All data consists of 8 -bit words. The first bit of each byte of serial data indicates whether a read command or a write command is issued, thus changing the data transmission direction of the SDIO pin from input to output. In addition to the word length, the instruction cycle also determines whether the serial frame is a read or write operation, thereby writing to the chip through the serial port and reading data from the on-chip register. If the instruction is a readback operation, a read operation is performed, and the SDIO pin changes from input to output at the appropriate position in the serial frame.
Data can be sent in MSB first mode or LSB first mode. The default mode is MSB first when powered on , and the data sending mode can be changed through the SPI configuration register.

20.2 Hardware Interface
Table 36 comprise the physical interface between the user programming device and the CW9689 serial interface. When using the SPI interface, the SCLK pin and the CSB pin act as inputs. The SDIO pin is bidirectional and acts as an input pin during the write phase and an output pin during the readback phase. The SPI interface is very flexible and can be controlled by an FPGA or microcontroller. When the converter is required to fully utilize its full dynamic performance, the SPI interface should be disabled. Since the SCLK , CSB , and SDIO signals are usually asynchronous with the ADC clock, Therefore, noise from these signals can degrade the performance of the converter. If the on-board SPI bus is used for other devices, it is recommended to add buffers between this bus and the CW9689 to prevent these signals from changing at the converter input during the critical sampling period.

20.3 SPI Access Characteristics

Table 37 briefly describes the functional features accessible via the SPI . The CW9689 specific device features are detailed in the Register Map Table section .

Table 37 Functional features accessible via SPI

Features	describe
Working Mode	Allows the user to set Power-Down mode or Standby mode.
clock	Allow users to SPI Access the clock divider.
DDC	Allows users to set the decimation filter for different applications.
Test Input / Output	Allows the user to set up test patterns to obtain known data on the output bits.
Output Mode	Allows the user to configure output.
SERDES Output Settings	Allow users to change SERDES set up.

21. Register Map

21.1 Reading the Register Map

Each row in the register map table has 8 bits. The register map is divided into the following sections:

Analog Devices SPI registers (register 0x0000 to register 0x000F)

l Clock /SYSREF/ Chip Power-Down Pin Control Registers (Register 0x003F to Register 0x0201)

l Fast Detection and Signal Monitoring Control Registers (Registers 0x0245 to Register 0x027A)

l DDC function registers (register 0x0300 to register 0x03CD)

l Digital Output and Test Mode Registers (Register 0x0550 to Register 0x05CB)

l Programmable filter control and coefficient registers (Registers 0x0DF8 to Register 0x0F2F , Register 0x2DF8 to Register 0x2F2F)

Table 38 (See Register Map section) Each hexadecimal address shown is recorded The default hexadecimal value for the address is given in the output sampling mode register. Bit 7 (MSB) is the starting bit for the default hexadecimal value. For example, the hexadecimal default value for address 0x0561 (output sampling mode register) is 0x01 , which means bit 0 = 1 and the remaining bits are 0. This setting is the default output format (two's complement). See Table 38 for more information on this and other features .

21.2 Prohibition and reservation

All addresses and bits not included in Table 38 are not currently supported by the CW9689 . Unused bits of an address location should be written with 0 unless the default value is set otherwise. If the entire address is disabled (for example, address 0x0013) , then you should not Write to this address.

21.3 Default Values

After the CW9689 is reset, the key registers will be loaded with default values. Table 38 (Register Map Table) lists the default values of each register.

21.4 Logic Levels

The following is an explanation of the logic level terminology:

l " Set " means " set a bit to logic 1" or " write logic 1 to a bit " .

l " Clear a bit " means " set a bit to logic 0" or " write a logic 0 to a bit" .

l X indicates don't care bit.

21.5 Channel Specific Registers

For some channel setup functions, such as the input buffer control register (0x1A4C), each channel can be set to a different value. In these cases, the channel address is repeated internally for each channel. These registers and corresponding bits are referred to as local registers in Table 38. These local registers and corresponding bits are accessed by setting the Channel A bit or the Channel B bit of register 0x0008 . If both channel bits are set, subsequent write operations affect the registers of both channels. Only one channel (Channel A or Channel B) is allowed to be set to read both registers in one read cycle. A. If these two channel bits are set during an SPI read cycle, The device returns the value of Channel A. The global registers and corresponding bits listed in Table 38 affect the characteristics of the entire device and channels and do not allow each channel to be set separately.

21.6 SPI Soft Reset

performing a soft reset by writing 0x81 to register 0x0000 , CW9689 needs 5ms to recover . Ensure that adequate delay time is programmed into the program firmware after asserting soft reset and before starting device setup.

21.7 Register Map

The detailed register configuration list of the chip is shown in the table below.

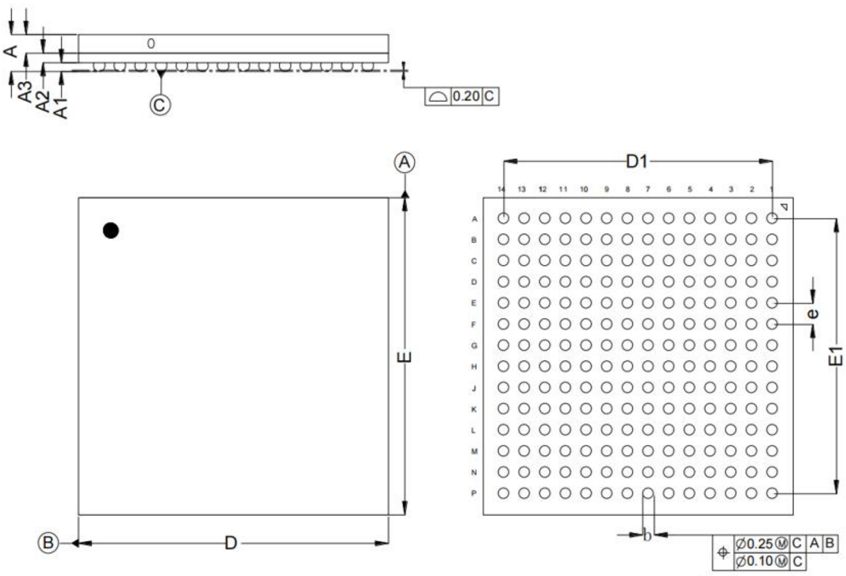
surface 38 Register Map

register address	Register Name	Bit	Bit Name	describe	default value	access type
0x0000	SPI Configuration A	7	Soft reset image (Self-clearing)	After a soft reset, the user must wait 5 ms Only then can other registers be written. 1'b0 : No operation. 1'b1 ： Reset SPI and registers (self -clearing) .	0x0	WC
		6	LSB Priority mirror	1'b1 : For all SPI Operation, LSB First shift. 1'b0 : For all SPI Operation, MSB First shift.	0x0	R/W
		5	Address self-mirror	1'b0 : multi-byte SPI During operation, the address is automatically decremented. 1'b1 : multi-byte SPI During operation, the address is automatically increased.	0x0	R/W
		[4:3]	reserve	reserve.	0x0	R
		2	Add address	1'b0 : multi-byte SPI During operation, the address is automatically decremented. 1'b1 : multi-byte SPI During operation, the address is automatically increased.	0x0	R/W
		1	LSB priority	1'b1 : For all SPI Operation, LSB First shift. 1'b0 : For all SPI Operation, MSB First shift.	0x0	R/W
		0	Soft Reset (Self-clearing)	After a soft reset, the user must wait 5 ms Only then can other registers be written. 1'b0 : No operation. 1'b1 ： Reset SPI and registers (self -clearing) .	0x0	WC
0x0001	SPI Configuration B	[7:2]	reserve	reserve.	0x0	R
		1	Data path soft reset Bit (self-clearing)	1'b0 : Normal operation. 1'b1 : Datapath soft reset (self-clearing).	0x0	WC
		0	reserve	reserve.	0x0	R
0x0002	Chip Configuration	[7:2]	reserve	reserve.	0x0	R
		[1:0]	Channel Power Mode	Channel power mode: 2'b00 : Normal mode (power on). 2'b10 : Standby mode, digital circuit data path clock disabled; JESD 204B interface enabled, normal output. 2'b11 : Power-down mode, digital circuit data path clock disabled, data path The path is held in reset, the JESD 204B interface is shut down, and the outputs are shut down.	0x0	R/W

0x0003	Chip Type	[7:0]	Chip Type	Chip type: high-speed analog-to-digital converter.	0x3	R
0x0004	chipID (LSB)	[7:0]	chipID [7:0]	chipID low byte.	0x00	R
0x0005	chipID (MSB)	[7:0]	chipID [15:8]	chipID High byte.	0x00	R
0x0006	Chip level	[7:4]	Chip speed grade	Chip speed grade: 0x0: 1.3 GSPS .	0x0	R
		[3:0]	reserve	reserve.	0x0	R
0x0008	Chip Channel Index	[7:2]	reserve	reserve.	0x0	R
		1	B aisle	1'b0 : channelB Do not accept the next SPI Order . 1'b1 : Channel B accepts the next SPI Order.	0x1	R/W
		0	A aisle	1'b0 : channelA Do not accept the next SPI Order . 1'b1 : ChannelA accept the next SPI Order.	0x1	R/W
0x000C	ManufacturerID (LSB)	[7:0]	Manufacturer ID [7:0]	ManufacturerID low byte.	0x53	R
0x000D	ManufacturerID (MSB)	[7:0]	Manufacturer ID [15:8]	ManufacturerID High byte.	0x4D	R
0x000F	transmission	[7:1]	reserve	reserve.	0x0	R
		0	Chip transfer	Register transfer bit (self-clearing). DDC The phase update mode is 1(Send Memory 0x0300, Bit 7) , this bit is used to synchronize the update DDC FTW / POW / MAW / MBW Phase increment and phase offset registers, same This bit is also used to update the coefficients of the programmable filter (PFILT) when 1'b0 : No operation. 1'b1 : Self-clearing bit used to synchronize data transfer from the master register to the slave register Remove the position.	0x0	WC

Note: For other register configurations, please contact technical personnel.

22. Package size



Dimension symbol	min	Typ	max	Unit
A	1.18	1.39	1.60	mm
A1	0.28	0.33	0.38	mm
A2	0.33	0.36	0.39	mm
A3	0.70 BASIC			mm
D	11.90	12.00	12.10	mm
D1	10.40 BASIC			mm
E	11.90	12.00	12.10	mm
E1	10.40 BASIC			mm
b	0.40	0.45	0.50	mm
e	0.80BASIC			mm

picture 61 CW9689 Fc - PBGA 196 Package Outline

23. CW9689 and AD 9689 Difference Comparison

1) AVDD 2 voltage pin NC , does not affect the power supply design;

2) Built-in temperature sensor, can directly read digital memory and calculate temperature;

3) Sampling occurs on the rising edge of the clock, but it can also support sampling on the falling edge of the clock, which is configurable ;

4) In full bandwidth mode, overrange function is not supported ;

5) Some addresses of register configuration are different from those of foreign original chips ;