CW10D1000 Data Manual

Dual-Channel 10-Bit, 1.0 GSPS High-Speed ADC

1.0 Overview

The CW10D1000 is a 10-bit high-speed ADC product integrated with two 10-Bit, 1.0 GSPS high-speed ADCs. Each channel ADC features an independent DDR data clock (DCLKI and DCLKQ). When both channel ADCs are operating, DCLKI and DCLKQ are always in phase, allowing data acquisition using either clock for all channels. If the 1:2 Demux mode is selected, an additional set of 10-Bit LVDS buses are enabled, reducing the data rate of each LVDS group to half of that in Non-Demux mode, thereby easing the timing requirements for data capture.

The CW10D1000 supports the AutoSync function, which enables multi-device cascading. It is packaged in a plastic BGA292 package and operates within a temperature range of -55°C to 105°C. This device achieves excellent dynamic performance with low power consumption of less than 2W.The data output format of the CW10D1000 is programmable as either Offset Binary or Two's Complement. It utilizes an LVDS interface compliant with international standards for data transmission, with an adjustable output common-mode voltage selectable between 0.8V and 1.2V.

The CW10D1000 is pin-compatible with the CW10D1500, CW12D1800, CW12D1600, and CW12D1000 series.

2.0 Applications

- RF direct down-conversion
- High-speed data acquisition systems
- Ultra-wideband satellite data reception
- Automatic test equipment
- High-speed testing instruments
- Broadband radar
- Electronic countermeasures

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3.0 Features

- Built-in dual-channel 1.0 GSPS ADCs
- Low power consumption, no heat sink required
- Integrated termination resistors (with automatic calibration) and high-speed buffers
- Test patterns provided for system debugging and batch testing
- 1:1 Non-demuxed or 1:2 Demuxed LVDS data outputs
- Multi-chip automatic synchronization function
- Single 1.9V power supply
- 292-BGA package (27mm × 27mm × 1.7mm, 1.27mm ball pitch)
- Pin-compatible with CW10D1500 / CW12D1800 / CW12D1600 / CW12D1000

4.0 Performance Indicators

- Full Power Bandwidth: 2.4 GHz
- Data Latency: 26 master clock cycles
- Static Performance: DNL -0.8/+1.2 LSB, INL -2.5/+2.8 LSB
- Dynamic Performance (fs = 1.0 GSPS, input signal power -1 dBFS)

  — fin = 100MHz
  ENOB = 8.2 Bit, SFDR = 64.7 dBFS, SNR = 51.4 dBFS
  — fin = 248MHz
  ENOB = 8.1 Bit, SFDR = 62.6 dBFS, SNR = 50.9 dBFS
  — fin = 373 MHz
  ENOB = 8.0 Bit, SFDR = 62.7 dBFS, SNR = 50.2 dBFS
  — fin = 498 MHz
  ENOB = 7.9 Bit, SFDR = 63.3 dBFS, SNR = 49.9 dBFS
  — fin = 750 MHz
  ENOB = 7.7 Bit, SFDR = 63.9 dBFS, SNR = 48.4 dBFS

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5.0 Simplified Block Diagram

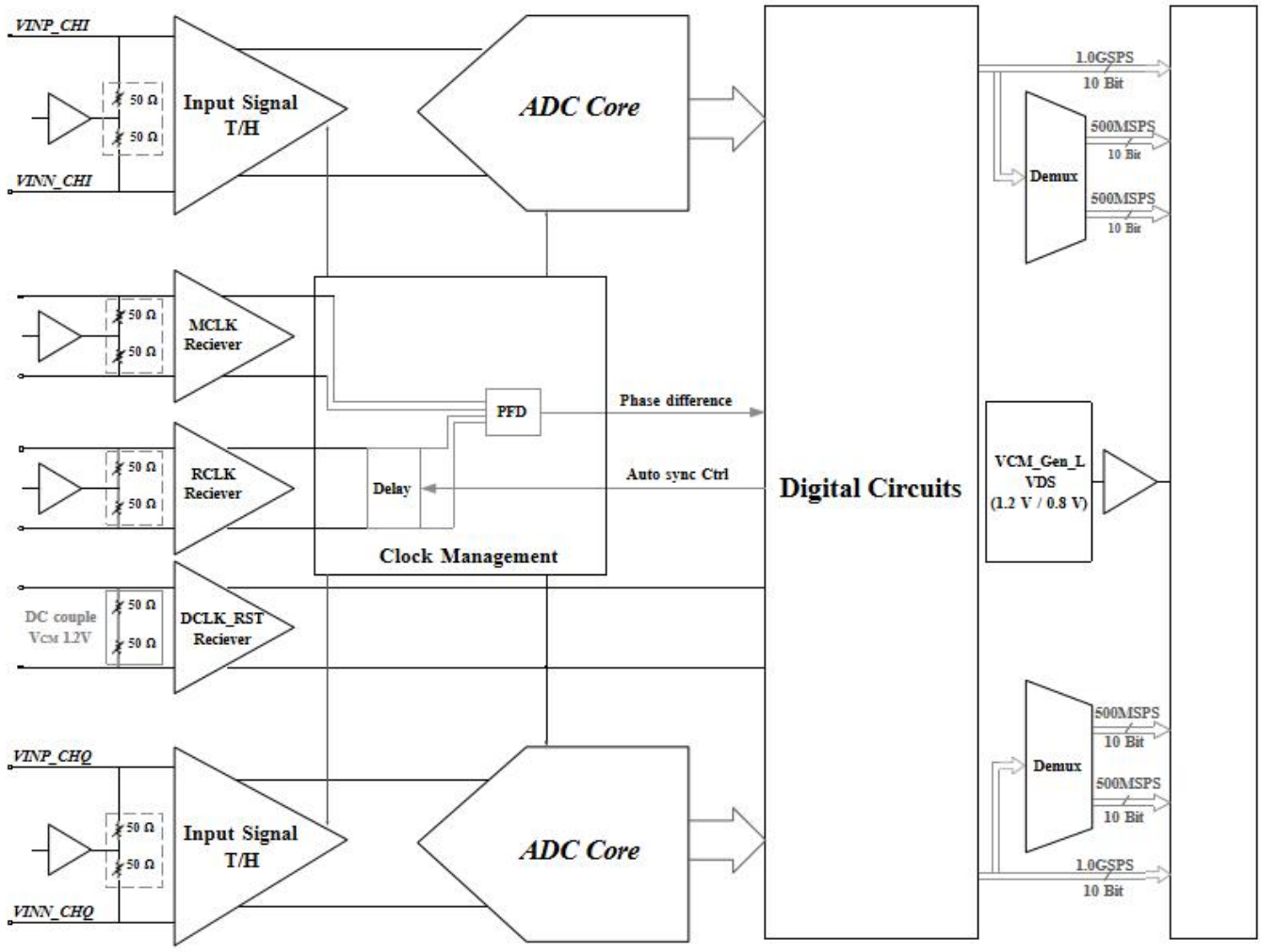

Figure 5.1 System Block Diagram of CW10D1000

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6.0 Typical Performance

Table 6-1 Chip Usage Conditions

Parameters	Symbols	Notes	Value	Unit
Power supply voltage	V_A	Analog circuit power supply	1.9	V
	V_{TC}	Sample-hold and clock circuit power supply	1.9	V
	V_{DR}	Output driver circuit power supply	1.9	V
	V_E	Digital circuit power supply	1.9	V
Power-up sequence		No power-up sequence requirement		
Ground	GND_A	Analog circuit ground	0	V
	GND_{TC}	Sample-hold and clock circuit ground	0	V
	GND_{DR}	Output driver circuit ground	0	V
	GND_E	Digital circuit ground	0	V
Differential input analog signal amplitude (1)	V_{INIP}-V_{ININ} $V_{INQP} - V_{INQN}$	Input signal differential amplitude	600/800	mVpp
Logic input high level	V_{IH}		V_A	V
Logic input low level	V_{IL}		GND	
Clock differential input signal amplitude	$V_{CLKP} - V_{CLKN}$		$400 \le V_{CLKP} - V_{CLKN} \le 2000$	mVpp
Clock frequency	f_{MCLK}		$0.4 \le f_{MCLK} \le 1.0$	GHz
Operating temperature range	T_C		$-55 \le T_C \le 105$	℃

NOTE:

(1) The differential input analog signal amplitude can be adjusted through register 10h, the default is 800mVpp, for specific adjustment, see the register list;

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Table 6-2 Electrical characteristics of power supply, input and output

The following performance indicators are all without power-on calibration (CAL pin connected to "V_A"), the chip works in Non-Demux and Non-DES mode, and $V_A = V_{DR} = V_{TC} = V_E = +1.9V$, AC coupled signal input, unused channel terminal connected to "AC ground", AC coupled sine wave sampling clock, f_{CLK} = 1.0 GHz at 0.6 Vpp (single-ended signal converted to differential signal input through Balun); Rext = Rtrim = 3300 Ω ± 0.1%; input signal source impedance 50 Ω (single-ended signal converted to differential signal input through Balun, 100 Ω is connected in parallel with the chip input on the PCB board to form 50 Ω to match the signal source impedance); T_A = 25 ℃.

Parameter	Symbol	Minimum	Typical value	Maximum value	Unit
Resolution			10		
Power supply voltage:					
Analog circuit power supply	V_A	1.8	1.9	2.0	V
Sampling and holding and clock circuit power supply	V_{TC}	1.8	1.9	2.0	V
Output driver circuit power supply	V_{DR}	1.8	1.9	2.0	V
Digital circuit power supply	V_E	1.8	1.9	2.0	V
Power supply current:					
Analog circuit power supply	I_A		16		mA
Sampling and holding and clock circuit power supply	I_{TC}		544		mA
Output driver circuit power supply	I_{DR}		170		mA
Digital circuit power supply	I_E		185		mA
Power consumption					
PDI = PDQ = GND	P_D		1.74		W
PDI = GND, PDQ = V_A			1.12		W
PDI = V_A, PDQ = GND			1.12		W
PDI = V_A, PDQ = V_A			23		mW
Data input					
Input differential analog signal amplitude	$V_{INIP} - V_{ININ}$ $V_{INQP} - V_{INQN}$		400 400		mVpp mVpp
Differential input resistance	R_{IN}	93	100	103	Ω

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Table 6-2 Electrical characteristics of power supply, input and output (continued)

Parameter	Symbol	Minimum value	Typical value	Maximum value	Unit
Clock input					
Clock source type		Differential sine wave			
Clock input differential swing	$V_{CLKP}-V_{CLKN}$	400	600	2000	mVpp
Clock differential input resistance	R_{MCLK}	95	100	105	Ω
External clock jitter requirement	Jitter			100	fs
Clock duty cycle requirement	Duty Cycle	48	50	52	%
Multi-chip DCLK_RST synchronization signal					
Logic compatibility	LVDS				
Input voltage: Logic low Logic high Swing Common mode voltage Input resistance	 V_{IL_DRST} V_{IH_DRST} V_{ID_DRST} V_{CM_DRST} R_{DRST}	 1.4 	 350 1.20 100	 1.1 	 V V mV V Ω
Multi-chip RCLK synchronization signal					
Logic compatibility	LVDS (supports DC/AC coupling, VCM_RCLK must be connected to the same voltage when AC coupling is used) =High)				
Input voltage: Logic low Logic high Swing Common mode voltage Input resistance	 V_{IL_RCLK} V_{IH_RCLK} V_{ID_RCLK} V_{CM_RCLK} R_{RCLK}	 1.4 	 350 1.20 100	 1.1 	 V V mV V Ω
SPI					
Low level input voltage	V_{IL_SPI}	0		$0.3\times V_A$	V
High level input voltage	V_{IH_SPI}	$0.7\times V_A$		V_A	V
Low level output voltage	V_{OL_SPI}			0.3	V
High level output voltage	V_{OH_SPI}	$0.8\times V_A$			V
Serial clock frequency	f_{SCLK}		15	20	MHz
Digital signal data and data ready output					
Logic compatibility	LVDS				
Output amplitude 50Ω transmission line, 100Ω differential termination Swing (single side) Common mode voltage Aperture delay Output data delay Data output rising edge (5 pF) Data output falling edge (5 pF) Clock data output deviation Clock data setup time (90°) Clock data hold time (90°)	 V_{OD} V_{CM_LVDS} t_{AD} t_{LAT} t_{LHT} t_{HLT} t_{OSK} t_{SU} t_H	 300 290 	 350 1.2 (0.8 optional) 825 26 220 220 650 850	 400 470 	 mVpp V ps Sampling clock period ps ps ps ps ps

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Table 6-3 Static characteristics

Parameter	Symbol	Minimum value	Typical value	Maximum value	Unit
Differential nonlinearity	DNL	-0.84		1.16	LSB
Integral nonlinearity	INL	-2.54		2.85	LSB
Offset error	VOS		5		LSB
Full scale error		-70		68	mV

Table 6-4 Dynamic characteristics

Parameter	Symbol	Minimum value	Typical value	Maximum value	Unit
Full power bandwidth:	FPBW		2.4		GHz
fs = 1.0 Gsps, Vin = -1 dBFS					
Effective number of bits					
fin = 100 MHz	ENOB		8.2		bit
fin = 248 MHz			8.1		bit
fin = 373 MHz			8.0		bit
fin = 498 MHz			7.9		bit
fin = 750 MHz			7.7		bit
Signal-to-noise ratio					
fin = 100 MHz	SNR		51.4		dBFS
fin = 248 MHz			50.9		dBFS
fin = 373 MHz			50.2		dBFS
fin = 498 MHz			49.9		dBFS
fin = 750 MHz			48.4		dBFS
Total Harmonic Distortion					
fin = 100 MHz	|THD|		63.7		dBFS
fin = 248 MHz			61.1		dBFS
fin = 373 MHz			61.5		dBFS
fin = 498 MHz			59.7		dBFS
fin = 750 MHz			61.6		dBFS
Spurious Free Dynamic Range					
fin = 100 MHz	|SFDR|		64.7		dBFS
fin = 248 MHz			62.6		dBFS
fin = 373 MHz			62.7		dBFS
fin = 498 MHz			63.3		dBFS
fin = 750 MHz			63.9		dBFS
Second Harmonic					
fin = 100 MHz	|2nd Harm|		88.4		dBFS
fin = 248 MHz			87.8		dBFS
fin = 373 MHz			83.6		dBFS
fin = 498 MHz			79.5		dBFS
fin = 750 MHz			82.7		dBFS
Third Harmonic					
fin = 100 MHz	|3rd Harm|		74.6		dBFS
fin = 248MHz			70.5		dBFS
fin = 373 MHz			70.6		dBFS
fin = 498 MHz			71.3		dBFS
fin=750MHz			69.2		dBFS

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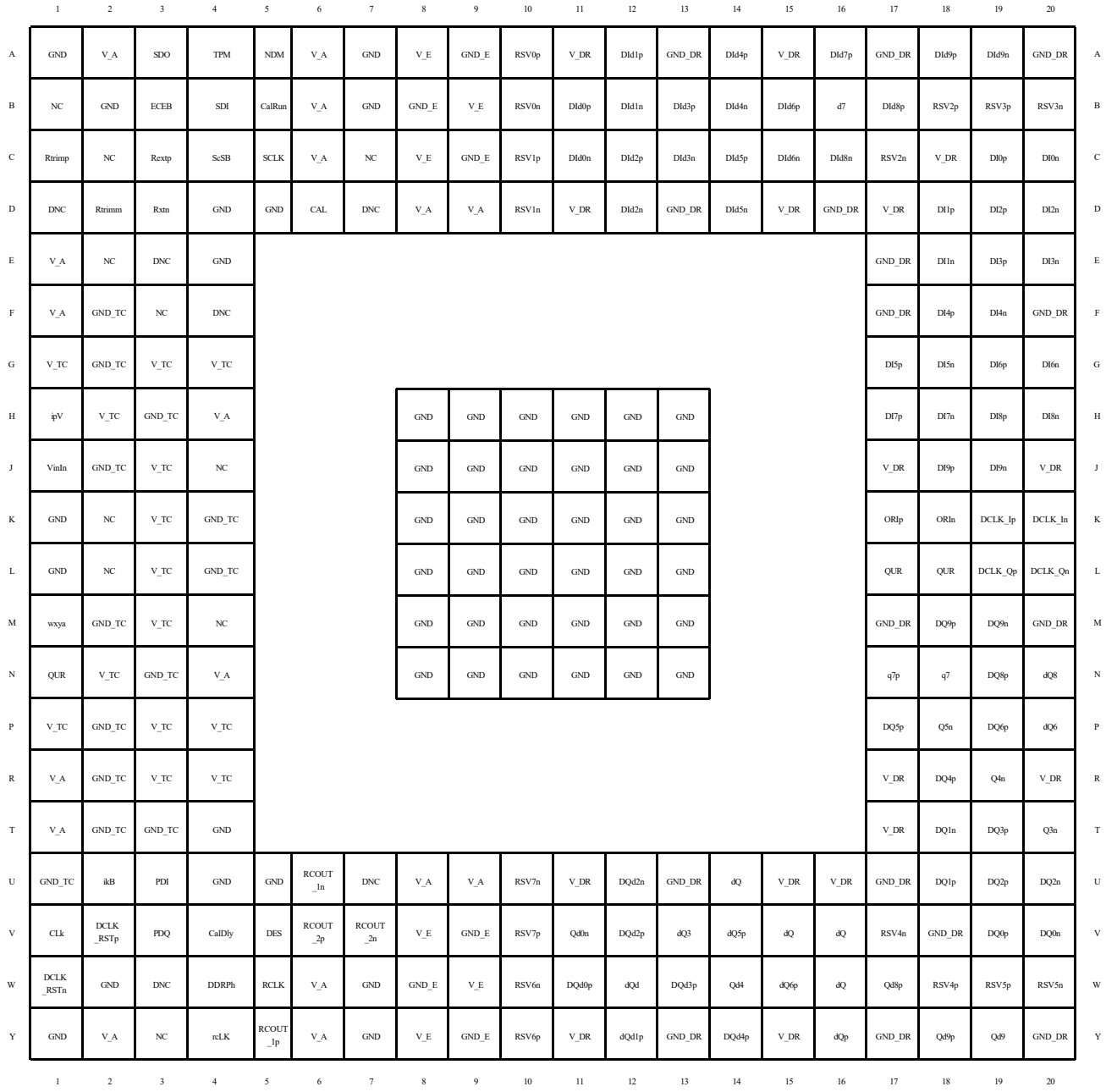
7.0 Pin configuration and functional description



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	V_A	SDO	TPM	NDM	V_A	GND	V_E	GND_E	RSV0p	V_DR	DId1p	GND_DR	DId4p	V_DR	DId7p	GND_DR	DId9p	DId9n	GND_DR	A
B	NC	GND	ECEB	SDI	CalRun	V_A	GND	GND_E	V_E	RSV0n	DId0p	DId1n	DId3p	DId4n	DId6p	d7	DId8p	RSV2p	RSV3p	RSV3n	B
C	Rtrimp	NC	Rextp	ScSB	SCLK	V_A	NC	V_E	GND_E	RSV1p	DId0n	DId2p	DId3n	DId5p	DId6n	DId8n	RSV2n	V_DR	DI0p	DI0n	C
D	DNC	Rtrimm	Rxtn	GND	GND	CAL	DNC	V_A	V_A	RSV1n	V_DR	DId2n	GND_DR	DId5n	V_DR	GND_DR	V_DR	DI1p	DI2p	DI2n	D
E	V_A	NC	DNC	GND													GND_DR	DI1n	DI3p	DI3n	E
F	V_A	GND_TC	NC	DNC													GND_DR	DI4p	DI4n	GND_DR	F
G	V_TC	GND_TC	V_TC	V_TC													DI5p	DI5n	DI6p	DI6n	G
H	ipV	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				DI7p	DI7n	DI8p	DI8n	H
J	VinIn	GND_TC	V_TC	NC				GND	GND	GND	GND	GND	GND				V_DR	DI9p	DI9n	V_DR	J
K	GND	NC	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				ORIp	ORIn	DCLK_Ip	DCLK_In	K
L	GND	NC	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				QUR	QUR	DCLK_Qp	DCLK_Qn	L
M	wxya	GND_TC	V_TC	NC				GND	GND	GND	GND	GND	GND				GND_DR	DQ9p	DQ9n	GND_DR	M
N	QUR	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				q7p	q7	DQ8p	dQ8	N
P	V_TC	GND_TC	V_TC	V_TC													DQ5p	Q5n	DQ6p	dQ6	P
R	V_A	GND_TC	V_TC	V_TC													V_DR	DQ4p	Q4n	V_DR	R
T	V_A	GND_TC	GND_TC	GND													V_DR	DQ1n	DQ3p	Q3n	T
U	GND_TC	ikB	PDI	GND	GND	RCOUT _1n	DNC	V_A	V_A	RSV7n	V_DR	DQd2n	GND_DR	dQ	V_DR	V_DR	GND_DR	DQ1p	DQ2p	DQ2n	U
V	CLk	DCLK _RSTp	PDQ	CalDly	DES	RCOUT _2p	RCOUT _2n	V_E	GND_E	RSV7p	Qd0n	DQd2p	dQ3	dQ5p	dQ	dQ	RSV4n	GND_DR	DQ0p	DQ0n	V
W	DCLK _RSTn	GND	DNC	DDRPh	RCLK	V_A	GND	GND_E	V_E	RSV6n	DQd0p	dQd	DQd3p	Qd4	dQ6p	dQ	Qd8p	RSV4p	RSV5p	RSV5n	W
Y	GND	V_A	NC	rcLK	RCOUT _1p	V_A	GND	V_E	GND_E	RSV6p	V_DR	dQd1p	GND_DR	DQd4p	V_DR	dQp	GND_DR	Qd9p	Qd9	GND_DR	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 7.1 CW10D1000 pinout (top view)

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Table 7-1 Pin Function Description

Pin Number	Symbol	Function
H1, J1 N1, M1	VinIp, VinIn VinQp, VinQn	I/Q channel differential signal input
U2, V1	CLKp, CLKn	Differential sampling clock signal input
V2, W1	DCLK_RSTp, DCLK_RSTn	Differential clock reset. Positive pulse resets DCLKI and DCLKQ Output
D1, D7, E3, F4, W3, U7	DNC	Floating pin, cannot be connected to any potential
B1, C2, C7, E2, F3, J4, K2, L2, M4, Y3	NC	Null pin
C3, D3	Rextp, Rextn	External 3.3kΩ precision resistor port 1
C1, D2	Rtrimp, Rtrimn	External 3.3kΩ precision resistor port 2
Y4, W5	RCLKp, RCLKn	Synchronous reference clock input
Y5, U6 V6, V7	RCOut1p，RCOut1n RCOut2p，RCOut2n	Reference clock output 1 and output 2
V5	DES	Double edge sampling mode selection, when this input is set to logic high, the DES (Double Edge Sample) operating mode will be selected, which means that the I channel and Q channel inputs are sampled in a time-interleaved manner. When this input is set to logic low, the chip is in Non-DES mode, i.e., I and Q channels operate independently. In Extended Control Mode (ECM), this input is ignored and DES mode selection is controlled by the DES bit (address: 0h, bit 7) through the control register; the default is Non-DES mode operation. Pull-down by default inside the chip.
V4	CalDly	Calibration delay selection, pull-down by default inside the chip.
D6	CAL	Calibration cycle initialization (1), pull-up by default inside the chip.

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B5	CalRun	Calibration flag output, this output is logically high power when performing the calibration process. flat. Otherwise this output is logic low. The chip internal drop-down is pulled down by default.
U3 V3	PDI PDQ	I/Q channel shutdown control. Setting any input to logic high will turn off Close the corresponding I or Q channel. Setting either input to logic low will cause the corresponding I or Q channels to enter the operating state after a certain time delay. This pin is valid in both ECM and Non-ECM. In ECM, each pin is logical or operational with its respective bits. Therefore, both the PDI and PDQ bits in the control register can be used to turn off the I and Q channels respectively (address: 0h, bit 11 and bit 10). The chip internal drop-down is pulled down by default.
A4	TPM	Test mode selection, when the input is logic high, the chip continuously outputs a set of repeated fixed digital sequences. In ECM, this input is ignored, and the test mode can only control the register TPM bit (address: 0h, bit 12). The chip internal drop-down is pulled down by default.

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A5	NDM	Non-Demux mode selection, setting this input to logic high will set the digital output bus to 1:1 Non-Demuxed mode. Setting this input to logic low sets the digital output bus to 1:2 Demuxed mode. This function is only controlled by the pin and remains active during ECM and Non-ECM. The chip internal drop-down is pulled down by default.
W4	DDRPh	DDR phase selection. This input selects 0 ° when logic low Data-to-DCLK phase relationship. When logic is high, it selects the 90° Data-to-DCLK phase relationship, i.e. the DCLK conversion indicates the middle of the valid data output. This pin is only available when the chip is in 1:2 Demux mode Effective, i.e. the NDM pin is set to logic low. In ECM, this input is ignored and the DDR phase is selected by the DPS bit (address: 0h, bit 14) through the control register; defaults to 0° mode. The chip internal drop-down is pulled down by default.
B3	ECEb	Extended control enable. When this signal is valid (logic low), extended function control is performed through the SPI interface. In this case, most of the direct control pins do not work. When this signal is invalid (logic high), the SPI interface is disabled, all SPI registers are reset to their default values, and all available settings are controlled through the control pins. Pull-up by default inside the chip.
C4	SCSb	SPI chip select, pull-up by default inside the chip.
C5	SCLK	SPI serial clock, pull-down by default inside the chip.
B4	SDI	SPI serial data input, pull-down by default inside the chip.
A3	SDO	SPI serial data output, pull-down by default inside the chip.
A2, A6, B6, C6, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6	V_A	Analog circuit power supply
G1, G3, G4, H2 J3, K3, L3, M3 N2, P1, P3, P4 R3, R4	V_TC	Sampling and holding and clock circuit power supply
A11, A15, C18 D11, D15, D17 J17, J20, R17 R20, T17, U11 U15, U16, Y11 Y15	V_DR	Output Driver power supply

NOTE:

(1) When the ADC is used normally, the "power-on calibration function" must be turned off, that is, the user must connect the pin "CAL" to "VA".

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Table 7-1 Pin Function Description (Continued)

Pin Number	Symbol	Function
A8, B9, C8, V8 W9, Y8	V_E	Digital Encoding Circuit Power Supply
A1, A7, B2, B7 D4, D5, E4, K1 L1, T4, U4, U5 W2, W7, Y1, Y7	GND	Analog circuit ground
F2, G2, H3, J2 K4, L4, M2, N3 P2, R2, T2, T3 U1	GND_TC	Sample hold and clock circuit ground
A13, A17, A20 D13, D16, E17 F17, F20, M17 M20, U13, U17 V18, Y13, Y17 Y20	GND_DR	Output Driver ground
A9, B8, C9, V9 W8, Y9	GND_E	Digital encoding circuit ground
K19, K20 L19, L20	DCLKIp, DCLKIn DCLKQp, DCLKQn	I/Q channel data clock LVDS Outputs
K17, K18 L17, L18	ORIp, ORIn ORQp, ORQn	I/Q channel over-range LVDS outputs
J18, J19 H19,H20 H17,H18 G19,G20 G17,G18 F18, F19 E19, E20 D19, D20 D18, E18 C19, C20 M18,M19 N19, N20 N17,N18 P19, P20 P17, P18 R18, R19 T19,T20 U19,U20 U18, T18 V19,V20	DI9p, DI9n DI8p,DI8n DI7p,DI7n DI6p,DI6n DI5p,DI5n DI4p,DI4n DI3p,DI3n DI2p, DI2n DI1p, DI1n DI0p, DI0n DQ9p,DQ9n DQ8p,DQ8n DQ7p,DQ7n DQ6p,DQ6n DQ5p,DQ5n DQ4p,DQ4n DQ3p,DQ3n DQ2p,DQ2n DQ1p,DQ1n DQ0p,DQ0n	I/Q channel data LVDS output

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Table 7-1 Pin function description (continued)

Pin number	Symbol	Function
A18, A19	DId9p, DId9n	
B17, C16	DId8p,DId8n	
A16, B16	DId7p,DId7n	
B15, C15	DId6p,DId6n	
C14, D14	DId5p, DId5n	
A14, B14	DId4p, DId4n	
B13, C13	DId3p, DId3n	
C12, D12	DId2p, DId2n	
A12, B12	DId1p, DId1n	
B11, C11	DId0p, DId0n	
Y18, Y19	DQd9p,DQd9n	I/Q channel data delay LVDS output
W17,V16	DQd8p,DQd8n	
Y16,W16	DQd7p,DQd7n	
W15,V15	DQd6p, DQd6n	
V14, U14	DQd5p, DQd5n	
Y14,W14	DQd4p, DQd4n	
W13,V13	DQd3p, DQd3n	
V12, U12	DQd2p, DQd2n	
Y12,W12	DQd1p, DQd1n	
W11,V11	DQd0p, DQd0n	
V10, U10	RSV7p, RSV7n	
Y10, W10	RSV6p, RSV6n	
W19,W20	RSV5p, RSV5n	
W18, V17	RSV4p, RSV4n	Internally reserved ports, external leads floating
B19, B20	RSV3p, RSV3n	
B18, C17	RSV2p, RSV2n	
C10, D10	RSV1p, RSV1n	
A10, B10	RSV0p, RSV0n	

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8.0 Typical performance test curve

The following performance indicators are not enabled for power-on calibration (CAL pin connected to "VA"), the chip works in Non-Demux and Non-DES mode, and $V_A = V_{DR} = V_{TC} = V_E = +1.9V$,

AC coupled signal input, unused channels terminated to "AC ground", AC coupled sine wave sampling clock, f_{CLK} = 1.0 GHz at 0.6 Vpp (single-ended signal converted to differential signal input via Balun); $R_{ext} = R_{trim}$ = 3300 Ω ± 0.1%; input signal source impedance 50 Ω (single-ended signal converted to differential signal input via Balun, 100 Ω in parallel with the chip input on the PCB board forms 50 Ω to match the signal source impedance); TA = 27°C.

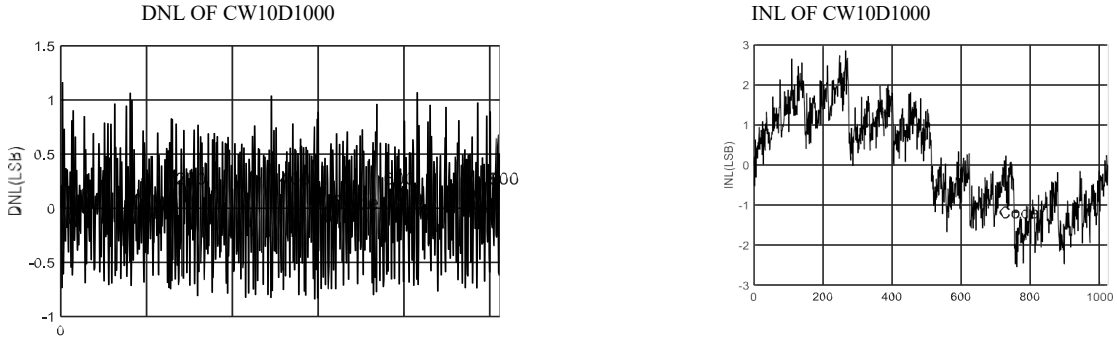
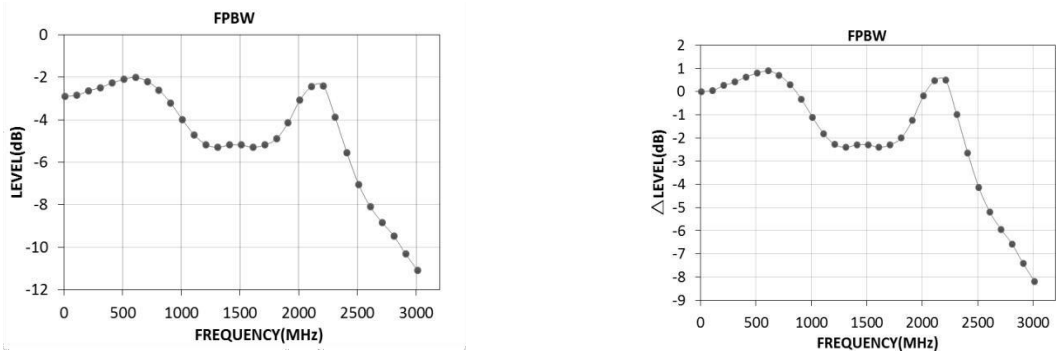
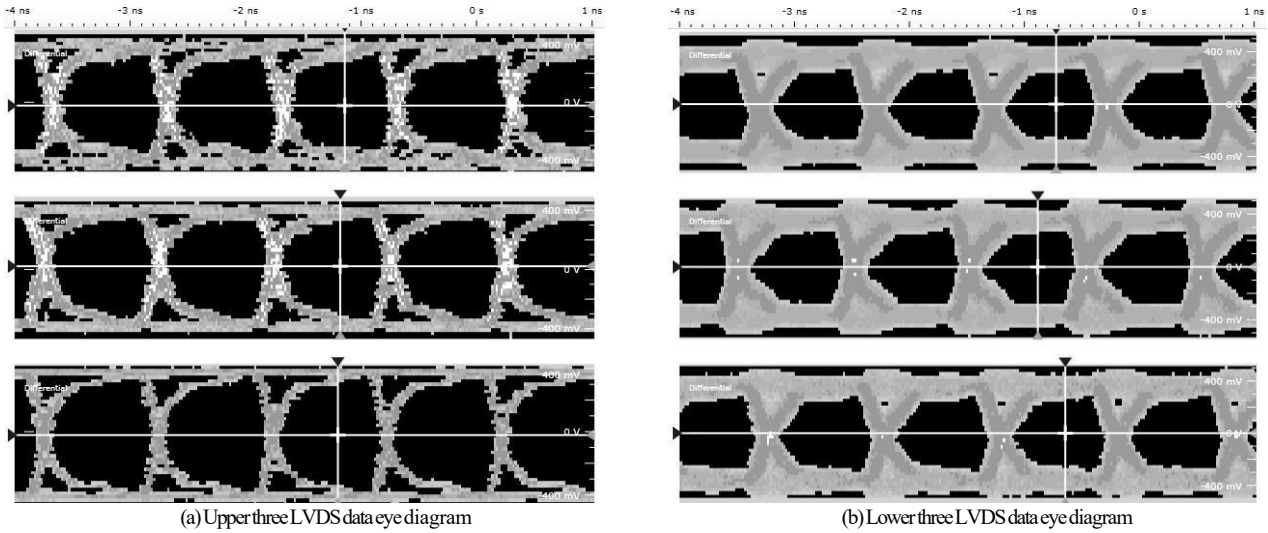


Figure 8.1 CW10D1000 linear error test curve



(a) Absolute amplitude output (b) Normalized amplitude output

Figure 8.2 CW10D1000 full power bandwidth test curve



(a) Upper three LVDS data eye diagram (b) Lower three LVDS data eye diagram

Figure 8.3 CW10D1000 LVDS output eye diagram (fs = 1.0 GHz)

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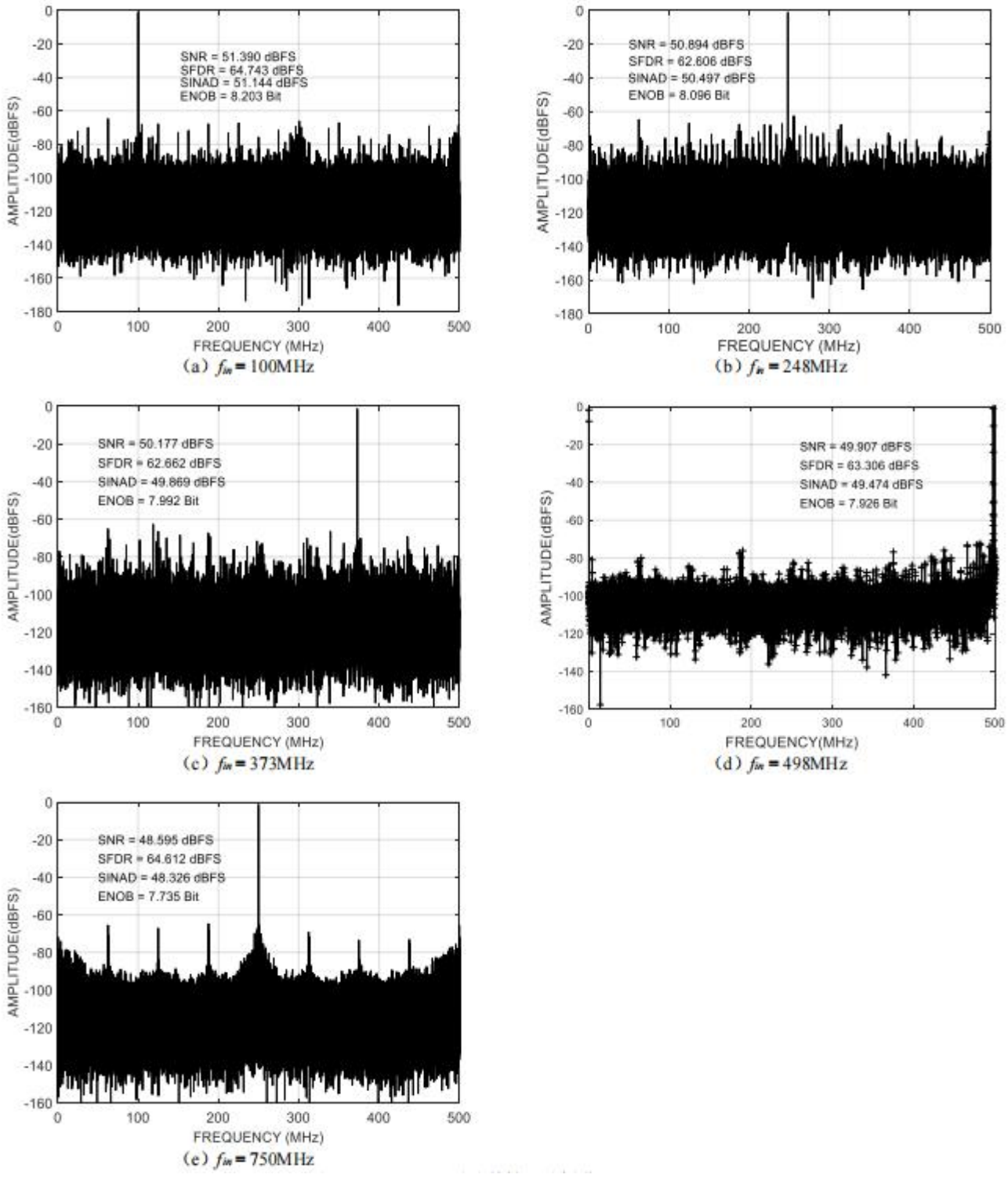

Figure 8.4 Dynamic characteristic test spectrum of CW10D1000 (fs = 1.0GHz)

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9.0 Timing diagram

9.1 Data timing

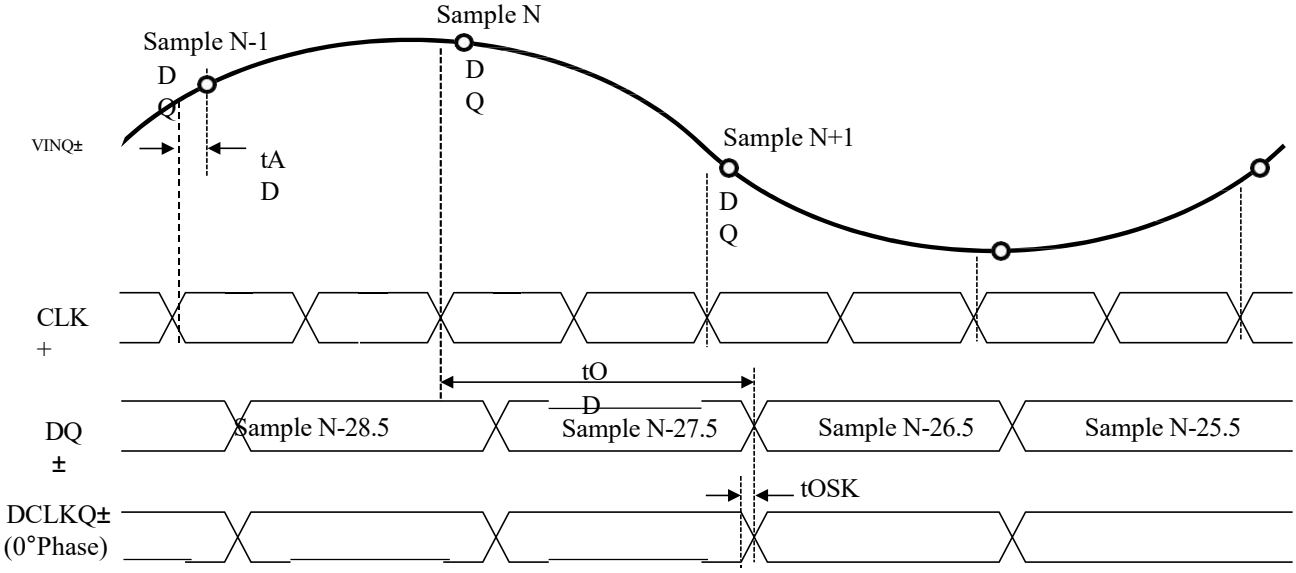

Figure 9.1 CW10D1000 data timing in Non-Demux Non-DES mode

NOTE: The I channel data timing is exactly the same as the Q channel

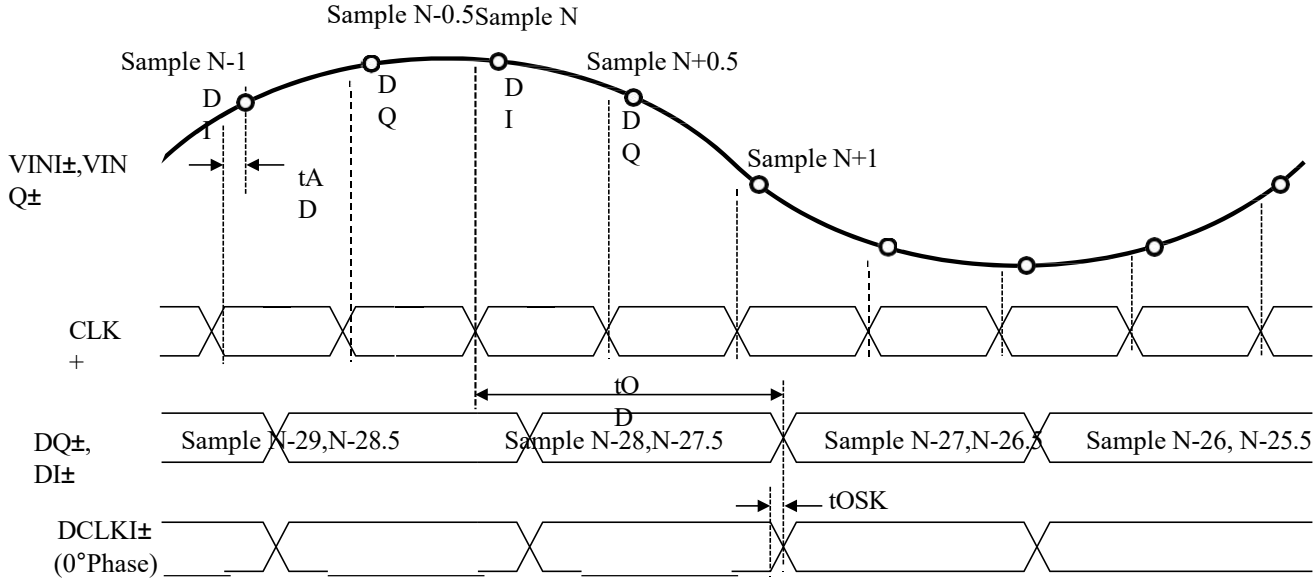

Figure 9.2 CW10D1000 data timing in Non-Demux DES mode

NOTE: In this mode, $V_{IN}I\pm$ and $V_{IN}Q\pm$ must be "short-circuited" at the ADC input;

I channel input is sampled on the rising edge of CLK, and Q channel input is sampled on the falling edge of CLK;

I channel output delay 26.5 cycles, Q channel output delay 27 cycles;

Data is output on both edges of DCLK, the time sequence is DQ, DI (F_{DCLK} = 1/2 F_S)

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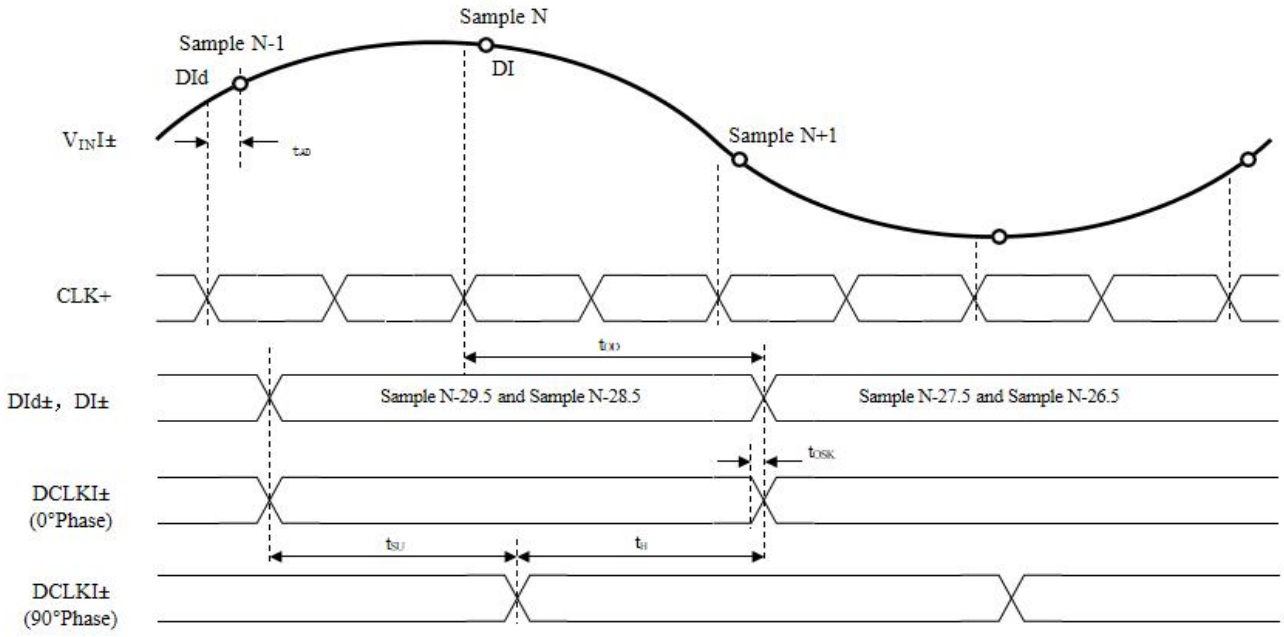

Figure 9.3 CW10D1000 data timing in 1:2 Demux Non-DES mode

NOTE: I channel input is sampled on the rising edge of CLK;

I channel output is delayed by 26.5 cycles;

Data is output on both edges of DCLK, the time sequence is DId, DI (F_{DCLK}= 1/4 F_S)

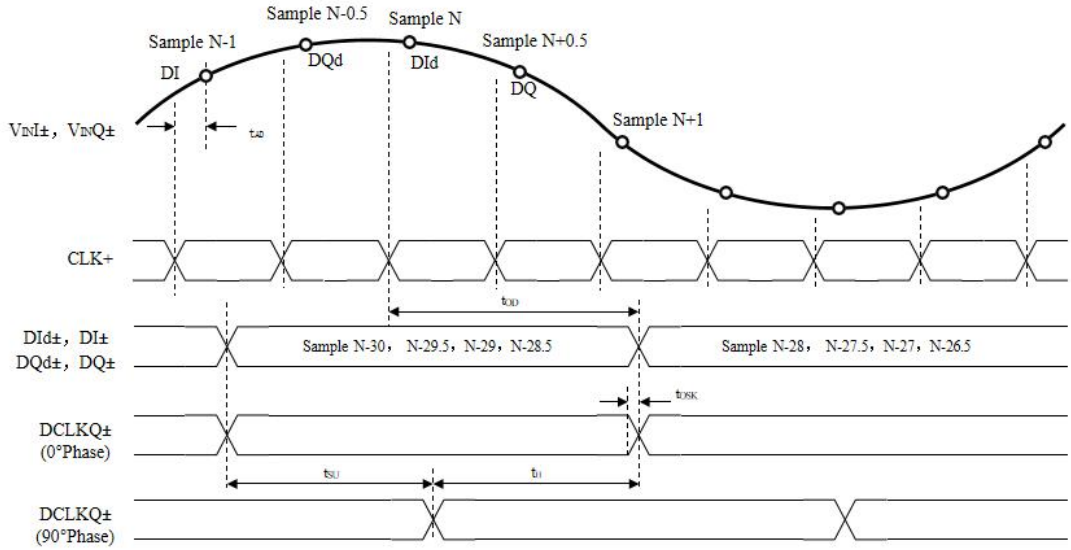

Figure 9.4 CW10D1000 data timing in 1:4 Demux DES mode NOTE: In this mode, VINI± and VINQ± must be "short-circuited" at the ADC input;

I channel input is sampled on the rising edge of CLK, Q channel input is sampled on the falling edge of CLK;

channel output delay 26.5 Cycles, Q channel output delay 27 cycles;

Data is output on both edges of DCLK, the time sequence is DQ, DI (FDCLK = 1/4 F_S)

9.2 SPI interface timing

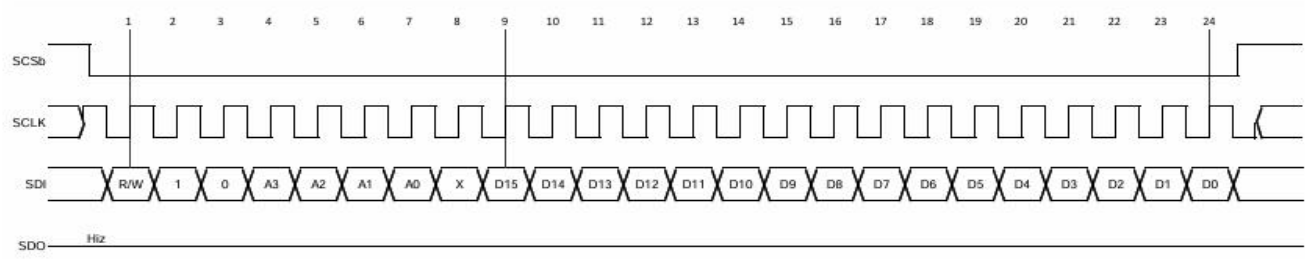

Figure 9.5 SPI write protocol

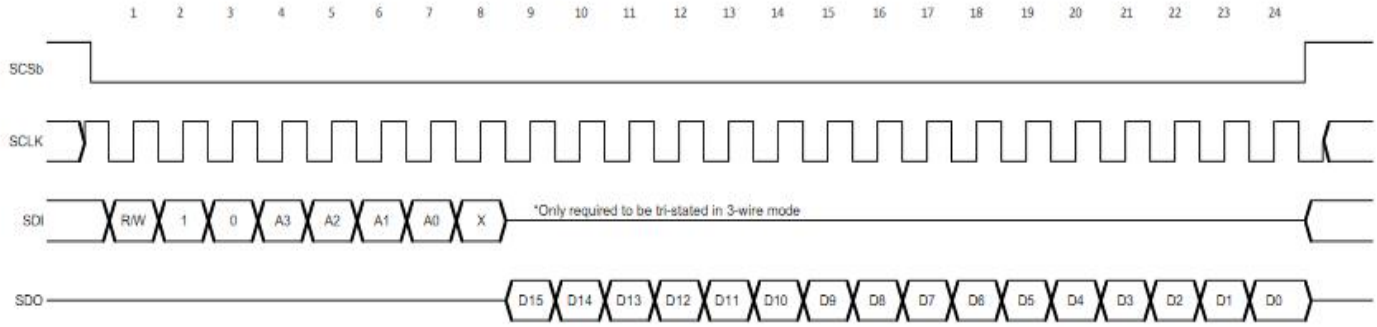

Figure 9.6 SPI read protocol

Table 9.1 SPI interface command and data field definition

Bit	Definition	Description
1	Read/write control bit	1b: read operation 0b: write operation
2~3	Reserved	Need to be set to 10b(1)
4~7	Address bit A[3:0]	16 register addresses, address order is MSB first
8	X	Reserved
9~24	Data bit D[15:0]	Data write or read from register

NOTE:
(1) For register address 0h~Fh, need to be set to 10, this chip also has some extended registers, not subject to this limitation;

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10.0 Encapsulation information

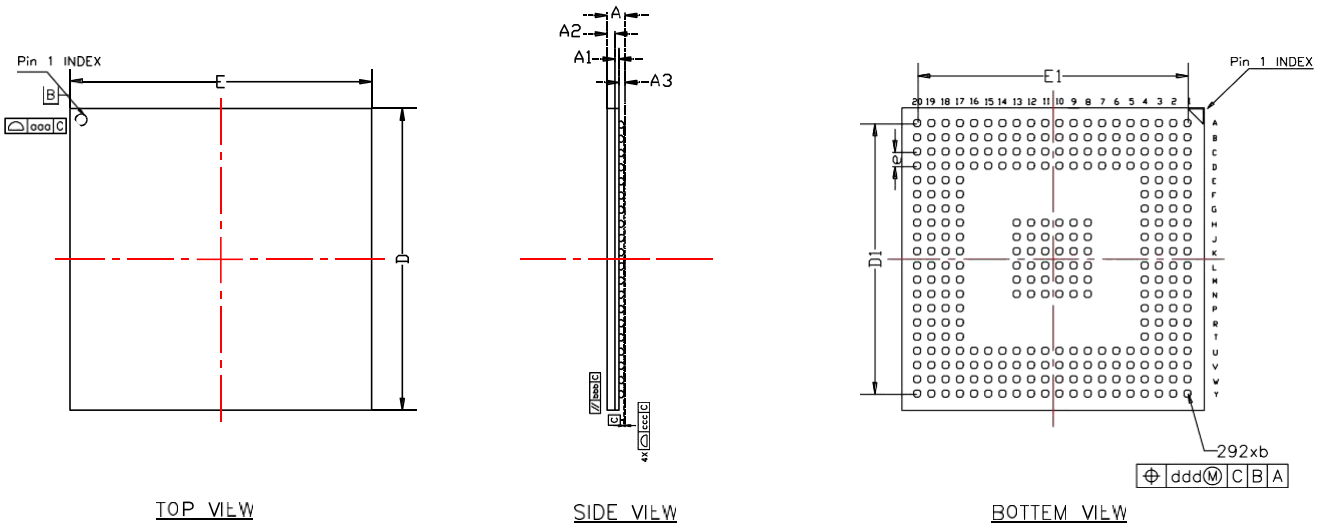

Figure 10.1 CW10D1000 Package Profile

Table 10.1 CW10D1000 Package Dimensions

Size symbol	Unit: mm		
	Minimum	typical	maximum
A	1.56	1.66	1.76
A1	0.32	0.36	0.40
A2	-	0.7	-
A3	0.55	0.6	0.65
D	-	27.0	-
E	-	27.0	-
D1	-	24.13	-
E1	-	24.13	-
e	-	1.27	-
b	0.71	0.76	0.81

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11.0 Multi-chip synchronization function

The CW10D1000 has two synchronization functions (AutoSync and DCLK Reset) for multiple ADC chips. Among them, the AutoSync function has two working modes: master-slave and full-slave. It is recommended to use full-slave mode. All CW10D1000 is used as Slave ADCs. The clock board provides the synchronous clock RCLK (CLK/16) driven by contour lines.

RCLKp/RCLKn realizes synchronization of multiple CW10D1000s. In order to synchronize the DCLK (including data) of multiple ADCs, all DCLKs must be in phase, as CW10D1000 The DCLK of the chip is generated by the RCLK inside the chip and is re-timed through the main clock CLK. Therefore, the CLK signals of multiple ADCs are required to be in phase, that is, the main clock CLK reaches each CW10D1000.

The moment is consistent. The AutoSync function must be enabled through the control register.

The following figure shows an example of two Slave ADC synchronization, where DCLKI and DCLKQ are not distinguished and are both represented by DCLK. The following figure shows an example of two Slave ADC synchronization, where DCLKI and DCLKQ are not distinguished and are both represented by DCLK.

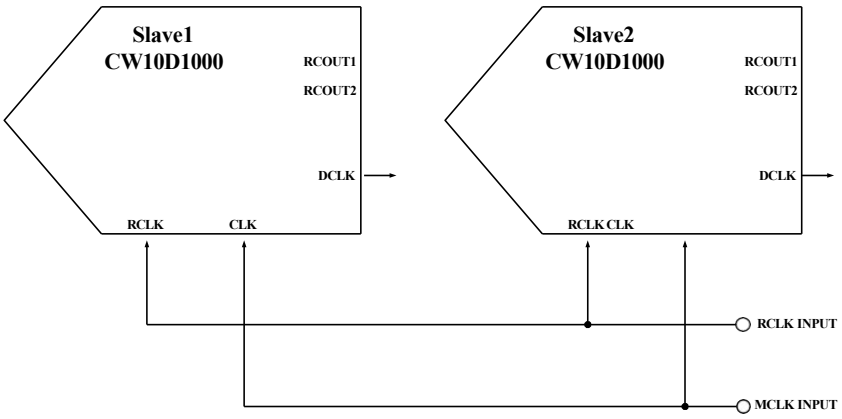

Figure 11.1 Example of CW10D1000 AutoSync function connection

The DCLK Reset function is consistent with AutoSync, but has stricter requirements on the timing of use, so it is not recommended to use this function for multi-chip synchronization. The default configuration of CW10D1000 does not enable this function.

If the AutoSync and DCLK Reset functions are not used, it is recommended to connect the unused PINs according to the following table.

Table 11.1 PIN connection suggestions when CW10D1000 does not use AutoSync and DCLK Reset functions

Port	Connection suggestions
RCLKp/RCLKn	Floating
RCOUT_1p/RCOUT_1n	Floating
RCOUT_2p/RCOUT_2n	Floating
DCLK_RSTp	Connect to GND through a 1kΩ resistor
DCLK_RSTn	Connect to VA through a 1kΩ resistor

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12.0 Register List

Configuration Register 1

Addr: 0h (0000b)									POR state: 2000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAL	DPS	OVS	TPM	PDI	PDQ	Res	LFS	DES	DEQ	DIQ	2SC	Res			
POR	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	CAL, calibration enable bit Setting CAL=1 will trigger a calibration process. Since this control bit will not be automatically cleared, when the user triggers calibration, CAL=0 must be set in advance. This control bit and the CAL pin can both trigger the calibration process. They are functionally "OR" relationships, and there is no polarity requirement between them.
Bit 14	DPS, DDR phase difference selection bit When DPS=0, the DDR Data-to-DCLK phase relationship is 0°When DPS=1, the DDR Data-to-DCLK phase relationship is 90°In Non-Demux mode, this bit setting is invalid
Bit 13	OVS, output voltage selection bit When OVS=0, low voltage level, 0.8vWhen OVS=1, high voltage level, 1.2v This control bit selects different voltages for the LVDS output pins (DATA, OR and DCLK)
Bit 12	TPM, test mode enable bit When TPM=0, normal working mode When TPM=1, the device's LVDS output pins (Digital DATA, OR) will continuously output a fixed digital pattern
Bit 11	PDI, I channel power-off enable bit When PDI=0, I channel is in normal working mode. When PDI=1, I channel is in shutdown working mode This control bit and PDI pin are functionally "OR" relationship. As long as any signal is valid (high level), I channel will be in power-off mode
Bit 10	PDQ, Q channel power-off enable bit When PDQ=0, Q channel is in normal working mode. When PDQ=1, Q channel is in shutdown working mode This control bit and PDQ pin are functionally "OR" relationship. As long as any signal is valid (high level), Q channel will be in power-off mode
Bit 9	Reserved
Bit 8	LFS, reserved word, Reserved
Bit 7	DES, dual-edge sampling enable bit When DES=0, the device works in single-edge sampling mode (Non-DES Mode) When DES=1, the device works in dual-edge sampling mode (DESIQ Mode), and the I- and Q-inputs need to be shorted together.
Bit 6	DEQ, reserved word, Reserved
Bit 5	DIQ, reserved word, Reserved
Bit 4	2SC, binary complement enable bit When 2SC=0, the LVDS data output format is offset binary format (Offset Binary format) When 2SC=1, the LVDS data output format is binary complement format (Two's Complement format)
Bit 3:0	Reserved

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VCMO configuration word (reserved word)

Addr: 1h (0001b)																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res								VCA<2:0>			Res				
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:8	Reserved															
Bit 7:5	VCA<2:0>, reserved word, Reserved															
Bit 4:0	Reserved															

I Channel Offset Configuration Word

Addr: 2h (0010b)																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM<11:0>											
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:13	Reserved															
Bit 12	OS, direction of offset When OS=0, Bits 11:0 represent the positive offset of ADC output. When OS=1, Bits 11:0 represent the negative offset of ADC output.															
Bit 11:0	OM, offset size 1/4 LSB															

Reserved word

Addr: 3h (0011b)																POR state: F771h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1
Bit 15:0	Reserved															

Calibration configuration word

Addr: 4h (0100b)																POR state: 0200h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res	CCS	Res				CMS<1:0>		SSC	Res						
POR	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Bit 15	Reserved															
Bit 14	CCS, reserved word, Reserved															
Bit 13:10	Reserved															
Bit 9:8	CMS, calibration time selection bit Used to select the time length of the internal calibration sequence 00b: 0.8*107 sampling clock cycles 01b: 1.5*107 sampling clock cycles 10b: 2.4*107 sampling clock cycles 11b: 2**25 sampling clock cycles															
Bit 7	SSC, SPI write enable bit When SSC=0, the user is prohibited from changing the calibration value (stored in 05h and 06h) When SSC=1, the user is allowed to change the calibration value (stored in 05h and 06h)															
Bit 6:0	Reserved															

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I channel calibration value

Addr: 5h (0101b)																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SS<15:0>															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:0	SS, I channel calibration value, only writeable, not readable															

Q channel calibration value

Addr: 6h (0110b)																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SS<15:0>															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 3:0	SS, Q channel calibration value, only writable, not readable															

I channel aperture delay adjustment control word

Addr: 7h (0111b)																POR state: 0600h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res				MAM<1:0>		FAM<9:0>									
POR	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
Bit 15:12	Reserved															
Bit 11:10	MAM<1:0>: medium adjustment control bit, I channel and Q channel are adjusted simultaneously and synchronized with 1Eh<5:4>, adjustment range is 66ps, four configurations in total, 22ps as one step															
Bit 9:10	FAM<9:0>: fine adjustment control bit, I channel and Q channel are adjusted simultaneously, adjustment range is 30ps, 30fs as one step															

Q channel aperture delay adjustment control word

Addr: 8h (1000b)																POR state: 0600h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res				MAM<1:0>		FAM<9:0>									
POR	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
Bit 15:12	Reserved															
Bit 11:10	MAM<1:0>: Medium adjustment control bit, I channel and Q channel are adjusted at the same time and synchronized with 1Eh<5:4>, adjustment range is 66ps, four configurations in total, 22ps as a step															
Bit 9:10	FAM<9:0>: Fine adjustment control bit, I channel and Q channel are adjusted at the same time, adjustment range is 30ps, 30fs as a step															

Reserved Word

Addr: 9h (1001b)																POR state: F771h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1
Bit 15:0	Reserved															

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Q channel offset configuration word

Addr: Ah (1010b)																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM<11:0>											
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:13	Reserved															
Bit 12	OS, direction of offset When OS=0, Bits 11:0 represent the positive offset of ADC output. When OS=1, Bits 11:0 represent the negative offset of ADC output															
Bit 11:0	OM, size of offset 1/4 LSB															

Reserved word

Addr: Bh (1011b)																POR state: F771h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1
Bit 15:0	Reserved															

Reserved word

Addr: Ch (1100b)																POR state: F771h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1
Bit 15:0	Reserved															

Reserved word

Addr: Dh (1101b)																POR state: F771h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1
Bit 15:0	Reserved															

Automatic synchronization control word

Addr: Eh (1110b)																POR state: 0003h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRC<9:0>										Res	SP<1:0>		ES	DOC	DR
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit 15:6	DRC, internal delay control word of reference clock RCLK Bit 15:12, Reserved Bit 11:8, 16 configurations in total, 50ps per step Bit 7:6, Reserved															
Bit 5	Reserved															
Bit 4:3	SP, select phase Used to select the phase difference of the reference clock RCLK 00b: 0˚ 01b: 90˚ 10b: 180˚ 11b: 270˚															
Bit 2	ES, slave enable bit When ES=0, the device works in the host mode When ES=1, the device works in the slave mode															
Bit 1	DOC, disable the output of the reference clock RCLK When DOC=0, enable the output of the reference clock RCLK of the two ports RCOut1/2. When DOC=1, disable the output of the reference clock RCLK of the two ports RCOut1/2.															
Bit 0	DR, disable the DCLK_RST function When DR=0, enable the DCLK_RST function. When DR=1, disable the DCLK_RST function.															

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Reserved word

Addr: Fh (1111b)																POR state: F771h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1
Bit 15:0	Reserved															

Extended register

Full-scale voltage configuration word

Addr: 10h (01_0000b)																POR state: 0788h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res												FA			FS
POR	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0
Bit 15:4	Reserved															
Bit 3:1	FA<2:0>: Full-scale range adjustment, adjustment is based on the selected range, the adjustment range is 28mV, 4mV is a step, used in conjunction with FS setting															
Bit 0	FS: Full-scale voltage selection, the default value is 0 when FS=0, the full-scale voltage is 800mVpp when FS=1, the full-scale voltage is 600mVpp															

Aperture delay coarse adjustment configuration word

Addr: 11h (01_0001b)																POR state: 0F0Fh
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM<3:0>				Res							STA	Res		ES	Res
POR	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Bit 15:12	CAM<3:0>: Aperture delay coarse adjustment control, adjustment range 825ps, 55ps as a step, used with STA, when STA is 1, aperture delay coarse adjustment control is enabled															
Bit 11:5	Reserved															
Bit 4	STA: Aperture delay coarse adjustment selection, default value is 0 When STA is 0, aperture delay coarse adjustment control is not enabled When STA is 1, aperture delay coarse adjustment control is enabled															
Bit 3:2	Reserved															
Bit 1	ES: Sampling clock (MCLK) edge selection, the default value is 1 When ES is 0, select the sampling clock falling edge When ES is 1, select the sampling clock rising edge															
Bit 0	Reserved															

Aperture delay synchronization control word

Addr: 1Eh (01_1110b)																POR state: 03D0h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res										MAM<1:0>		Res			
POR	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0
Bit 15:6	Reserved															
Bit 5:4	MAM<1:0>: Medium adjustment control bit, synchronized with 7h and 8h<11:10>, adjustment range 66ps, a total of four configurations, 22ps for a step															
Bit 3:0	Reserved															

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Reserved word

Addr: Fh (1111b)									POR state: F771h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1
Bit 15:0	Reserved															

Extended register

Full-scale voltage configuration word

Addr: 10h (01_0000b)									POR state: 0788h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res												FA			FS
POR	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	0
Bit 15:4	Reserved															
Bit 3:1	FA<2:0>: Full-scale range adjustment, adjustment is based on the selected range, the adjustment range is 28mV, 4mV is a step, used in conjunction with FS setting															
Bit 0	FS: Full-scale voltage selection, the default value is 0 when FS=0, the full-scale voltage is 800mVpp when FS=1, the full-scale voltage is 600mVpp															

Aperture delay coarse adjustment configuration word

Addr: 11h (01_0001b)									POR state: 0F0Fh							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAM<3:0>				Res							STA	Res		ES	Res
POR	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Bit 15:12	CAM<3:0>: Aperture delay coarse adjustment control, adjustment range 825ps, 55ps as a step, used with STA, when STA is 1, aperture delay coarse adjustment control is enabled															
Bit 11:5	Reserved															
Bit 4	STA: Aperture delay coarse adjustment selection, default value is 0 When STA is 0, aperture delay coarse adjustment control is not enabled When STA is 1, aperture delay coarse adjustment control is enabled															
Bit 3:2	Reserved															
Bit 1	ES: Sampling clock (MCLK) edge selection, the default value is 1 When ES is 0, select the sampling clock falling edge When ES is 1, select the sampling clock rising edge															
Bit 0	Reserved															

Aperture delay synchronization control word

Addr: 1Eh (01_1110b)									POR state: 03D0h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res										MAM<1:0>		Res			
POR	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0
Bit 15:6	Reserved															
Bit 5:4	MAM<1:0>: Medium adjustment control bit, synchronized with 7h and 8h<11:10>, adjustment range 66ps, a total of four configurations, 22ps for a step															
Bit 3:0	Reserved															

ChengduCuiweiElectronicCo., LTD E-mail: sales @ cdcwtec.com
Address:No 5,Gaopeng East Road, Gaoxin District, Chengdu, China Website:www.cdcwtec.com