CW12DL3200 Data Sheet

V1.0

Dual Channel 12- bit , 3.2 GSPS high speed ADC

1 Overview

CW12DL3200 is a 12 -bit high-speed ADC product with two built-in 12-Bit , 3.2 GSPS high-speed ADCs . Each channel ADC has an independent DDR data clock. When both channel ADCs are working, If Demux-by-1 mode (LDEMUX=0) is used, only LVDSBUSA and LVDS BUSB are needed to collect all data. If Demux-by-2 mode (LDEMUX=1) is selected, all LVDSBUSA/B/C/D buses will be used, so that the data rate of each LVDS group changes to 1/2 of that in Demux-by-1 mode , which can reduce the timing requirements for data capture. CW12DL3200 achieves excellent dynamic performance with low power consumption of less than 2W .

CW12DL3200 has a unique 5.0 GSPS single-channel working mode. In this mode, the user does not need to adjust the interleaving related parameters, which is convenient for users to use and obtain excellent performance.

CW12DL3200 can be programmed into offset binary code and complement code, and uses LVDS interface that complies with international standards to output data, with an output common mode of 1.2V .

of CW12DL3200 is -55 ℃ ~ 105 ℃ , and it is pin-compatible with ADC12DL3200 .

2 application

- RF Direct Down Conversion
- High-speed data acquisition system
- Ultra-wideband satellite data reception
- Automatic test equipment
- High speed test equipment
- Broadband radar
- Electronic Countermeasures

3 Features

- Built-in dual channel3.2 GSPS ADC
- Support single channel5.0 GSPS Working Mode
- Low power consumption, no heat sink required
- Built-in terminal resistor, high-speed buffer
- Provides test sequences for system commissioning and batch testing
- Single power supply 1.9 V power supply
- FCBGA -256 (17 mm × 17 mm × 1.36 mm, 1 mm Ball spacing)

4 Performance Indicators

- Data Delay: 30 master clock cycles (LALIGNED = 0)
- Full Power Bandwidth: 4. 0GHz
- Static performance: DNL -0.4/+0.4 LSB, INL -1.8/+2.0 LSB
- Dynamic performance (f_s = 3.2 GSPS , input signal power -1 dBFS ）

— f_{in} = 347 MHz

ENOB = 8.4 Bit， SFDR = 70.8 dBFS， SNR = 52.1 dBFS

— f_{in} = 997MHz

ENOB = 8.3 Bit， SFDR = 67.9 dBFS， SNR = 51.9 dBFS

— f_{in} = 2482 MHz

ENOB = 8.1 Bit， SFDR = 62.4 dBFS， SNR = 50.4 dBFS

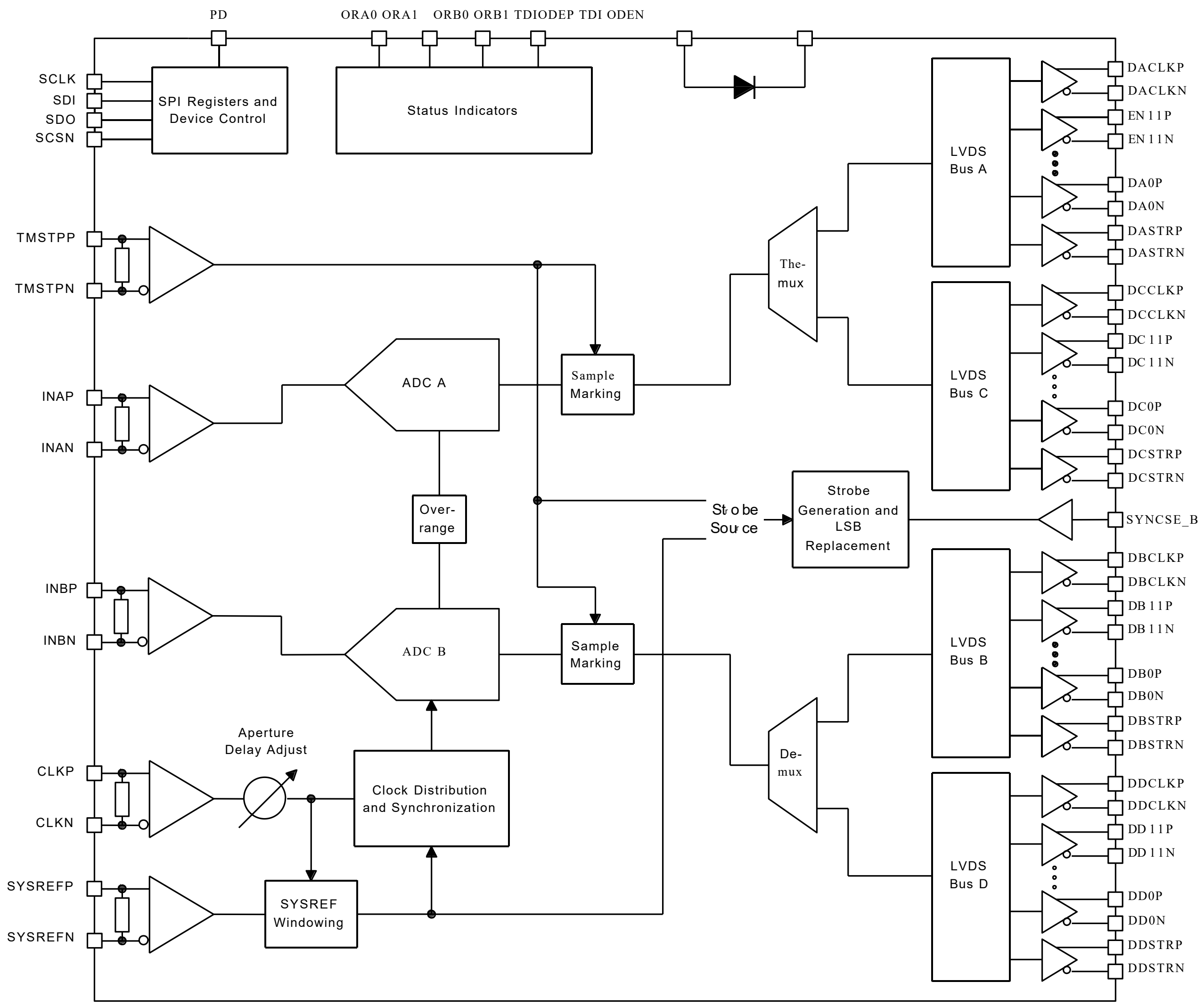
— f_{in} = 4997 MHz

ENOB = 7.5 Bit， SFDR = 56.5 dBFS， SNR = 47.0 dBFS

— f_{in} = 6250 MHz

ENOB = 7.2 Bit， SFDR = 52.7 dBFS， SNR = 45.1 dBFS

5 Simplified Block Diagram



picture 1 CW12DL3200 System Block Diagram

6 Typical Performance

surface 1. Chip usage conditions

parameter	symbol	Notes	Numeric	unit
Supply voltage	VA 19	Analog circuit power supply	1.9	V
	VD 19	Digital circuit power supply	1.9	V
	VLVDS	Digital interface power supply	1.9	V
Recommended power-on sequence		suggestion VA 19 Power on first. VD 19 and VLVDS After power on		
land	AGND	Analog circuit ground	0	V
	AGND_SYS	SYSREF Circuit Ground	0	V
	DGND	Digital circuit ground	0	V
Differential input analog signal amplitude	V_{INAP} —V_{INAN} V_{INBP} —V_{INB}	Input signal differential amplitude	800	mV_{PP}
Logic input high	V_{I}		VD 19	V
Logic input low	V_{IL}		DGND	
Clock differential input signal amplitude	V_{CLKP} —V_{CLKN}		1	V_{PP}
Clock frequency	f_{MCLK}	Dual Channel 3.2 GSPS	$0.4 \leq f_{MCLK} \leq 3.2$	GHz
		Single Channel 5.0 GSPS	$0.4 \leq f_{MCLK} \leq 5.0$	GHz
Operating temperature range	T_A		$-55 \leq T_A \leq 105$	℃

surface 2 Electrical characteristics of power supply, input and output

The chip works on LDEMUX = 1 and DES_EN = 0 mode , and VA 19 = VD 19 = VLVDS = +1.9V , AC Coupled signal input, unused channels terminated with “ AC land " , AC Coupled sine wave sampling clock , f_{CLK} = 3.2 GHz @1 V_{PP} (Single-ended signal through 1:2 Balun Convert to differential signal input) ; Input signal source impedance 50 Ω (single-ended signal through 1:2 Balun Convert to differential signal input) ; T_A = 25℃ .

parameter	symbol	Minimum	Typical Value	Maximum	unit
Resolution			12		
Supply voltage: Analog circuit power supply Digital interface power supply Digital circuit power supply	VA 19 VLVDS VD 19	1.8 1.8 1.8	1.9 1.9 1.9	2.0 2.0 2.0	V V V
Supply Current: Analog circuit power supply Digital interface power supply Digital circuit power supply	I_A I_{LVDS} I_D		98 270 565		mA mA mA
Power consumption PD = GND PD = VD 19	P_D		1.8 23		W mW
Signal input					
Input differential analog signal amplitude	V_{INAP} —V_{INAN} V_{INBP} —V_{INB}		800 800		mV_{PP} mV_{PP}
Input common mode voltage	V_{CMI}		1.3		V
Differential input resistance	R_{IN}	100	105	110	Ω
Clock Input(Not supported DC coupling)					
Clock source type		Differential sine wave			
Clock input differential swing	V_{CLKP} —V_{CLKN}	0.8	1	1.2	V_{PP}
Clock differential input resistance	R_{CLK}	95	100	105	Ω
Clock differential input common mode voltage	V_{CM_CLK}		0.7		V
External clock jitter requirements	Jitter			50	fs
Clock duty cycle requirements	Duty Cycle	40	50	60	%

surface 3 Electrical Characteristics of Power Supply, Input, and Output (Continued)

Multi-chip SYSREF Synchronous signal(Not supported DC coupling)					
Logical compatibility	LVDS				
Input Voltage:					
Logic Low	V_{IL_SYSREF}			1.1	V
Logic High	V_{IH_SYSREF}	1.4			V
Swing	V_{ID_SYSREF}	500	800		mV
Common mode voltage	V_{CM_SYSREF}		1.20		V
Input resistance	R_{SYSREF}		100		Ω
SPI					
Low level input voltage	V_{IL_SPI}	0		0.3 × VD 19	V
High level input voltage	VIH_SPI	0.7 × VD 19		VD 19	V
Low level output voltage	V_{OL_SPI}			0.3	V
High level output voltage	V_{OH_SPI}	0.8 × VD 19			V
Serial clock frequency	f_{SCLK}		10		MHz
Digital Signal LVDS Output					
Logical compatibility	LVDS				
50Ω transmission line, 1 00Ω Differential Termination					
Swing (one side)	VOD	300	350	400	mV_{PP}
Common mode voltage	V_{CM_LVDS}		1.2		V
Output data delay	t_{LAT}				
LALIGNED = 0			30		Sampling clock period
LALIGNED = 1			38		Sampling clock period
Clock data output deviation (within group)	$t_{SKEW(SAME)}$		100		ps
Clock data output deviation (between groups)	$t_{SKEW(ALL)}$		200		ps
Data output rising edge (20 pF)	t_H		220		ps
Data output falling edge (20 pF)	t_{HLT}		220		ps

surface4 Static characteristics

parameter	symbol	Minimum	Typical Value	Maximum	unit
Differential Nonlinearity	DNL	-0.4		0.4	LSB
Integral Nonlinearity	INL	-1.8		2	LSB

surface5 Dynamic characteristics (f_S = 3.2 GSPS , $fCLK$ = 3.2 GHz, dual channel mode)

parameter	symbol	Minimum	Typical Value	Maximum	unit
Full power bandwidth (-3 dB)			4.0		GHz
Channel isolation (interference channel input =400 MHz, -1 dBFS)			-98		dB
Noise spectral density (no input)			-145		dBFS/Hz
f_s = 3.2 GSPS, V_{in} = -1 dBFS					
Number of effective digits	ENOB				
fin = 347 MHz			8.4		bits
fin = 997 MHz			8.3		bits
fin = 2482 MHz			8.1		bits
fin = 4997 MHz			7.5		bits
fin = 6250 MHz			7.2		bits
Signal-to-noise ratio	SNR				
f_{in} = 347 MHz			52.1		dBFS
f_{in} = 997 MHz			51.9		dBFS
f_{in} = 2482 MHz			50.4		dBFS
f_{in} = 4997 MHz			47.0		dBFS
f_{in} = 6250 MHz			45.1		dBFS
Spurious Free Dynamic Range	| SFDR |				
fin = 347 MHz			70.8		dBFS
fin = 997 MHz			67.9		dBFS
fin = 2482 MHz			62.4		dBFS
fin = 4997 MHz			56.5		dBFS
fin = 6250 MHz			52.7		dBFS
Total Harmonic Distortion	| THD |				
fin = 347 MHz			72.3		dBFS
fin = 997 MHz			70.0		dBFS
fin = 2482 MHz			66.8		dBFS
fin = 4997 MHz			61.0		dBFS
fin = 6250 MHz			59.6		dBFS
Second Harmonic	| 2nd Harm |				
fin = 347 MHz			80		dBFS
fin = 997 MHz			75		dBFS
fin = 2482 MHz			72		dBFS
fin = 4997 MHz			62		dBFS
fin = 6250 MHz			60		dBFS
Third harmonic	| 3rd Harm |				
fin = 347 MHz			74		dBFS
fin = 997 MHz			70		dBFS
fin = 2482 MHz			67		dBFS
fin = 4997 MHz			60		dBFS
fin = 6250 MHz			58		dBFS

Note: The above test results are based on our laboratory test environment.

surface 6 Dynamic characteristics (f_s = 5.0 GSPS , f_{CLK} = 5.0 GHz, single channel mode)

parameter	symbol	Minimum	Typical Value	Maximum	unit
Full power bandwidth (-3 dB)			4.0		GHz
Noise spectral density (no input)			-145		dBFS/Hz
f_s = 5.0 GSPS, V_{in} = -1 dBFS					
Number of effective digits	ENOB				
f_{in} = 347 MHz			8.2		bits
f_{in} = 997 MHz			8.2		bits
f_{in} = 2482 MHz			8.0		bits
f_{in} = 4997 MHz			7.6		bits
f_{in} = 6250 MHz			7.2		bits
Signal-to-noise ratio	SNR				
fin = 347 MHz			51.3		dBFS
fin = 997 MHz			51.5		dBFS
fin = 2482 MHz			50.0		dBFS
fin = 4997 MHz			47.7		dBFS
fin = 6250 MHz			46.1		dBFS
Spurious Free Dynamic Range	| SFDR |				
fin = 347 MHz			67.5		dBFS
fin = 997 MHz			68.7		dBFS
fin = 2482 MHz			64.7		dBFS
fin = 4997 MHz			58.0		dBFS
fin = 6250 MHz			52.9		dBFS
Total Harmonic Distortion	| THD |				
fin = 347 MHz			74.6		dBFS
fin = 997 MHz			68.4		dBFS
fin = 2482 MHz			66.9		dBFS
fin = 4997 MHz			62.7		dBFS
fin = 6250 MHz			52.1		dBFS
Second Harmonic	|2nd Harm|				
f_{in} = 347 MHz			75		dBFS
f_{in} = 997 MHz			72		dBFS
f_{in} = 2482 MHz			66		dBFS
f_{in} = 4997 MHz			64		dBFS
f_{in} = 6250 MHz			60		dBFS
Third harmonic	| 3rd Harm |				
fin = 347 MHz			73		dBFS
fin = 997 MHz			70		dBFS
fin = 2482 MHz			63		dBFS
fin = 4997 MHz			62		dBFS
fin = 6250 MHz			58		dBFS

Note: The above test results are based on our laboratory test environment.

7 Pin Configuration and Function Description

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	AGND	AGND	AGND	INAP	INAN	AGND	AGND	ORA1	0P	0N	DA 6P	DA 6N	DC 0P	DC 0N	DGND DGND	
B	DNC	DNC	AGND	AGND	AGND	AGND	AGND	ORA0	DA 1P	DA 1N	7P	DA 7N	DC 1P	DC 1N	DC 7P	DC 7N
C	AGND AGND		AGND	AGND	AGND	AGND	AGND ORB1		DA 2P	DA 2N	DA 8P	DA 8N	DC 2P	DC 2N	DC 8P	DC 8N
D	TMSTPP	DNC	AGND	AGND	AGND	AGND	DGND	ORB0	DA3P	DA3N	DA9P	DA9N	DC3P	DC3N	DC9P	DC9N
E	TMSTPN	SYNCSE _B	AGND	NC	NC	NC	DGND	NC	DA4P	DA4N	DA10P	DA10N	DC4P	DC4N	DC10P	DC10N
F	AGND	AGND	NC	NC	NC	NC	DGND	NC	DA5P	DA5N	DA11P	DA11N	DC5P	DC5N	DC11P	DC11N
G	AGND	AGND	VA19	VA19	VD19	VD19	DGND	NC	DACLKP	DACLKN	VLVDS	VLVDS	DC 6P	DC6N	DCCLKP	DCCLKN
H	CLKP	AGND	VA19	VD19	CEO1 9	VD19	DGND	DGND	DASTRP	DASTRN	VLVDS	VLVDS	VLVDS	DGND	DCSTRP	DCSTRN
J	CLKN	AGND	VA19	VD19	CEO1 9	CEO1 9	DGND	DGND	DBSTRP	DBSTRN	VLVDS	VLVDS	VLVDS	DGND	DDSTRP	DDSTRN
K	AGND	AGND	VA19	VA19	VD19	VD19	DGND	NC	DBCLKP	DBCLKN	VLVDS	VLVDS	DD6P	DD6N	DDCLKP	DDCLKN
L	AGND	AGND	NC	NC	NC	NC	DGND	NC	DB5P	DB5N	DB11P	DB11N	DD5P	DD5N	DD11P	DD11N
M	SYSREF P	TDIODEP	AGND_S YS	NC	NC	NC	DGND	NC	DB4P	DB4N	DB10P	DB10N	DD4P	DD4N	DD10P	DD10N
N	SYSREF N	TDIODEN	AGND_S YS	AGND	AGND	AGND	DGND	SDO	DB3P	DB3N	DB9P	DB9N	DD3P	DD3N	DD9P	DD9N
P	AGND	AGND	AGND	AGND	AGND	AGND	AGND	SDI	DB2P	DB2N	DB8P	DB8N	DD2P	DD2N	DD8P	DD8N
R	PD	AGND	AGND	AGND	AGND	AGND	AGND	SCSN	DB1P	DB1N	DB7P	DB7N	DD1P	DD1N	DD7P	DD7N
T	AGND	AGND	AGND	INBP	INBN	AGND	AGND	SCLK	DB0P	DB0N	DB6P	DB6N	DD0P	DD0N	DGND	DGND

picture2 CW12DL3200 Pinout (top view)

Note: In order to ADC 12 DL 3200 hold PIN to PIN compatible,CW12DL3200 Reserved VA 11 、 VD 11 two groups PIN foot(marked NC ）, but CW12DL3200 The internal circuit does not require these two sets of power supplies. CW12DL3200 These two sets of power supplies can be disconnected at this time.

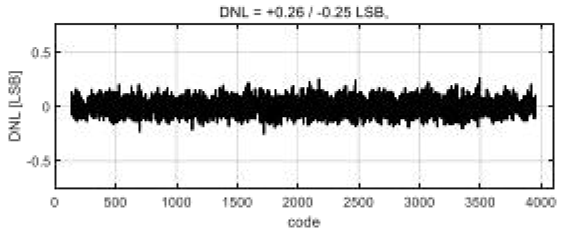
surface 7 Pin Function Description

Pin number	symbol	Function
A4 , A5 T4 , T5	INAP, INAN INBP, INBN	aisleA/B analog signal differential input.
H1 , J1	CLKP, CLKN	Sampling Clock Signal Differential Input.
D1 , E1	TMSTPP , TMSTP N	Timestamp differential input.
M1 , N1	SYSREFP , SY SREFN	SYSREF Differential input for multi-chip synchronization function.
E2	SYNCSE _B	Digital interface synchronous control terminal, CMOS Level, low level is effective , the chip internal default Pull up.
M2 , N2	TDIODEP , TDIODEN	Temperature sensor diode anode and cathode. enter 100uA When the current is (Temperature /℃) =-677.34*X (Diode voltage) +540.78 .
B1 , B2 , D2	DNC	Floating feet,When using, please be careful not to connect to any potential.
R1	PD	Turn off all analog circuitry and LVDS Output, high level is valid , the chip is pulled down by default.
R8	SCS _N	SPI Chip select, the chip is pulled up by default.
T8	SCLK	SPI Serial clock, the chip is pulled down by default .
P8	SDI	SPI Serial data input, the chip is pulled down by default.
N8	SDO	SPI Serial data output
G3 , G4 , H3 , J3 , K3 , K4	VA 19	1.9V analog power supply
G5 , G6 , H4 , H5 , H6 , J4 , J5 , J6 , K5 , K6	VD 19	1.9V Digital Power
G11 , G12 , H11 , H12 , H13 , J11 , J12 , J13 , K11 , K12	VLVDS	1.9 V LVDS Digital interface power supply
E4 , E5 , E6 , E8 , F3 , F4 , F5 F6 , F8 , G8 , K8 , L3 , L4 , L5 , L6 , L8 , M4 , M5 , M6 , M8	NC	Empty pin (corresponding to ADC 12 DL 3200 of VA 11 and VD 11, CW12DL3200 internal The circuit does not need VA 11 , VD 11 these two power supplies)
A1 A2 A3 A6 A7 B3 B4 B5, B6, B7, C1, C2, C3, C4, C5, C6 , C7 , D3 , D4 , D5 , D6 , E3 , F1, F2, G1, G2, H2, J2, K1, K2, L1, L2, N4, N5, N6, P1, P2, P3, P4, P5, P6, P7, R2, R3, R4, R5, R6 , R7 , T1 , T2 , T3 , T6 , T7	AGND	Analog circuit ground
N3 , M3	AGND_SYS	SYSREF Analog circuit ground, connected AGND
A15 , A16 , D7 , E7 , F7 , G 7 , H7 , H8 , H14 , J7 , J8 , J14 , K7 , L7, M7 , N7 , T15 , T16	DGND	Digital power ground
A8 , B8 C8 , D8	ORA 1 , ORA 0 ORB 1 , ORB 0	A channel fast over-amplitude detection status bit (threshold OVR _T1/ OVR _T0) B channel fast over-amplitude detection status bit (threshold OVR _T1/ OVR _T0)
H9 , H10 J9 , J10 H15 , H16 J15 , J16	DASTRP , DASTRN DBSTRP , DBSTRN DCSTRP , DCSTRN DDSTRP , DDSTRN	LVDS A bus strobe Differential output LVDS B bus strobe Differential output LVDS C bus strobe Differential output LVDS D bus strobe Differential output
G9 , G10 K9 , K10 G15 , G16 K15 , K16	DACLKP , DACLKN DBCLKP , DBCLKN DCCLKP , DCCLKN DDCLKP , DDCLKN	LVDS A Bus data and clock differential output LVDS B Bus data and clock differential output LVDS C Bus data and clock differential output LVDS D Bus data and clock differential output
A9 , A10 B9 , B10 C9 , C10 D9 , D10 E9 , E10 F9 , F10 A11 , A12	0P , DA 0N DA 1P , DA 1N DA 2P , DA 2N DA 3P , DA 3N 4P , DA 4N DA 5P , DA 5N DA 6P , DA 6N	LVDS A Data bus differential output

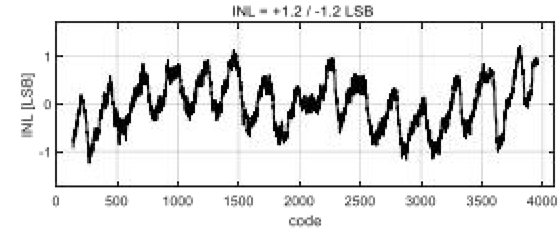
B11 , B12 C11 , C12 D11 , D12 E11 , E12 F11 , F12	7P , DA 7N DA 8P , DA 8N DA 9P , DA 9N EN 10P ， EN 10N EN 11P ， EN 11N	
T9， T10 R9， R10 P9， P10 N9， N10 M9， M10 L9， L10 T11， T12 R11， R12 P11， P12 N11， N12 M11， M12 L11， L12	DB0P， DB0N DB1P， DB1N DB2P， DB2N DB3P， DB3N DB4P， DB4N DB5P， DB5N DB6P， DB6N DB7P， DB7N DB8P， DB8N DB9P， DB9N DB 10P, DB 10N DB 11P, DB 11N	LVDS B Data bus differential output
A13 , A14 B13 , B14 C13 , C14 D13 , D14 E13 , E14 F13 , F14 G13， G14 B15， B16 C15， C16 D15， D16 E15， E16 F15， F16	DC0P， DC0N DC1P， DC1N DC2P， DC2N DC3P， DC3N DC4P， DC4N DC5P， DC5N DC6P， DC6N DC7P， DC7N DC8P， DC8N DC9P， DC9N DC 10P, DC 10N DC 11P, DC 11N	LVDS C Data bus differential output
T13 , T14 R13 , R14 P13 , P14 N13 , N14 M13 , M14 L13 , L14 K13， K14 R15， R16 P15， P16 N15， N16 M15， M16 L15， L16	DD0P， DD0N DD1P， DD1N DD2P， DD2N DD 3P , DD 3N DD 4P , DD 4N DD 5P , DD 5N DD 6P , DD 6N DD 7P , DD 7N DD 8P , DD 8N DD 9P , DD 9N DD 10P , DD 10N DD 11P , DD 11N	LVDS D Data bus differential output

8 Typical performance test curves

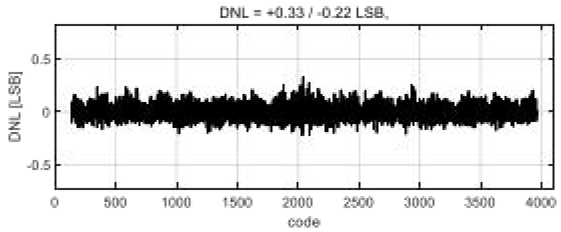
The following performance index curve is the chip workingLDEMUX = 1 andDES_EN = 0 mode , andVA 19 = VD 19 = VLVDS = +1.9V , AC Coupled signal input, Unused channels are terminated with " AC land " , AC Coupled sine wave sampling clock, f_{CLK} = 3.2 GHz @ 1 V $_{PP}$ (Single-ended signal through 1:2 Balun Convert to differential signal input); Input letter Source Impedance50 Ω (Single-ended signal through 1:2 Balun Convert to differential signal input); T $_{A}$ = 25°C .



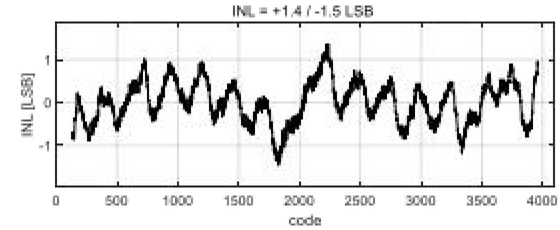
（a）DNL（f_s =3.2 GHz）



（b）INL（f_s =3.2 GHz）

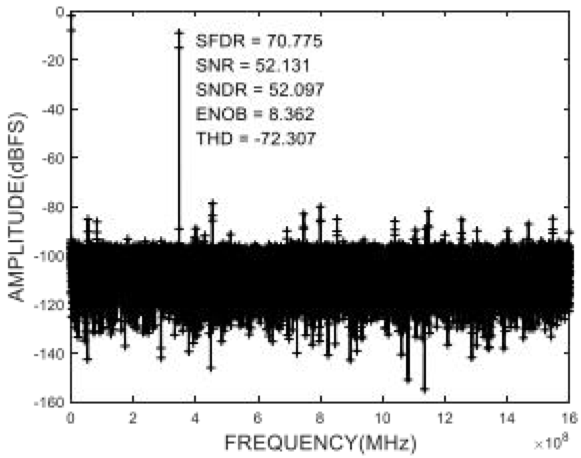


(c) DNL (f_s =5.0 GHz)

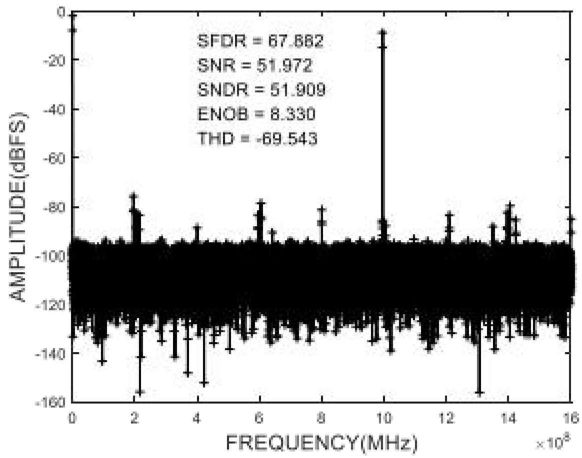


(d) INL (f_s =5.0 GHz)

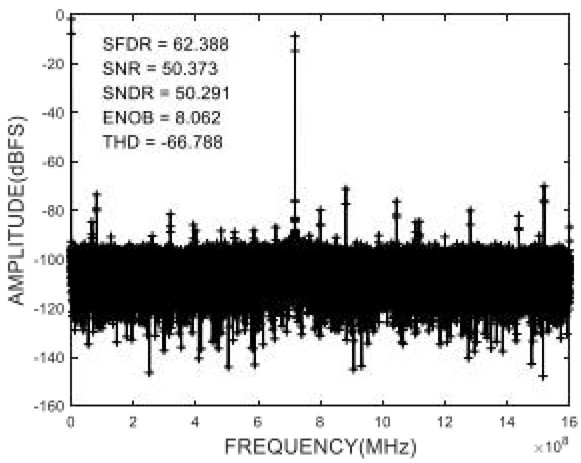
picture3 CW12DL3200 Linear error test curve



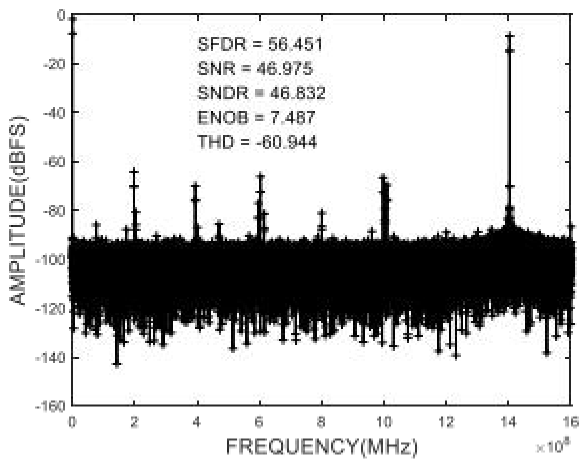
(a) f_{in} =347MHz



（b）f_{in} = 997MHz

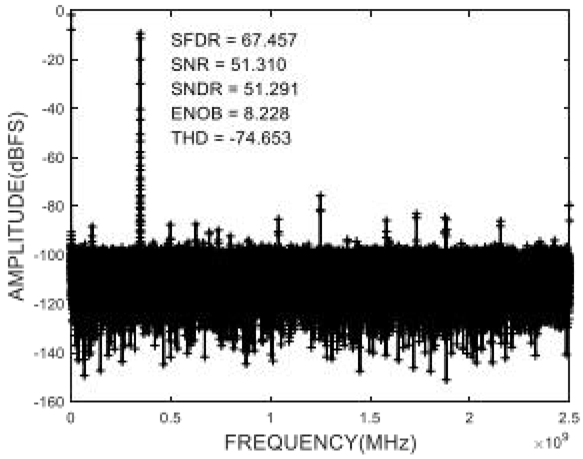


(c) f_{in} = 2482MHz

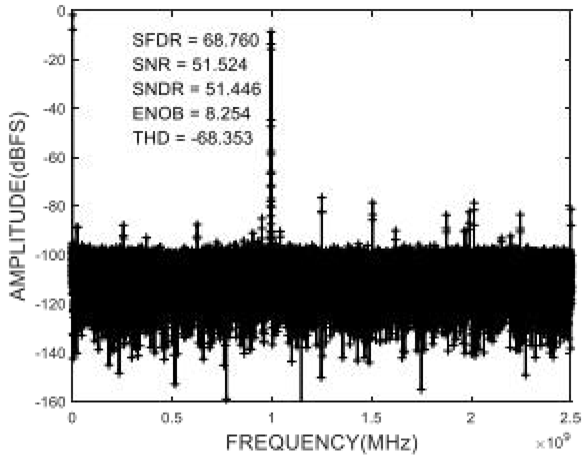


（d）f_{in} = 4997MHz

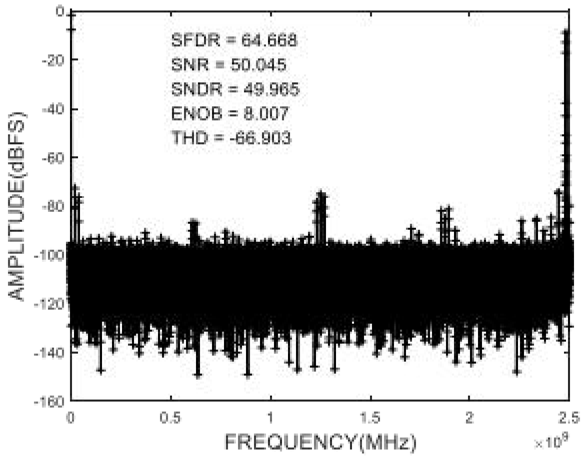
picture4 CW12DL3200 Dynamic characteristics (f_S = 3.2 GHz)



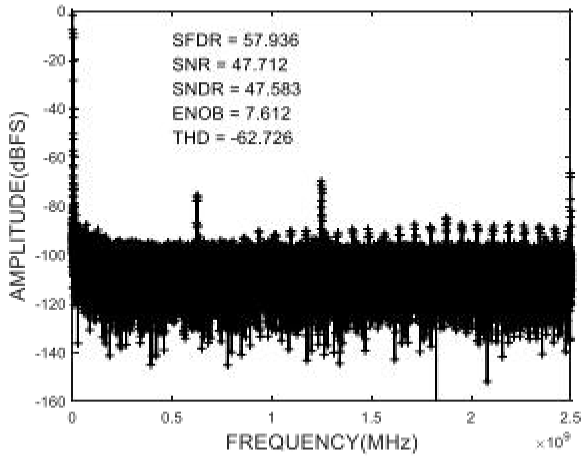
（a) *fin* =347 MHz



（ b ） *fin* = 9 97 MHz



（c) *fin* = 2482 MHz

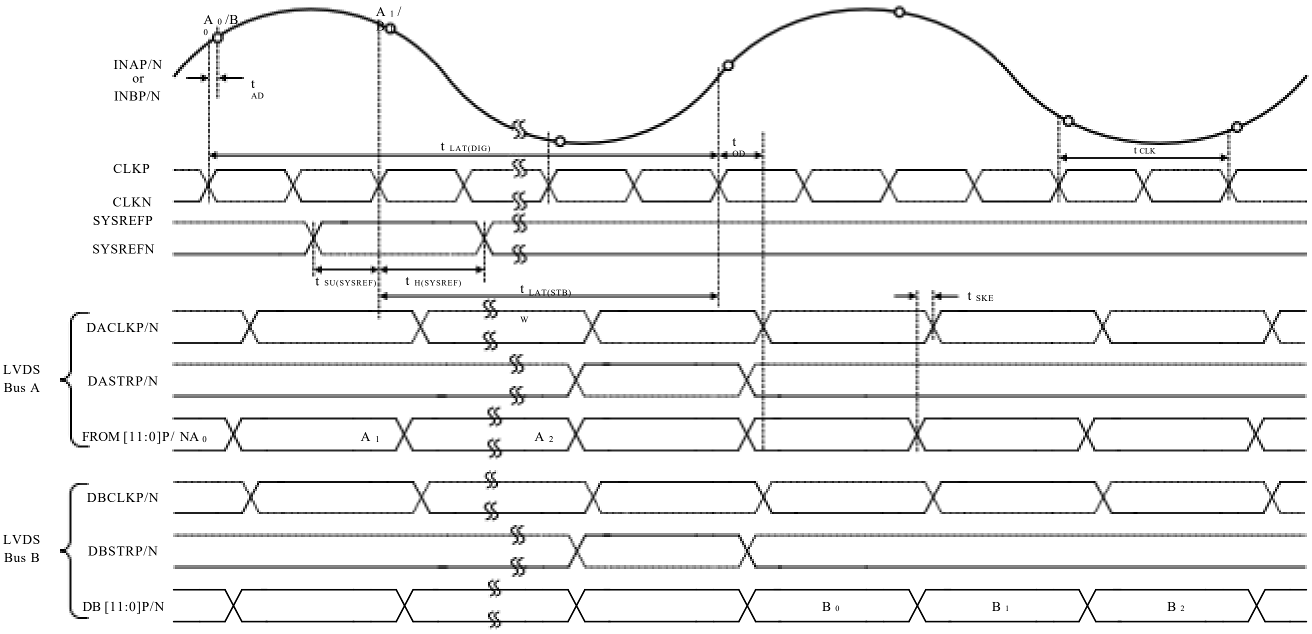


（ d ） f_{in} = 4997 MHz

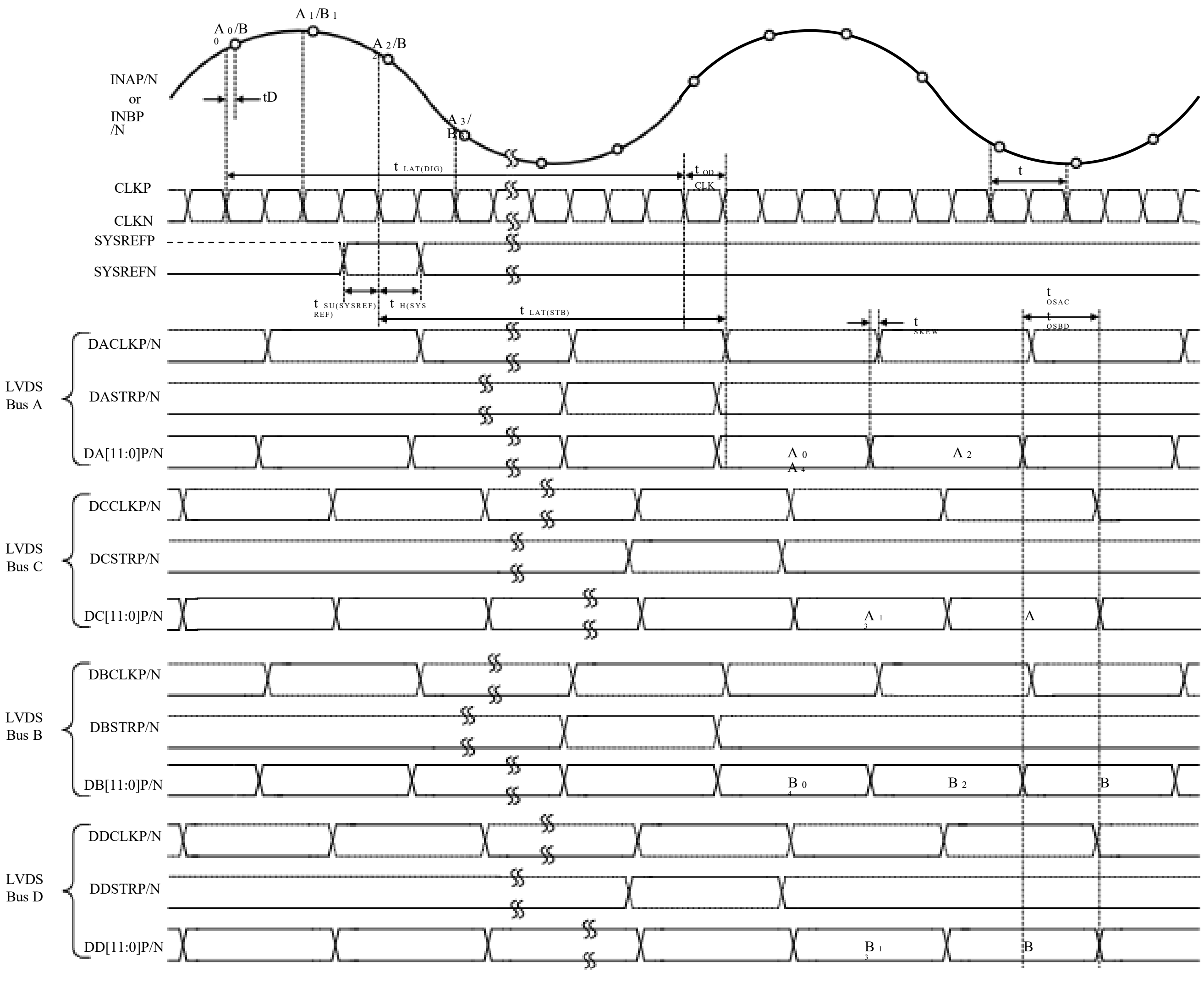
picture 5 CW12DL3200 Dynamic characteristics（ f_S = 5.0 GHz ）

9 Timing diagram

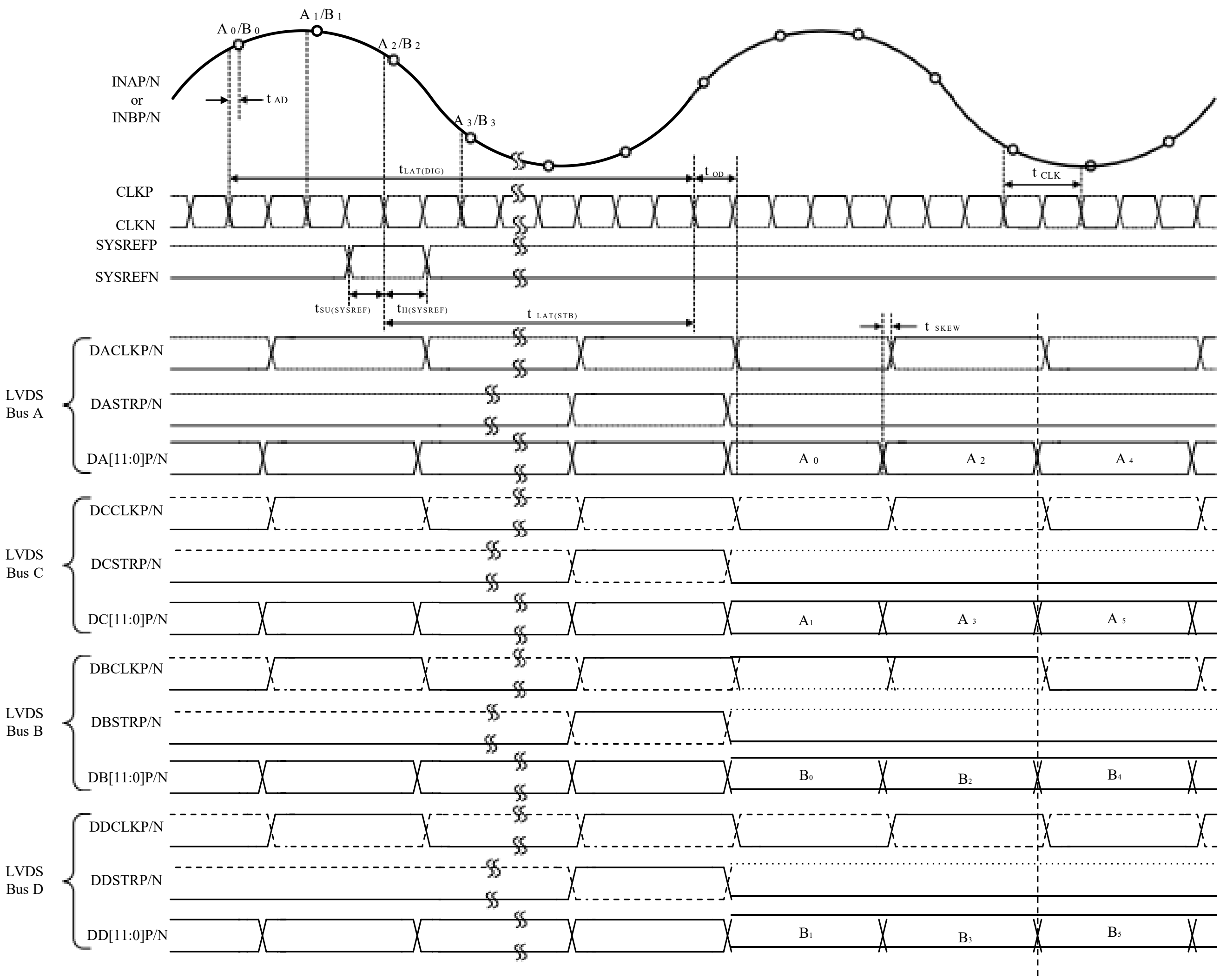
9.1 Data timing



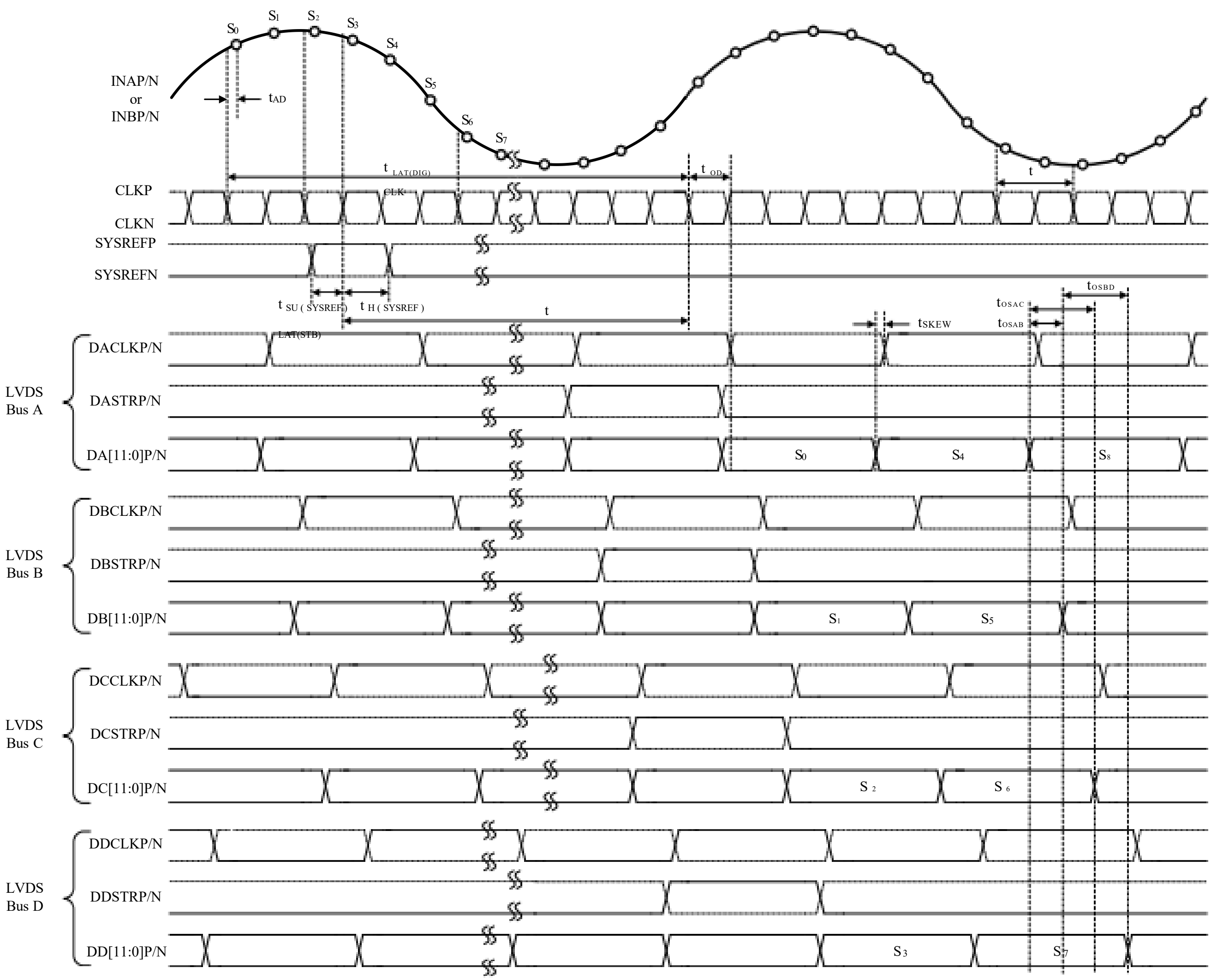
picture6 CW12DL3200 Dual Channel, Dual Bus Mode Timing (LDEMUX = 0, DES_EN = 0 , LALIGNED = 0 or 1)



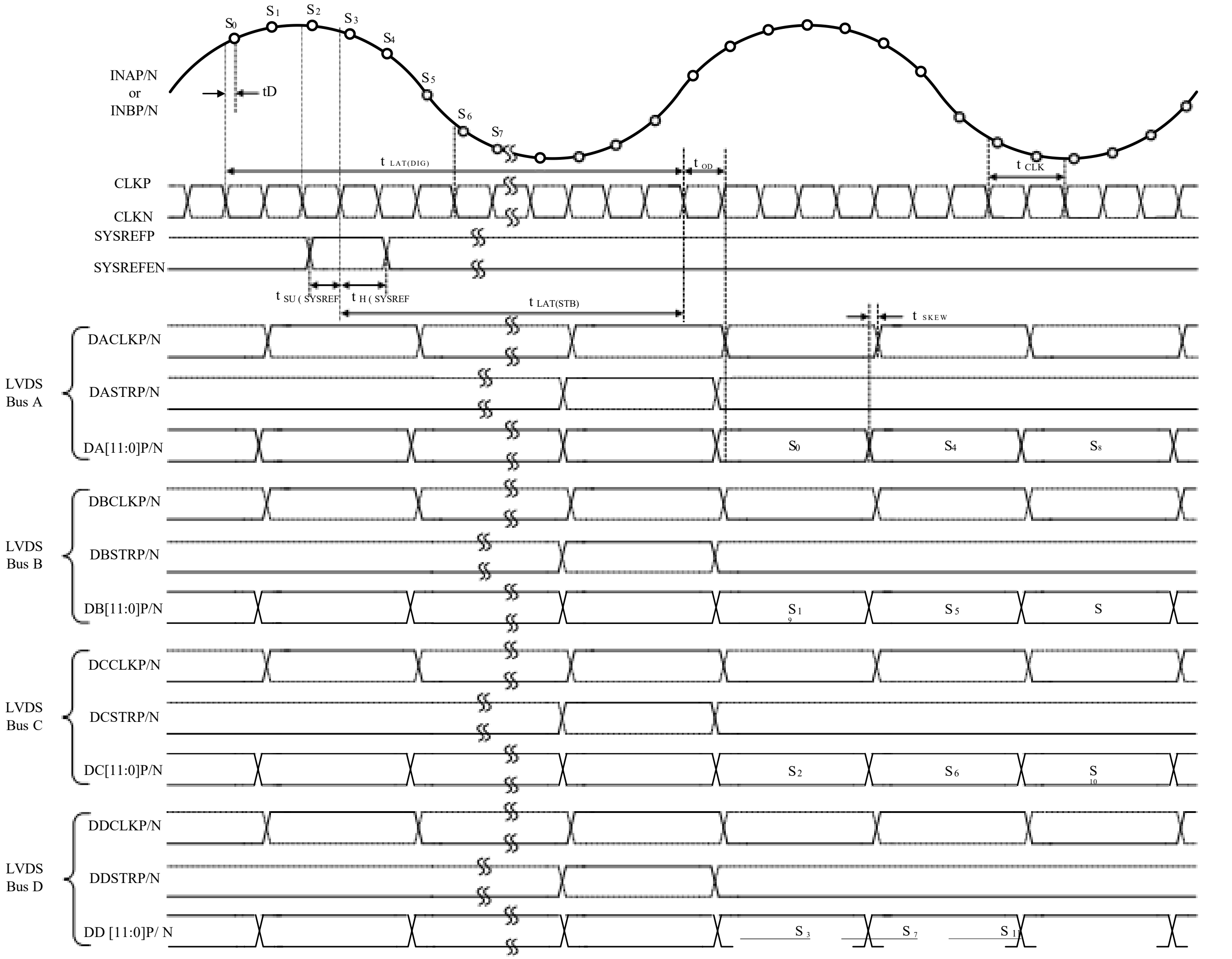
picture7 CW12DL3200 Dual-channel, four-bus interleaved mode timing (LDEMUX = 1, DES_EN = 0 , LALIGNED = 0)



picture 8 CW12DL3200 Dual Channel , Quad Bus Alignment Mode Timing (LDEMUX = 1, DES_EN = 0 , LALIGNED = 1)

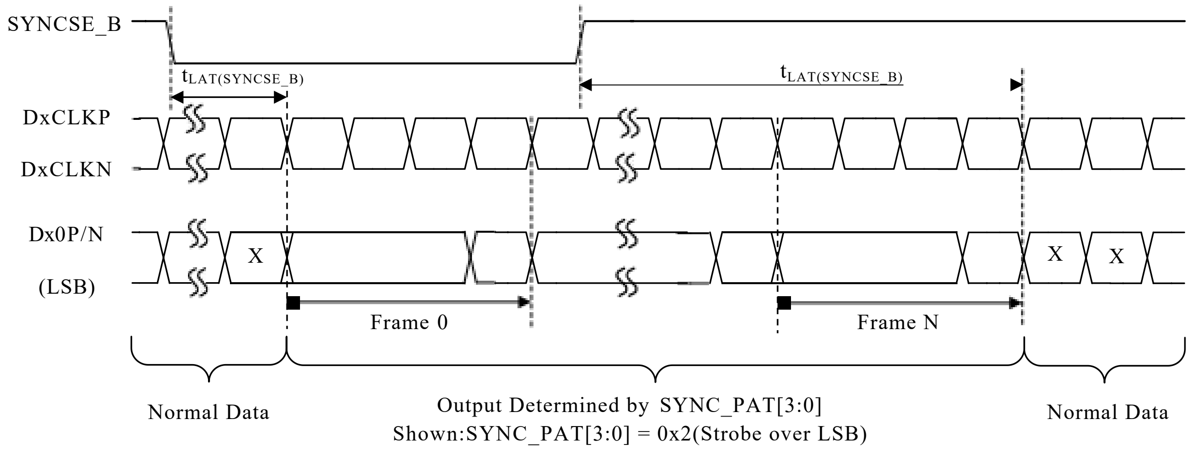


picture9 CW12DL3200 Single Channel, Four Bus Interleaved Mode Timing (LDEMUX = 1 , DES_EN = 1, LALIGNED = 0)



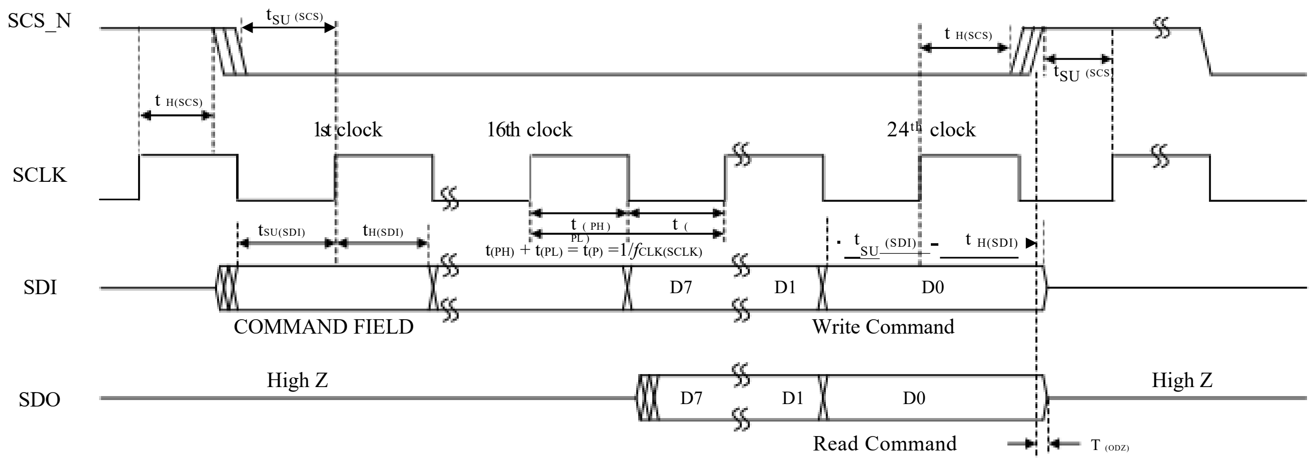
picture 10 CW12DL3200 Single Channel, Quad Bus Alignment Mode Timing (LDEMUX = 1 , DES_EN = 1, LALIGNED = 1)

9.2 SYNCSE _B Timing



picture 11 SYNCSE _B Timing

9.3 SPI Interface Timing



picture 12 SPI Read and write timing

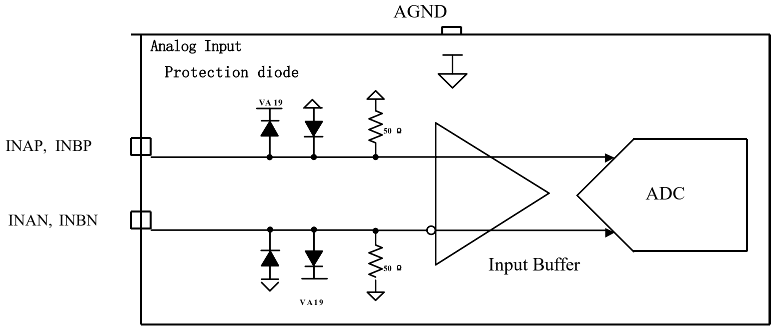
surface 8 SPI Interface command and data field definitions

Bit	definition	illustrate
1	Read / write control bit	1b : Read operation 0b : Write operation
2~16	Address bits A[14:0]	Register address, address order is MSB first
17~24	Data bits D[7:0]	Data is written to or read from a register

10 analog inputs

CW12DL3200 The analog inputs are internally buffered to achieve high input bandwidth and isolate noise from the input circuit sampling capacitors. The analog inputs must be driven differentially. Single-ended input will result in performance degradation and is not recommended. Analog input supports two input modes: AC coupling or DC coupling. The analog input common mode voltage is 1.3V , which passes through each Single-ended on differential input pins 50Ω Resistor Pair AGND Implement internal biasing. When using DC coupled inputs, it is recommended to drive the analog inputs through an external fully differential amplifier. The common-mode voltage is determined by the amplifier's V_{OCM} input signal to determine. when V_{OCM} When the value is set to about half the supply voltage of the fully differential op amp, the driver will achieve maximum output swing, but Is driving this model ADC When V_{OCM} Values and backends ADC of V_{CM} The values match.

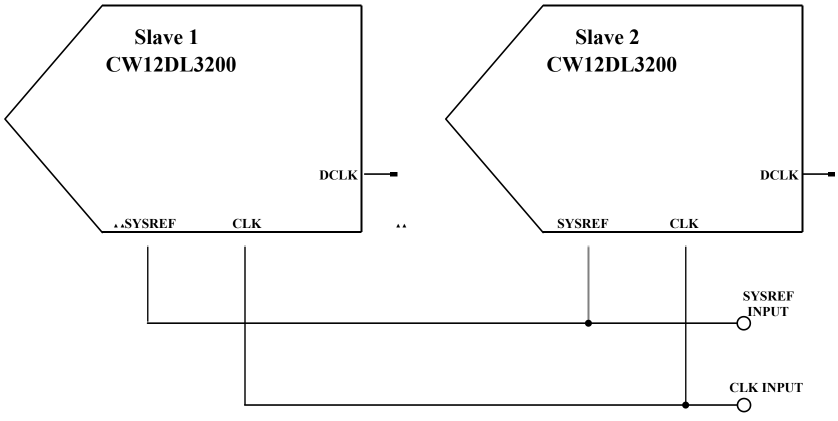
In single-channel mode, the analog input channel **INAP and INAN Will** be ADC Using single-channel mode does not reduce the analog input bandwidth compared to dual-channel mode .



picture 13 Analog input structure

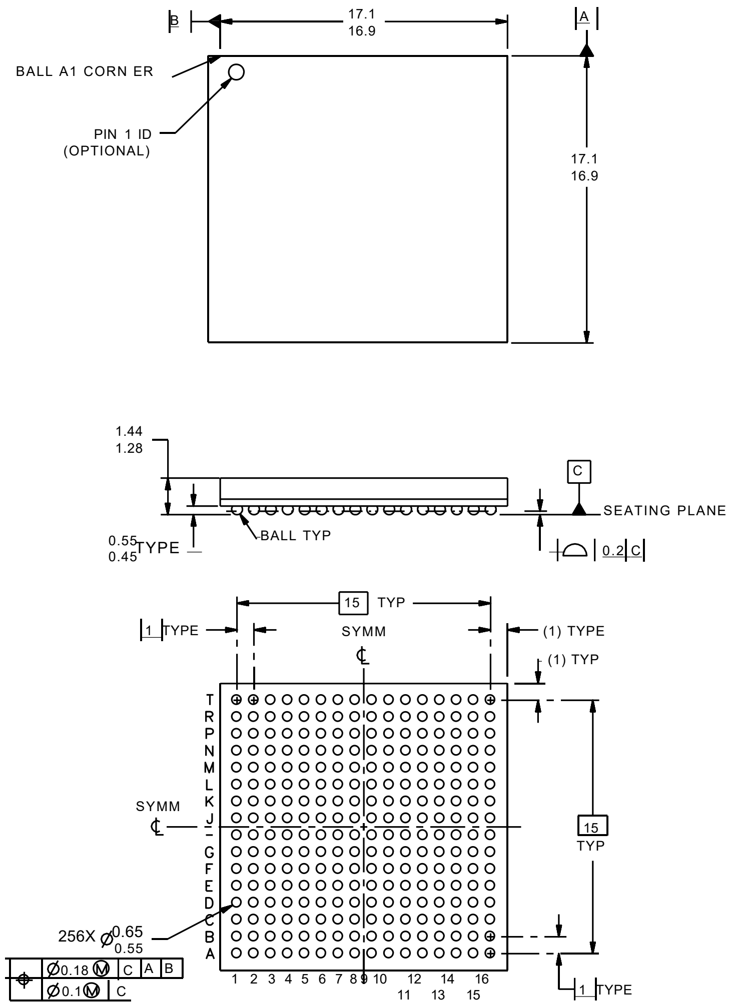
11 Introduction to Multi-chip Synchronization Function

CW12DL3200 It can realize multi-chip synchronization (AutoSync) function, and recommends users to use full slave mode. All CW12DL3200 As Slave ADC , clocked by an external clock core The chip provides a synchronous clock SYSREF = CLK /16, CLK /32, CLK /64 or CLK /128) , and SYSREF Need and CLK Homologous, driving each through equal length lines CW12DL3200 SYSREFP / SYSREFN , to achieve multiple CW12DL3200 To synchronize multiple chips ADC DCLK (including data), all DCLK Must be in phase, DCLK (including data) traces need to be of equal length, because CW12DL3200 of DCLK By chip CLK Generate and pass SYSREF Synchronization, in order to eliminate Except for each ADC Master clock CLK The difference in paths ensures CLK Reach each piece CW12DL3200 The time of receiving SYSREF The clock function must be enabled by controlling Register configuration to enable synchronization function.



picture 14 CW12DL3200 AutoSync Functional connection diagram

12 Packaging Information



picture 15 CW12DL3200 Package Outline

13 Register List

CONFIG_A Regist								
Addr: 0x0 00 reset state : 0x30								
Bit	7	6	5	4	3	2	1	0
Name	SOFT_RESET	RESERVED	ASCEND	SDO_ACTIVE	RESERVED			
reset	0x0	0x0	0x0	0x1	0x0			
Bit 7	SOFT_RESET , R/W Setting this bit causes a full reset of the device and all SPI registers (including CONFIG_A). This bit is self-clearing. After writing this bit,the device may take up to 750 ns to reset. During this time, do not perform any SPI transactions.							
Bit 6	RESERVED, R							
Bit 5	ASCEND, R/W 0 : Address is decremented during streaming reads or writes (default) 1 : Address is incremented during streaming reads or writes							
Bit 4	SDO_ACTIVE, R Always returns 1. Always use SDO for SPI reads. No SDIO mode is supported.							
Bit 3-0	RESERVED, R							

DEVICE_CONFIG Register								
Addr: 0x002 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED						MODE	
reset	0x0						0x0	
Bit 7-2	RESERVED, R							
Bit 1-0	MODE, R/W 0 : Normal operation (default) 1 : Reserved 2 : Reserved 3 : Power-down							

CHIP_TYPE Register								
Addr: 0x003 reset state: 0x01								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				CHIP_TYPE			
reset	0x0				0x01			
Bit 7-4	RESERVED, R							
Bit 3-0	CHIP_TYPE, R Always returns 0x1, indicating that the device is a high-speed ADC.							

CHIP_ID_0 Register								
Addr: 0x004 reset state: 0x03								
Bit	7	6	5	4	3	2	1	0
Name	CHIP_ID_0							
reset	0x03							
Bit 7-0	CHIP_ID_0 , R Returns 0x03							

CHIP_ID_1 Register								
Addr: 0x005 reset state: 0x10								
Bit	7	6	5	4	3	2	1	0
Name	CHIP_ID_1							
reset	0x10							
Bit 7-0	CHIP_ID_0 , R, Returns 0x10							

VENDOR_ID_0 Register								
Addr: 0x00C reset state: 0x18								
Bit	7	6	5	4	3	2	1	0
Name	VENDOR_ID_0							
reset	0x18							
Bit 7-0	VENDOR_ID_0 , R, Returns 0x18							

VENDOR_ID_1 Regis ter								
Addr : 0x00D reset state : 0x03								
Bit	7	6	5	4	3	2	1	0
Name	VENDOR_ID_1							
reset	0x03							

Bit 7-0	VENDOR_ID_1， R, Returns 0x03							
CLK_CTRL0 Register								
Addr: 0x029 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED	SYSREF_PROC_EN	SYSREF_RECV_EN	SYSREF_ZOOM	SYSREF_SEL			
reset	0x0	0x0	0x0	0x0	0x0			
Bit 7	RESERVED， R							
Bit 6	SYSREF_PROC_EN， R/W This bit enables the SYSREF processor, which allows the device to process SYSREF events (default: disabled). SYSREF_RECV_EN must be set before setting SYSREF_PROC_EN.							
Bit 5	SYSREF_RECV_EN， R/W Set this bit to enable the SYSREF receiver circuit (default: disabled).							
Bit 4	SYSREF_ZOOM， R/W Set this bit to zoom in the SYSREF windowing status and delays (impacts SYSERF_POS and SYSREF_SEL). When set, the delays used in the SYSREF windowing feature (reported in the SYSREF_POS register) become smaller. Use SYSREF_ZOOM for high clock rates, specifically when multiple SYSREF valid windows are encountered in the SYSREF_POS register.							
Bit 3-0	SYSREF_SEL， R/W Set this field to select which SYSREF delay to use. Set this field based on the results returned by SYSREF_POS;These bits must be set to 0 to use SYSREF calibration.							
CLK_CTRL1 Register								
Addr: 0x02A reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				SYSREF_TIME_STAMP_EN	DEVCLK_LVPECL_EN	SYSREF_LVPECL_EN	SYSREF_INVERTED
reset	0x0	0x0	0x0	0x0	0x0			
Bit 7-4	RESERVED， R							
Bit 3	SYSREF_TIME_STAMP_EN， R/W The SYSREF signal is output on the LSB of the LVDS output samples when SYSREF_TIMESTAMP_EN and TIME_STAMP_EN are both set. This bit allows SYSREF±to be used as the timestamp input.							
Bit 2	DEVCLK_LVPECL_EN， R/W Activate DC-coupled, low-voltage PECL mode for CLKP/N.							
Bit 1	SYSREF_LVPECL_EN， R/W Activate DC-coupled, low-voltage PECL mode for SYSREFP/N.							
Bit 0	SYSREF_INVERTED， R/W This bit inverts the SYSREF signal used for alignment.							
SYSREF_POS_0 Register								
Addr: 0x02C reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	SYSREF_POS_0							
reset	0x0							
Bit 7-0	SYSREF_POS_0， R SYSREF_POS Returns a 8-bit status value that indicates the position of the SYSREF edge with respect to CLKP/N. Use this field to program SYSREF_SEL.							
SYSREF_POS_1 Register								
Addr: 0x02D reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	SYSREF_POS_1							
reset	0x0							
Bit 7-0	SYSREF_POS_1， R SYSREF_POS Returns a 8-bit status value that indicates the position of the SYSREF edge with respect to CLKP/N. Use this field to program SYSREF_SEL.							
SYSREF_POS_2 Register								
Addr: 0x02E reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	SYSREF_POS_2							
reset	0x0							
Bit 7-0	SYSREF_POS_2， R SYSREF_POS Returns a 8-bit status value that indicates the position of the SYSREF edge with respect to CLKP/N. Use this field to program SYSREF_SEL.							
FS_RANGE_A_0 Register								
Addr: 0x030 reset state: 0x00								

Bit	7	6	5	4	3	2	1	0
Name	FS_RANGE_A_0							
reset	0x0							
Bit 7-0	FS_RANGE_A_0， R/W FS_RANGE_A_0 and FS_RANGE_A_1 enable adjustment of the analog full-scale range for INAP/N. 0x0000: Settings below 0x2000 result in degraded performance 0x2000: 500 mVPP - Recommended minimum setting 0xA000: 800 mVPP (default) 0xFFFF: 1000 mVPP - Maximum setting							

FS_RANGE_A_1 Register

Addr: 0x031
reset state: 0xA0

Bit	7	6	5	4	3	2	1	0
Name	FS_RANGE_A_1							
reset	0xA0							
Bit 7-0	FS_RANGE_A_1， R/W FS_RANGE_A_0 and FS_RANGE_A_1 enable adjustment of the analog full-scale range for INAP/N. 0x0000: Settings below 0x2000 result in degraded performance 0x2000: 500 mVPP - Recommended minimum setting 0xA000: 800 mVPP (default) 0xFFFF: 1000 mVPP - Maximum setting							

FS_RANGE_B_0 Register

Addr: 0x032
reset state: 0x00

Bit	7	6	5	4	3	2	1	0
Name	FS_RANGE_B_0							
reset	0x0							
Bit 7-0	FS_RANGE_B_0， R/W FS_RANGE_B_0 and FS_RANGE_B_1 enable adjustment of the analog full-scale range for INBP/N. 0x0000: Settings below 0x2000 result in degraded performance 0x2000: 500 mVPP - Recommended minimum setting 0xA000: 800 mVPP (default) 0xFFFF: 1000 mVPP - Maximum setting							

FS_RANGE_B_1 Register

Addr: 0x033
reset state: 0xA0

Bit	7	6	5	4	3	2	1	0
Name	FS_RANGE_B_1							
reset	0xA0							
Bit 7-0	FS_RANGE_B_1， R/W FS_RANGE_B_0 and FS_RANGE_B_1 enable adjustment of the analog full-scale range for INBP/N. 0x0000: Settings below 0x2000 result in degraded performance 0x2000: 500 mVPP - Recommended minimum setting 0xA000: 800 mVPP (default) 0xFFFF: 1000 mVPP - Maximum setting							

SYNC_CTRL Register

Addr: 0x03B
reset state: 0x00

Bit	7	6	5	4	3	2	1	0
Name	RESERVED						TMSTP_LVPECL_EN	TMSTP_RECV_EN
reset	0x0						0x0	0x0
Bit 7-2	RESERVED， R							
Bit 1	TMSTP_LVPECL_EN， R/W When set, this bit activates the DC-coupled, low-voltage PECL mode for the differential TMSTPP/N receiver.							
Bit 0	TMSTP_RECV_EN， R/W This bit enables the differential TMSTPP/N receiver							

LVDS_SWING Register

Addr: 0x048
reset state: 0x00

Bit	7	6	5	4	3	2	1	0
Name	RESERVED						LVDS_SWING	
reset	0x0						0x0	
Bit 7-2	RESERVED， R							

Bit 1-0	LVDS_SWING, R/W These bits set the swing mode of the LVDS output buffers: 0 : High-swing mode (HSM) (default) 1 : Low-swing mode (LSM) 2 : Reserved (do not use) 3 : Low-swing mode for use with receivers that have a high-Z load termination (HZM). Only use with short transmission lines to avoid reflections caused by a high-Z receiver							
RTRIM_A Register								
Addr: 0x07E reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RTRIM_A							
reset	0x0							
Bit 7-0	RTRIM_A, R/W This register controls the INAP/N ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.							
RTRIM_B Register								
Addr: 0x07F reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RTRIM_B							
reset	0x0							
Bit 7-0	RTRIM_B, R/W This register controls the INBP/N ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.							
LSB_CTRL Register								
Addr: 0x160 reset state : 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED							TIME_STAMP_EN
reset	0x0							0x0
Bit 7-1	RESERVED , R							
Bit 0	TIME_STAMP_EN , R /W When set, the timestamp signal is transmitted on the LSB of the output samples. The latency of the timestamp signal (through the entire chip) matches the latency of the analog ADC inputs. Also set TMSTP_RECV_EN when using TIME_STAMP_EN.							
LSB_SEL Register								
Addr: 0x1 61 reset state : 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED							LSB_SEL
reset	0x0							0x0
Bit 7-1	RESERVED , R							
Bit 0	LSB_SEL , R/W 0 : Place timestamp on lane 0 (Dx0±) of each LVDS output bus, independent ofthe LWIDTH setting. Lane 0 of each bus is enabled regardless of LWIDTH. 1 : Place timestamp on the LSB of the effective sample size as set by the LWIDTH parameter. The timestamp is placed on the LSB of the output sample. The lane that carries timestamp depends on the selected output sample width (LWIDTH). For 12-bit samples, lane 0 carries the control data. For 11-bit samples, lane 1 carries the control data. For 10-bit samples, lane 2 carries the control data. For 8-bit samples, lane 4 carries the control data.							
UPAT0_0 Register								
Addr: 0x180 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	UPAT0_0							
reset	0x0							
Bit 7-0	UPAT0_0 , R/W UPAT0_0 and UPAT0_1 Defines the value for sample 0 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT0_1 Register								
Addr: 0x181 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				UPAT0_1			
reset	0x0				0x0			
Bit 7-4	RESERVED, R							

Bit 3-0	UPAT0_1， R/W UPAT0_0 and UPAT0_1 Defines the value for sample 0 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT1_0 Register								
Addr: 0x182 reset state: 0xFF								
Bit	7	6	5	4	3	2	1	0
Name	UPAT1_0							
reset	0xFF							
Bit 7-0	UPAT1_0， R/W UPAT1_0 and UPAT1_1 Defines the value for sample 1 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT1_1 Register								
Addr: 0x183 reset state: 0x0F								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				UPAT1_1			
reset	0x0				0xF			
Bit 7-4	RESERVED， R							
Bit 3-0	UPAT1_1， R/W UPAT1_0 and UPAT1_1 Defines the value for sample 1 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT2_0 Register								
Addr: 0x184 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	UPAT2_0							
reset	0x00							
Bit 7-0	UPAT2_0， R/W UPAT2_0 and UPAT2_1 Defines the value for sample 2 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT2_1 Register								
Addr: 0x185 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				UPAT2_1			
reset	0x0				0x0			
Bit 7-4	RESERVED， R							
Bit 3-0	UPAT2_1， R/W UPAT2_0 and UPAT2_1 Defines the value for sample 2 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT3_0 Register								
Addr: 0x186 reset state: 0xFF								
Bit	7	6	5	4	3	2	1	0
Name	UPAT3_0							
reset	0xFF							
Bit 7-0	UPAT3_0， R/W UPAT3_0 and UPAT3_1 Defines the value for sample 3 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT3_1 Register								
Addr: 0x187 reset state: 0x0F								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				UPAT3_1			
reset	0x0				0xF			
Bit 7-4	RESERVED， R							
Bit 3-0	UPAT3_1， R/W UPAT3_0 and UPAT3_1 Defines the value for sample 3 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT4_0 Register								
Addr: 0x188 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	UPAT4_0							
reset	0x00							
Bit 7-0	UPAT4_0， R/W UPAT4_0 and UPAT4_1 Defines the value for sample 4 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							

UPAT4_1 Register								
Addr: 0x189 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				UPAT4_1			
reset	0x0				0x0			
Bit 7-4	RESERVED, R							
Bit 3-0	UPAT4_1, R/W UPAT4_0 and UPAT4_1 Defines the value for sample 4 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT5_0 Register								
Addr: 0x18A reset state: 0xFF								
Bit	7	6	5	4	3	2	1	0
Name	UPAT5_0							
reset	0xFF							
Bit 7-0	UPAT5_0, R/W UPAT5_0 and UPAT5_1 Defines the value for sample 5 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT5_1 Register								
Addr: 0x18B reset state: 0x0F								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				UPAT5_1			
reset	0x0				0xF			
Bit 7-4	RESERVED, R							
Bit 3-0	UPAT5_1, R/W UPAT5_0 and UPAT5_1 Defines the value for sample 5 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT6_0 Register								
Addr: 0x18C reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	UPAT6_0							
reset	0x00							
Bit 7-0	UPAT6_0, R/W UPAT6_0 and UPAT6_1 Defines the value for sample 6 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT6_1 Register								
Addr: 0x18D reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				UPAT6_1			
reset	0x0				0x0			
Bit 7-4	RESERVED, R							
Bit 3-0	UPAT6_1, R/W UPAT6_0 and UPAT6_1 Defines the value for sample 6 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT7_0 Register								
Addr: 0x18E reset state: 0xFF								
Bit	7	6	5	4	3	2	1	0
Name	UPAT7_0							
reset	0xFF							
Bit 7-0	UPAT7_0, R/W UPAT7_0 and UPAT7_1 Defines the value for sample 7 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT7_1 Register								
Addr: 0x18F reset state : 0x0F								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				UPAT7_1			
reset	0x0				0xF			
Bit 7-4	RESERVED, R							
Bit 3-0	UPAT7_1, R/W UPAT7_0 and UPAT5_1 Defines the value for sample 7 of the user defined pattern. Note: Only change this register when LVDS_EN = 0.							
UPAT_CTRL Register								

Addr: 0x190
reset state: 0x1E

Bit	7	6	5	4	3	2	1	0
Name	RESERVED			LANE_PAT	UPAT_INV_D	UPAT_INV_C	UPAT_INV_B	UPAT_INV_A
reset	0x0			0x1	0x1	0x1	0x1	0x0

Bit 7-5	RESERVED , R
Bit 4	LANE_PAT , R/W When set, the UPATn registers are ignored, and the user-defined pattern is set to: 0x000, 0xFFF, 0x000, 0x000, 0x000, 0xFFF, 0xFFF, 0xFFF. This bit acts as a shortcut to avoid programming the UPATn registers. PAT_SEL register must still be programmed to configure the interface to select the user-defined pattern. The UPAT_INV_*registers still apply when using LANE_PAT.
Bit 3	UPAT_INV_D, R/W When set, bit [11] of the user-defined pattern is inverted on the bus D output
Bit 2	UPAT_INV_C, R/W When set, bit [10] of the user-defined pattern is inverted on the bus C output.
Bit 1	UPAT_INV_B, R/W When set, bit [9] of the user-defined pattern is inverted on the bus B output.
Bit 0	UPAT_INV_A, R/W When set, bit [8] of the user-defined pattern is inverted on the bus A output. Note: Only change this register when LVDS_EN = 0.

LVDS_EN Register

Addr: 0x200
reset state: 0x01

Bit	7	6	5	4	3	2	1	0
Name	RESERVED							LVDS_EN
reset	0x0							0x1

Bit 7-1	RESERVED, R
Bit 0	LVDS_EN, R/W 0 : Disable LVDS interface 1 : Enable LVDS interface Note 1: Before altering other LVDS registers, you must clear LVDS_EN. When LVDS_EN is 0, the LVDS interface block is held in reset and the outputs are powered down. The clocks are gated off to save power. The frame counter is also held in reset, so SYSREF will not align the frame counter.

LMODE Register

Addr: 0x201
reset state: 0x01

Bit	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	LWIDTH		RESERVED	DES_EN	LALIGNED	LDEMUX
reset	0x0	0x0	0x0		0x0	0x0	0x0	0x1

Bit 7	RESERVED, R
Bit 6	RESERVED, R
Bit 5-4	LWIDTH, R/W Specifies the sample width for the LVDS output interface. 0 : 12-bit sample width (default) 1 : 11-bit sample width 2 : 10-bit sample width 3 : 8-bit sample width
Bit 3	RESERVED, R
Bit 2	DES_EN, R/W 0 : Enable dual channel mode (default) 1 : Enable single channel mode
Bit 1	LALIGNED, R/W 0 : The LVDS buses are staggered for optimized switching noise and latency. 1 : The LVDS buses are aligned for simplified timing.
Bit 0	LDEMUX, R/W 0 : Demux-by-1, uses 2 LVDS buses total 1 : Demux-by-2, uses 4 LVDS buses total

LFRAME Register

Addr: 0x202
reset state : 0x80

Bit	7	6	5	4	3	2	1	0
Name	LFRAME							
reset	0x80							

Bit 7-0	LFRAME , R/W Defines the number of UIs in each LVDS frame. Any multiple of 4 from 4 to 128 is supported. All other values are unsupported. When LDEMUX=0, one UI is one CLK±cycle. When LDEMUX=1, one UI is two CLK±cycles. Note: Setting LFRAME to 4 is not recommended, as it may be difficult to achieve deterministic latency over all process, voltage, and temperature conditions. The propagation delay variation may be larger than the frame period.

LSYNC_N Register

Addr: 0x2 03
reset state : 0x01

Bit	7	6	5	4	3	2	1	0
Name	RESERVED							LSYNC_N
reset	0x0							0x1

Bit 7-1	RESERVED , R
Bit 0	LSYNC_N , R/W Set this bit to 0 to request LVDS synchronization (equivalent to the hardware SYNC signal being asserted, as selected by SYNC_SEL). For normal operation, leave this bit set to 1. Note: The LSYNC_N register can always generate a synchronization request, regardless of the SYNC_SEL setting in the LCTRL register. However, if the selected sync pin is stuck low, the synchronization request cannot be de-asserted unless SYNC_SEL=2.

LCTRL Register

Addr: 0x2 04
reset state : 0x02

Bit	7	6	5	4	3	2	1	0
Name	RESERVED			SCR	SYNC_SEL		FORMAT	RESERVED
reset	0x0			0x0	0x0		0x1	0x0

Bit 7-5	RESERVED , R
Bit 4	SCR, R/W When set, all LVDS data and strobes are scrambled. This also includes the part-time strobes or timestamp signals (since they are output on the data lanes).
Bit 3-2	SYNC_SEL, R/W 0 : Use the SYNC_SE input for SYNC function (default) 1 : Use the TMSTP±input for SYNC function. also set TMSTP_RECV_EN to use the differential TMSTP±input. 2 : Do not use any SYNC input pin, set if using LSYNC_N.
Bit 1	SFORMAT, R/W Output sample format for LVDS output samples 0 : Offset binary 1 : Signed 2' s complement (default)
Bit 0	RESERVED, R

PAT_SEL Register

Addr: 0x205
reset state: 0x02

Bit	7	6	5	4	3	2	1	0
Name	RESERVED			ACT_PAT	SYNC_PAT			
reset	0x0			0x0	0x2			

Bit 7-5	RESERVED, R
Bit 4	ACT_PAT, R/W This selects the output pattern that is generated when the SYNC signal is de-asserted. 0: ADC output data 1: All LVDS lanes output the user-defined pattern (see UPAT registers)
Bit 3-0	SYNC_PAT, R/W This selects the output pattern that is generated when the SYNC signal is asserted. 0: Reserved 1: All LVDS lanes output the user-defined pattern (see UPAT registers) 2: Frame strobe is transmitted on the LSB of the output samples only. The other bits transmit data based on ACT_PAT. 3: The frame strobe is transmitted on all active LVDS data lanes and strobes. 4-15: Reserved

LCS_EN Register

Addr: 0x206
reset state: 0xFF

Bit	7	6	5	4	3	2	1	0
Name	DDSTB_EN	DCSTB_EN	DBSTB_EN	DASTB_EN	DDCLK_EN	DCCLK_EN	DBCLK_EN	DACLK_EN
reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1

Bit 7	DDSTB_EN, R/W Enable DDSTBP/N output
Bit 6	DCSTB_EN, R/W Enable DCSTBP/N output
Bit 5	DBSTB_EN, R/W Enable DBSTBP/N output

Bit 4	DASTB_EN ， R/W Enable DASTBP/N output							
Bit 3	DDCLK_EN，R/W Enable DDCLKP/N output							
Bit 2	DCCLK_EN，R/W Enable DCCLKP/N output							
Bit 1	DBCLK_EN，R/W Enable DBCLKP/N output							
Bit 0	DACLK_EN，R/W Enable DACLKP/N output							
LVDS_STATUS Register								
Addr: 0x208 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED		SYNC_STATUS	REALIGNED	ALIGNED	RESERVED		
reset	0x0		0x0	0x0	0x0	0x0		
Bit 7-6	RESERVED，R							
Bit 5	SYNC_STATUS，R/W Returns the instantaneous state of the LVDS interface SYNC signal (SYNC_SE or TMSTPP/N). 0：SYNC asserted 1：SYNC de-asserted							
Bit 4	REALIGNED，R/W When high, indicates that SYSREF realigned internal clocks. REALIGNED_ALM should be used for monitoring of realignment events instead of this bit. Writing a 1 to this bit will clear it, but will not affect the REALIGNED_ALM bit.							
Bit 3	ALIGNED，R/W When high, indicates that internal clock phases have been established by SYSREF. Any SYSREF rising edge that is processed after enabling the LVDS system will set this bit. This bit can be monitored during startup to verify that SYSREF has been processed before continuing system initialization. Writing a 1 to this bit will clear it and the next SYSREF event will set it again.							
Bit 2-0	RESERVED，R							
PD_CH Register								
Addr: 0x209 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED						PD_BCH	PD_ACH
reset	0x0						0x0	0x0
Bit 7-2	RESERVED，R							
Bit 1	PD_BCH，R/W When set, the “B” ADC channel is powered down.							
Bit 0	PD_ACH，R/W When set, the “A” ADC channel is powered down. Important notes: LVDS_EN must be set to 0 before changing PD_CH. PD_CH disables the LVDS lanes (Dx[11:0], DxSTB, DxCLK) for the powered down channel. To power down both ADC channels, use MODE or the PD pin.							
OVR_T0 Register								
Addr: 0x211 reset state: 0xF2								
Bit	7	6	5	4	3	2	1	0
Name	OVR_T0							
reset	0xF2							
Bit 7-0	OVR_T0，R/W This parameter defines the absolute sample level that causes OVA0 or OVB0 to be set. The detection level in dBFS (peak) is 20log10(OVR_T0/256) (default: 0xF2 = 242 –> -0.5dBFS)							
OVR_T1 Register								
Addr: 0x212 reset state: 0xAB								
Bit	7	6	5	4	3	2	1	0
Name	OVR_T1							
reset	0xAB							
Bit 7-0	OVR_T1，R/W This parameter defines the absolute sample level that causes OVA1 or OVB1 to be set. The detection level in dBFS (peak) is 20log10(OVR_T1/256) (default: 0xAB = 171 –> -3.5dBFS)							
OVR_CFG Register								
Addr: 0x213 reset state: 0x07								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				OVR_EN	OVR_N		
reset	0x0				0x0	0x7		
Bit 7-4	RESERVED , R							

Bit 3	OVR_EN , R/W ORA0, ORA1, ORB0 and ORB1 outputs pins are enabled and output the overrange status when this bit is set high. The outputs are held low when this bit is set low.							
Bit 2-0	OVR_N, R/W Program this register to adjust the pulse length for the ORA0, ORA1 and ORB0, ORB1 outputs. The minimum pulse duration of the overrange outputs is 8 ×2OVR_N CLKP/N cycles.							
SPIN_ID Register								
Addr: 0x297 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED			SPIN_ID				
reset	0x0			0x0				
Bit 7-5	RESERVED, R							
Bit 4-0	SPIN_ID, R Chip Spin Identifier,Read only.							
SRC_EN Register								
Addr: 0x2B0 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED							SRC_EN
reset	0x0							0x0
Bit 7-1	RESERVED , R							
Bit 0	SRC_EN , R/W 0 : SYSREF calibration disabled (default). Use the TAD register to manually control the tAD Adjust setting and adjust the CLK±aperture delay. 1: SYSREF calibration enabled. The CLK±delay is automatically calibrated. The TAD register is ignored. A 0-to-1 transition on SRC_EN starts the SYSREF calibration sequence. Program SRC_CFG before setting SRC_EN. Ensure that ADC calibration is not running before setting SRC_EN.							
SRC_STATUS_2 Register								
Addr: 0x2B4 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED					SRC_FAIL	SRC_DONE	RESERVED
reset	0x0							
Bit 7-3	RESERVED, R							
Bit 2	SRC_FAIL, R SYSREF Calibration Status.							
Bit 1	SRC_DONE, R SYSREF Calibration Status. This bit returns ‘1’ when SRC_EN=1 and SYSREF Calibration has been completed.							
Bit 0	RESERVED, R							
TAD_0 Register								
Addr: 0x2B5 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	TAD_0							
reset	0x0							
Bit 7-0	TAD_0 , R/W TAD_0,TAD_1 and TAD_2 controls t_{AD} Adjust when SRC_EN=0. Use this register to manually control the CLKP/N inversion and delay when SYSREF Calibration is disabled. TAD_0 controls the fine delay adjustment. If the LVDS interface is enabled (LVDS_EN=1), the following rules must be obeyed to avoid clock glitches and unpredictable behavior: TAD_0 may be changed to any value at any time since its resolution is too fine to cause clock glitches.							
TAD_1 Register								
Addr: 0x2B6 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	TAD_1							
reset	0x0							
Bit 7-0	TAD_1 , R/W TAD_0,TAD_1 and TAD_2 controls tAD Adjust when SRC_EN=0. Use this register to manually control the CLKP/N inversion and delay when SYSREF Calibration is disabled. TAD_1 controls the coarse delay adjustment. If the LVDS interface is enabled (LVDS_EN=1), the following rules must be obeyed to avoid clock glitches and unpredictable behavior: TAD_1 must be increased or decreased gradually (no more than 4 codes at a time). This rule can be obeyed manually via SPI writes or by setting TAD_RAMP_EN.							
TAD_2 Register								
Addr: 0x2 B7 reset state : 0x00								

Bit	7	6	5	4	3	2	1	0
Name	RESERVED							TAD_2
reset	0x0							0x0
Bit 7-1	RESERVED , R							
Bit 0	TAD_2 , R/W TAD_0,TAD_1 and TAD_2 controls t_{AD} Adjust when SRC_EN=0. Use this register to manually control the CLKP/N inversion and delay when SYSREF Calibration is disabled. TAD_2 inverts CLKP/N when set. If the LVDS interface is enabled (LVDS_EN=1), the following rules must be obeyed to avoid clock glitches and unpredictable behavior: Do not change TAD[16]. LVDS_EN must be set to 0 before changing TAD[16].							
ALARM Register								
Addr: 0x2C0 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED							ALARM
reset	0x0							0x0
Bit 7-1	RESERVED , R							
Bit 0	ALARM , R Alarm Interrupt (Read-only) This bit returns a '1' whenever any unmasked alarm is set in the ALM_STATUS register. Use ALM_MASK to mask (disable) individual alarms. CAL_STATUS_SEL can be used to drive the ALARM bit onto the CAL_STAT pin to provide a hardware alarm interrupt signal.							
ALM_STATUS Register								
Addr: 0x2C1 reset state: 0x05								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED					REALIGNED_ ALM	RESERVED	CLK_ALM
reset	0x0					0x1	0x0	0x1
Bit 7-3	RESERVED , R							
Bit 2	REALIGNED_AL M , R Realigned Alarm: This bit is set whenever SYSREF causes the internal clocks (including the frame counter) to be realigned to a new phase. Write a '1' to clear this bit.							
Bit 1	RESERVED, R							
Bit 0	CLK_ALM, R/W Clock Alarm: This bit can be used to detect an upset to the internal clocks. This bit is set whenever the internal clock dividers for the A and B channels do not match. Write a '1' to clear this bit. Refer to Alarm Monitoring for the proper usage of this register. Note: After power-on reset or soft-reset, all alarm bits are set to '1.'							
ALM_MASK Register								
Addr: 0x2C2 reset state : 0x05								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED					REAL_MASK GNED_ALM	RESERVED	MASK_CLK_ ALM
reset	0x0					0x1	0x0	0x1
Bit 7-3	RESERVED , R							
Bit 2	MASK_REALIGNED_ALM, R/W When set, REALIGNED_ALM is masked and will not impact the ALARM register bit.							
Bit 1	MASK_CLK_ALM, R							
Bit 0	MASK_REALIGNED_ALM, R/W When set, CLK_ALM is masked and will not impact the ALARM register bit.							
OADJ_A_FG0_VINA_0 Register								
Addr: 0x344 reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	OADJ_A_FG0_VINA_0							
reset	0x0							
Bit 7-0	OADJ_A_FG0_VINA_0 , R/W Offset adjustment value applied to A-ADC when it samples INAP/N using 0°clock phase and foreground calibration is enabled.							
OADJ_A_FG0_VINA_1 Register								
Addr: 0x345 reset state : 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				OADJ_A_FG0 _VINA_1			
reset	0x0				0x0			
Bit 7-4	RESERVED , R							
Bit 3-0	OADJ_A_FG0_VINA _1 , R/W Offset adjustment value applied to A-ADC when it samples INAP/N using 0°clock phase and foreground calibration i s enabled.							
OADJ_B_FG0_VINB_0 Register								

Addr: 0x3 4E reset state : 0x00								
Bit	7	6	5	4	3	2	1	0
Name	OADJ_B_FG0 _VINB_0							
reset	0x0							
Bit 7-0	OADJ_B_FG0_VINB_0 , R/W Offset adjustment value applied to B-ADC when it samples INBP/N using 0°clock phase and foreground calibration is enabled.							

OADJ_B_FG0_VINB_1 Register								
Addr: 0x34F reset state: 0x00								
Bit	7	6	5	4	3	2	1	0
Name	RESERVED				OADJ_B_FG0_VINB_1			
reset	0x0				0x0			
Bit 7-4	RESERVED, R							
Bit 3-0	OADJ_B_FG0_VINB_1 , R/W Offset adjustment value applied to B-ADC when it samples INBP/N using 0°clock phase and foreground calibration is enabled.							