# CW9653 Data Manual

# Four channels 16 bit 125MSPS ADC

## 1.0 Overview

CW9653 is a 4-channel, 16-bit, 125MSPS analog-to-digital converter (ADC) with built-in sample-and-hold circuit, designed for low cost, low power consumption, small size and ease of use . The product has a conversion rate of up to 125MSps , outstanding dynamic performance and low power consumption, and is suitable for applications with small package size.

CW9653 Using 1.8V Single supply and LVPECL/CMOS/LVDS
A compatible sample rate clock signal is required to fully operate the device. For most applications, no external reference power source or driver components are required.

To obtain a suitable LVDS Serial Data Rate, CW9653 The MCU automatically multiplies the sample rate clock. It provides a data clock output (DCO) for capturing data at the output, and a frame clock output (FCO) for signaling a new output byte. It also supports each channel to enter a power-saving state individually; when all channels are turned off, the power consumption is less than 10mW .

## 2.0 application

- Medical imaging and non-invasive ultrasound testing
- High-speed imaging
- Radio Receiver
- Test equipment

## 3.0 Features

- 1.8V Power supply
- Low power consumption: 190mW per channel @ 125MSps
- Signal-to-Noise Ratio (SNR) : 69.5dBFS@70MHz
- Differential nonlinearity (DNL) : ±0.7LSB ( typical )
- Integral nonlinearity (INL) : ±8LSB ( typical )
- Low Power Serial LVDS
- 2V PP Input voltage range
- QFN- 48 Package 7mm×7mm

## 4.0 Performance Indicators

- Full power bandwidth: 650 MHz
- Static performance: DNL -0.9 /+1.5 LSB , INL -8.0 /+8.0 LSB
- Dynamic performance ( $fS$ = 125MSps, input signal power - 1 dBFS )

— *fin* = 9.7MHz
ENOB = 11.7 Bit , SNDR = 72.3 dBFS , SNR = 72.6 dBFS

— *fin* = 70 MHz
ENOB = 11.3 Bit , SNDR = 69.5 dBFS , SNR = 69.8 dBFS

— *fin* = 128 MHz
ENOB = 10.7 Bit , SNDR = 66.4 dBFS , SNR = 66.7 dBFS

— *fin* = 200 MHz
ENOB = 10.2 Bit , SNDR = 62.9 dBFS , SNR = 63.2 dBFS

## 5.0 Simplified Block Diagram

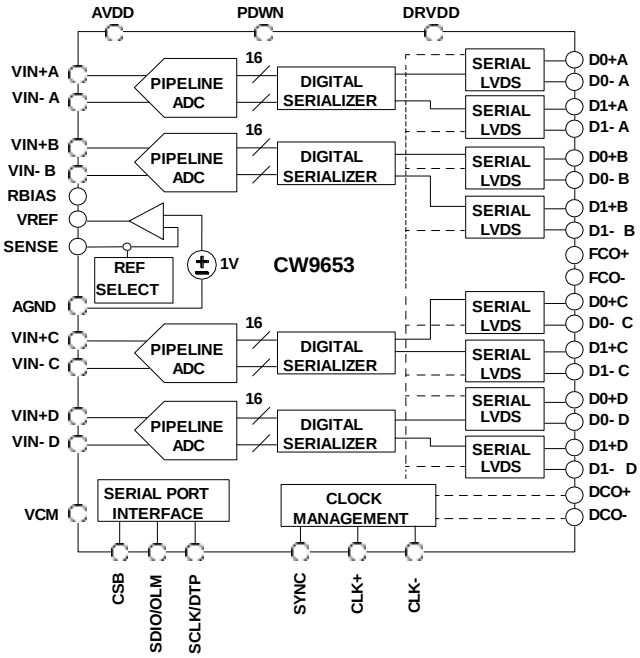


Figure5.1 CW9653 System Block Diagram



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## 6.0 Typical performance

Table6-1 Recommended chip usage conditions

| parameter | symbol | Notes | Numeric | unit |
|---|---|---|---|---|
| Supply voltage | $V_A$ | Analog circuit power supply | 1.8 | V |
| | $V_D$ | Output drive circuit power supply | 1.8 | V |
| Power-on sequence | | No power-up sequence required | | |
| land | $GND_A$ | Analog circuit ground | 0 | V |
| | $GND_{DR}$ | Output driver circuit ground | 0 | V |
| Differential input analog signal amplitude (1) | $V_{INIP} - V_{ININ}$<br>$V_{INQP} - V_{INQN}$ | Input signal differential amplitude | 400 | mVpp |
| Logic input high | $V_{IH}$ | | $V_A$ | V |
| Logic input low | $V_{IL}$ | | GND | |
| Clock differential input signal swing | $V_{CLKP} - V_{CLKN}$ | | $200 \le V_{CLKP} - V_{CLKN} \le 3600$ | mVpp |
| Clock frequency | $f_{MCLK}$ | | $f_{MCLK} \le 1000$ | MHz |
| Conversion rate | $f_S$ | | 20-125 | MSPS |
| Operating temperature range | $T_A$ | | $-55 \le T_A \le 125$ | ℃ |

**Note: (1) The measurement conditions are input frequency, full-scale sine wave, and a load of approximately 5pF per output bit.**



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Table6-2 Power supply, input and output electrical characteristics

Unless otherwise specified, AVDD = 1.8 V , DRVDD = 1.8 V , −1.0 dBFS The full-scale differential input is 2.0 V pp ; VREF = 1.0 V , DCS close.

| parameter | symbol | Minimum | Typical Value | Maximum | unit |
|---|---|---|---|---|---|
| Resolution | | | 16 | | Bits |
| Accuracy: | | | | | |
| No missing codes | | | 16 | | Bits |
| Offset Error | | | - 0.08 | | %FSR |
| Misalignment Matching | | | 0.05 | | %FSR |
| Offset Error Temperature Drift | | | 5.0 | | ppm/°C |
| Gain Error | | | 5 | | %FSR |
| Gain Matching | | | 1.5 | | %FSR |
| Integral Nonlinearity | INL | - 8.0 | 4 | 8.0 | LSB |
| Differential Nonlinearity | DNL | - 1.0 | 0.75 | +1.5 | LSB |
| Supply voltage: | | | | | |
| Analog circuit power supply | $V_A$ | 1.7 | 1.8 | 1.9 | V |
| Output drive circuit power supply | $V_D$ | 1.7 | 1.8 | 1.9 | V |
| Supply Current: | | | | | |
| Analog circuit power supply | $I_A$ | | 380 | | mA |
| Output drive circuit power supply | $I_{DR}$ | | 70 | | mA |
| Analog Input: | | | | | |
| Input differential analog signal amplitude | $V_{INIP} - V_{ININ}$ | 0.3 | 2 | $V_A$ | Vpp |
| Common mode voltage | $V_{CM}$ | | 0.9 | | V |
| Common mode range | | 0.75 | | 1 | V |
| Differential input resistance | $R_{IN}$ | | 2.6 | | kΩ |
| Internal reference voltage: | | | | | |
| Output voltage ( 1.0V model ) | $V_{REF}$ | | 1.0 | | V |
| Input resistance | | | 7.5 | | kΩ |
| Power consumption: | | | | | |
| DC input power consumption | | | 700 | | mW |
| Sine wave input power consumption | ANSI -644 model | | 760 | | mW |
| Sine wave input power consumption | Small output swing mode | | / | | mW |
| Shutdown power consumption | $P_D$ | | 10 | | mW |
| Standby power consumption | | | / | | mW |



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Table6-3 Digital specifications

| parameter | symbol | Minimum | Typical Value | Maximum | unit |
|---|---|---|---|---|---|
| Differential clock input **: CLK** ± | | | | | |
| Logic Compatibility | | | CMOS/LVDS LVPECL | | |
| Differential input voltage | | 0.2 | | 3.6 | $V_{P-P}$ |
| Input voltage range | | AGND - 0.2 | | AVDD+0.2 | V |
| Input common mode voltage | | | 0.9 | | V |
| Input resistance (differential ) | | | 15 | | kΩ |
| Input Capacitance | | | 4 | | pF |
| Logic Input: ( **PDWN/SYNC/SCLK** ) | | | 1.5 | | %FSR |
| High level input voltage | | 1.2 | | AVDD+0.2 | V |
| Low level input voltage | | 0 | | 0.8 | V |
| Input resistance | | | 30 | | kΩ |
| Input Capacitance | | | 2 | | pF |
| Logic Input ( **CSB/SDIO** ) **:** | | | | | |
| High level input voltage | | 1.2 | | AVDD+0.2 | V |
| Low level input voltage | | | 0.9 | | V |
| Input resistance | | | 30 | | kΩ |
| Input Capacitance | | | 2 | | pF |
| Digital Output ( **D0** ± **x/ D1** ± **x** ) **:** | ANSI -644 | | | | |
| Logic Compatibility | | | LVDS | | |
| Differential output voltage | | | 350 | | |
| Output offset voltage | | | 1.2 | | |
| Output Encoding | | | Two's complement | | |



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Table6-4 Dynamic characteristics ( reference )

Unless otherwise specified, AVDD = 1.8 V , DRVDD = 1.8 V , −1.0 dBFS The full-scale differential input is 2.0 V p-p ; VREF = 1.0 V , DCS close.

| parameter | symbol | Minimum | Typical Value | Maximum | unit |
|---|---|---|---|---|---|
| ***fs*** **= 125MSPS , V** ***in*** **= - 1 dBFS** | | | | | |
| Number of effective digits | | | | | |
| *fin* = 9.7MHz ( 25 ℃) | ENOB | 11 | 11.7 | | bit |
| *fin* = 15 MHz ( 25 ℃) | | | 11.7 | | bit |
| *fin* = 70 MHz ( full temperature ) | | | 11.3 | | bit |
| *fin* = 128 MHz ( 25 ℃) | | | 10.8 | | bit |
| *fin* = 200 MHz ( 25 ℃) | | | 10.2 | | bit |
| Signal-to-Noise Ratio | | | | | |
| *fin* = 9.7MHz ( 25 ℃) | SNR | 67 | 73 | | dBFS |
| *fin* = 15 MHz ( 25 ℃) | | | 72 | | dBFS |
| *fin* = 70 MHz ( full temperature ) | | | 69.5 | | dBFS |
| *fin* = 128 MHz ( 25 ℃) | | | 66.8 | | dBFS |
| *fin* = 200 MHz ( 25 ℃) | | | 64.3 | | dBFS |
| Sina ratio | | | | | |
| *fin* = 9.7MHz ( 25 ℃) | SINAD | 68.3 | 72.5 | | dBFS |
| *fin* = 15 MHz ( 25 ℃) | | | 72 | | dBFS |
| *fin* = 70 MHz ( full temperature ) | | | 70 | | dBFS |
| *fin* = 128 MHz ( 25 ℃) | | | 66.5 | | dBFS |
| *fin* = 200 MHz ( 25 ℃) | | | 61.5 | | dBFS |
| Spurious Free Dynamic Range | | | | | |
| *fin* = 9.7MHz ( 25 ℃) | \|SFDR\| | 81.5 | 87 | | dBc |
| *fin* = 15 MHz ( 25 ℃) | | | 86.3 | | dBc |
| *fin* = 70 MHz ( full temperature ) | | | 84 | | dBc |
| *fin* = 128 MHz ( 25 ℃) | | | 80.5 | | dBc |
| *fin* = 200 MHz ( 25 ℃) | | | 77.3 | | dBc |
| Second Harmonic | | | | | |
| *fin* = 9.7MHz ( 25 ℃) | \|2nd Harm\| | 84 | 90 | | dBc |
| *fin* = 15 MHz ( 25 ℃) | | | 89 | | dBc |
| *fin* = 70 MHz ( full temperature ) | | | 87.5 | | dBc |
| *fin* = 128 MHz ( 25 ℃) | | | 84.5 | | dBc |
| *fin* = 200 MHz ( 25 ℃) | | | 76 | | dBc |
| Channel isolation | | | 90 | | dB |
| Analog input bandwidth ( 25 °C) | | | 650 | | MHz |

Note **:** Crosstalk measurement conditions: one channel input parameters are **-1dBFS** , **70MHz** signal and no input signal on adjacent channels.



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## 7.0 Pin Configuration and Function Description

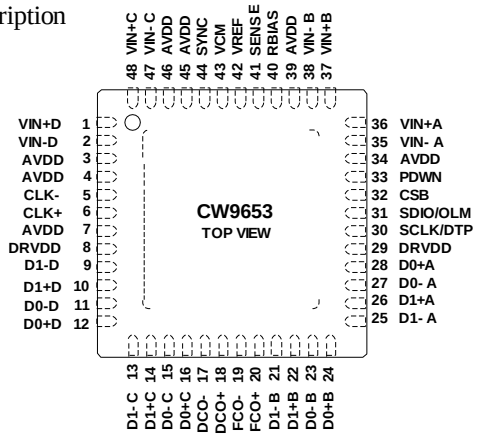


Figure7.1 CW9653 Pinout ( top view )

Table7- 1 Pin Function Description

| Pin number | symbol | achievement able |
|---|---|---|
| 0 | AGND,<br>Exposed Pad | Analog ground, pad exposed. The pad on the bottom of the package provides analog ground for the chip.<br>This exposed pad must be connected to ground for proper operation. |
| 1 | VIN+D | Channel D Analog Input + |
| 2 | VIN−D | Channel D Analog Input - |
| 3, 4, 7, 34,39, 45, 46 | AVDD | Analog power supply, 1.8 V |
| 5, 6 | CLK−, CLK+ | Differential clock input |
| 8, 29 | DRVDD | Digital output drive voltage source, 1.8V |
| 9, 10 | D1−D, D1+D | Channel D digital output |
| 11, 12 | D0−D, D0+D | Channel D digital output |
| 13, 14 | D1−C, D1+C | Channel C digital output |
| 15, 16 | D0−C, D0+C | Channel C digital output |
| 17, 18 | DCO−, DCO+ | Data clock output |
| 19, 20 | FCO−, FCO+ | Frame clock output |
| 21, 22 | D1−B, D1+B | Channel B digital output |
| 23, 24 | D0−B, D0+B | Channel B digital output |
| 25, 26 | D1−A, D1+A | Channel A digital output |
| 27, 28 | D0−A, D0+A | Channel A digital output |
| 30 | SCLK | SPI Clock Input |
| 31 | SDIO | SPI Data input and output |
| 32 | CSB | SPI Chip select bar, low enables operation, 30 kΩ Internal pull-up |
| 33 | PDWN | Digital input, 30kΩ Internal pull-down<br>PDWN high = turns the device off<br>PDWN low = device running, normal operation |
| 35 | VIN−A | Channel A Analog Input - |
| 36 | VIN+A | Channel A Analog Input + |
| 37 | VIN+B | Channel B Analog Input + |
| 38 | VIN−B | Channel B Analog Input - |
| 40 | RBIAS | Analog current bias, use a 10 kΩ ( 1%) resistor to ground |
| 41 | SENSE | Reference voltage mode selection |
| 42 | VREF | Reference voltage input / output |
| 43 | VCM | Analog input common mode voltage |
| 44 | SYNC | Digital input, divider synchronization input |
| 47 | VIN−C | Channel C Analog Input - |
| 48 | VIN+C | Channel C Analog Input + |



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## 8.0 Typical performance test curve

Unless otherwise specified, AVDD = 1.8 V , DRVDD=1.8 V , VIN=−1.0 dBFS Differential input , *fs* = 125MSPS , TA = 27°C 1.0 V Internal reference voltage.

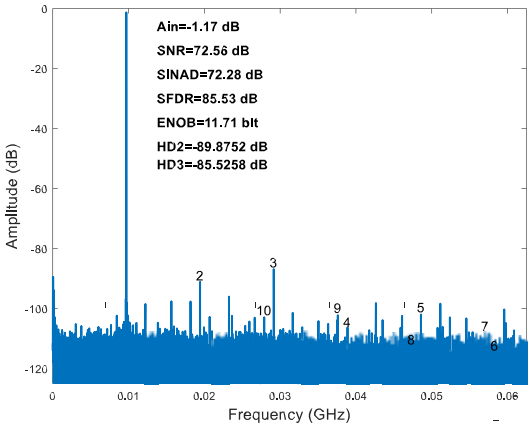


Figure 8.1 Single-tone FFT (fin = 9.7MHz@125MSPS)

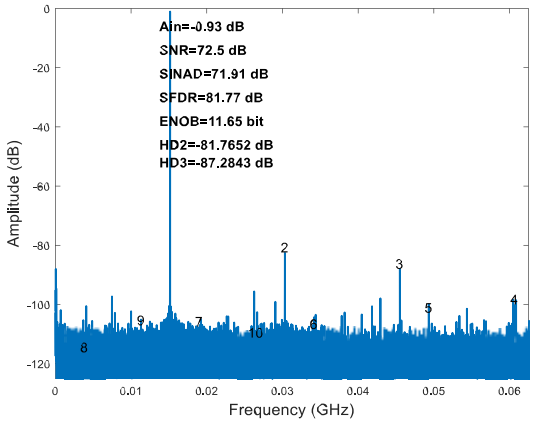


Figure 8.2 Single-tone FFT (fin = 15MHz@125MSPS

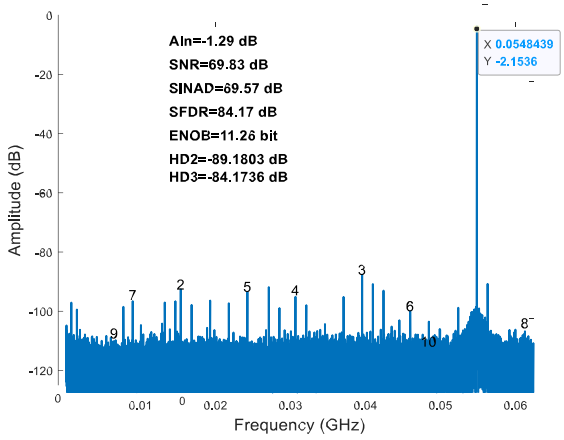


Figure 8.3 Single-tone FFT (fin = 70MHz@125MSPS

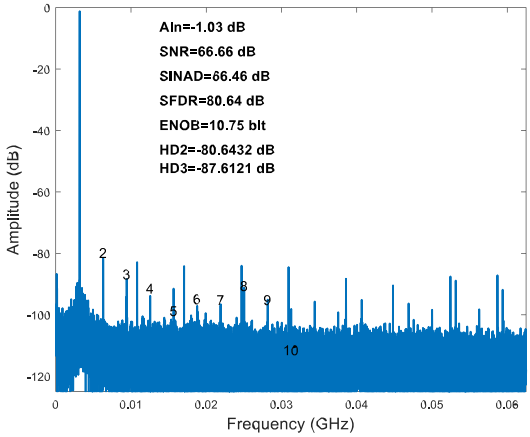


Figure 8.4 Single-tone FFT (fin = 128MHz@125MSPS

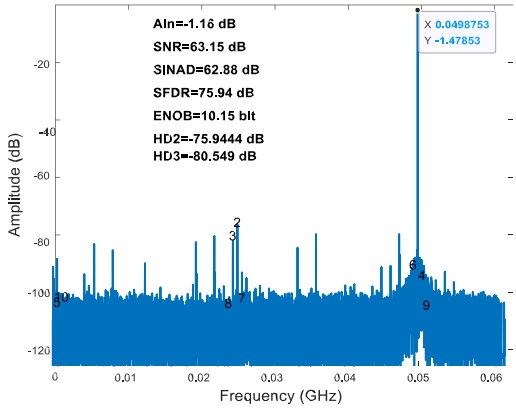


Figure 8.1 Single-tone FFT (fin = 200MHz@125MSPS

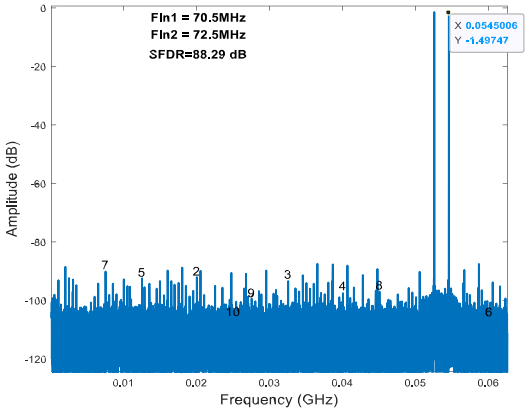


Figure 8.6 Two-tone FFT (fin1 = 70.5MHz and fin2 = 72.5MHz@125MSPS)



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## 9.0 Timing diagram

### 9.1 Data Timing

Unless otherwise specified, AVDD = 1.8 V , DRVDD=1.8 V , fs=125MSPS , VIN=−1.0 dBFS Differential input, 1.0 V Internal reference voltage.

| parameter | temperature | Minimum | Typical Value | Maximum | unit |
|---|---|---|---|---|---|
| Clock input parameters | | | | | |
| Input clock rate | Complete | 20 | | 1000 | MHZ |
| Conversion rate | Complete | 20 | | 125 | MHZ |
| Aperture | | | | | |
| Aperture delay ( $t_A$ ) | 25 ℃ | | 1 | | ns |
| Jitter | 25 ℃ | | 135 | | fs rms |
| Out of range recovery time | 25 ℃ | | 1 | | tcycle |
| Data output parameters | | | | | |
| Propagation delay $t_{PD}$ | | | 3 | | ns |
| FCO propagation delay $t_{FCO}$ | Complete | 1.5 | 2.3 | 3.1 | ns |
| DCO Propagation | Complete | | $t_{FCO}$ +( $t_{SAMPLE}$ /16) | | ns |
| DCO Delay to data | Complete | ( $t_{SAMPLE}$ /16)- 300 | ( $t_{SAMPLE}$ /16) | ( $t_{SAMPLE}$ /16)+300 | ps |
| DCO ToFCO Delay $t_{FRAME}$ | Complete | ( $t_{SAMPLE}$ /16)- 300 | ( $t_{SAMPLE}$ /16) | ( $t_{SAMPLE}$ /16)+300 | ps |
| Channel delay $t_{LD}$ | | | 90 | | ps |
| Wake-up time (standby ) | 25 ℃ | | 250 | | ns |
| Wake-up time ( power saving mode ) | 25 ℃ | | 375 | | us |
| Pipeline Delay | Complete | | 13 | | tcycle |

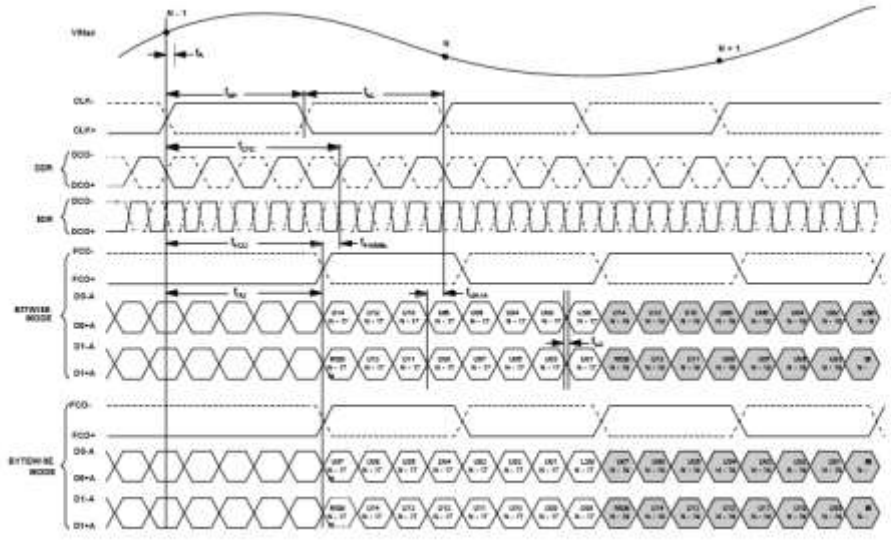

Figure9.1 16- Bit DDR/SDR, Two- Lane, 1 × Frame ( Default) working timing diagram



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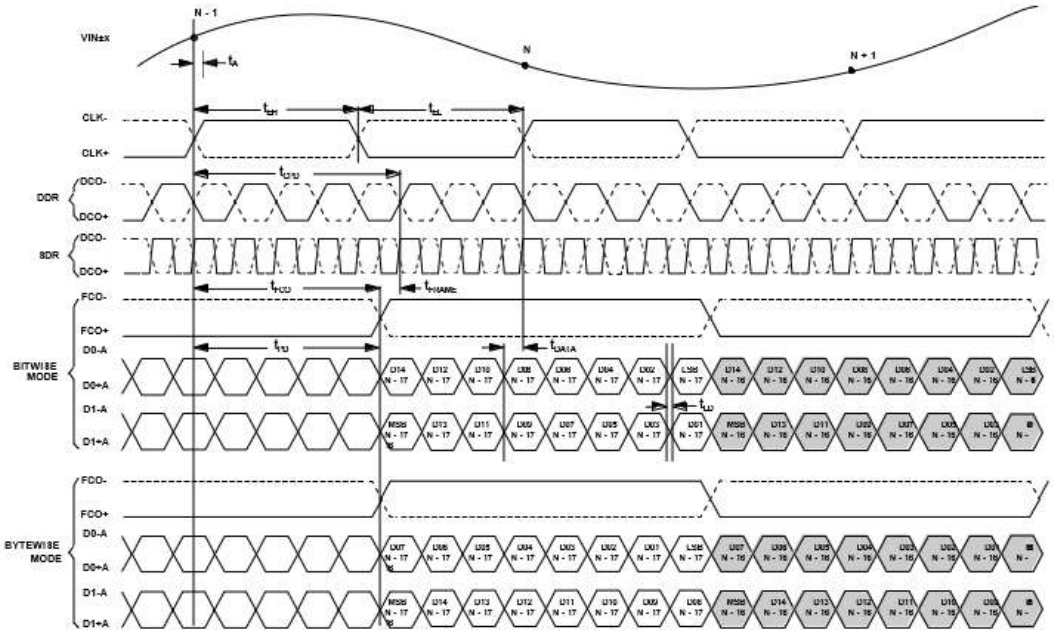


Figure 9.2 16- Bit DDR/SDR , Two- Lane , 2 × Frame
Working sequence diagram

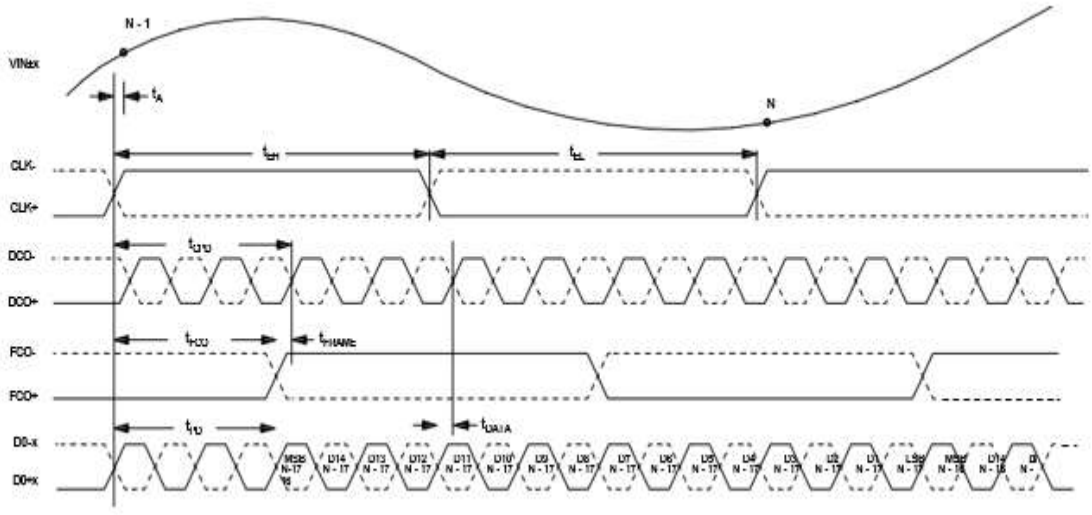


Figure 9.3 16- Bit Wordwise , One- Lane, 1 × Frame
Working sequence diagram



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**9.2 SPI** Interface Timing

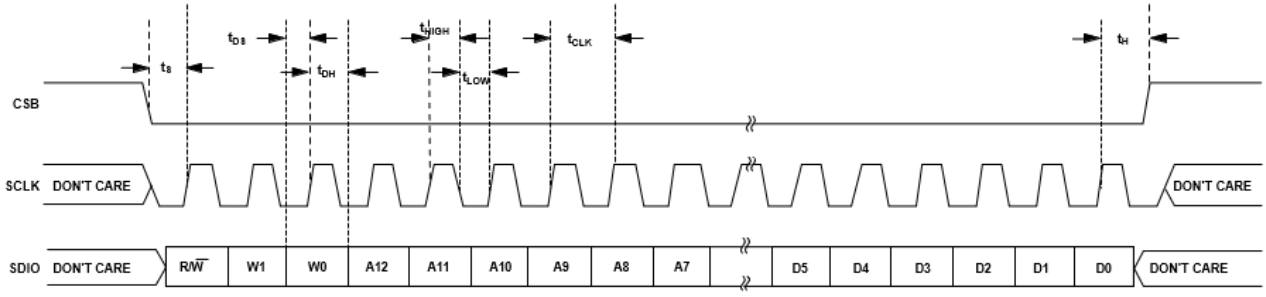


Figure 9.4 Serial port interface timing

Table9.2 SPI Timing parameters

| parameter | condition | Limits |
|---|---|---|
| $t_{DS}$ | Data and SCLK Setup time between rising edges | 2ns, min. |
| $t_{DH}$ | Data and SCLK Hold time between rising edges | 2ns, min. |
| $t_{CLK}$ | SCLK cycle | 40ns, min. |
| $t_S$ | CSB With SCLK The build time between | 2ns, min. |
| $t_H$ | CSB With SCLK Keep time between | 2ns, min. |
| $t_{HIGH}$ | SCLK High level pulse width | 10ns, min. |
| $t_{LOW}$ | SCLK Low level pulse width | 10ns, min. |



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**10.0** How it works

CW9653 It is a multi-stage, pipelined ADC with sufficient overlap in each stage to correct the flash of the previous stage. The quantized outputs of each stage are combined together to form a 1 6 The serializer converts the result in 1 6 This converted data is sent in a 10-bit output format. The pipelined architecture allows the first stage to process a new input sample while the other stages continue to process previous samples. Sampling occurs on the rising edge of the clock. Each stage of the pipeline, except the last, is controlled by a low-resolution Flash The ADC is composed of a switch capacitor DAC connected to it and an interstage residual amplifier ( such as a multiplying digital-to-analog converter (MDAC)) . The residual amplifier amplifies and reconstructs the DAC Output and Flash The difference between the input types is then provided to the next stage in the pipeline . The error is corrected digitally, with one bit of redundancy set at each level. The last level consists of only one Flash Type AD C The output stage blocks perform data alignment, error correction, and transfer data to the output buffer. The data is then serialized and aligned with the frame and data clocks.

**10.1** Analog Input Network

ADC The best performance is achieved by driving the analog inputs differentially. Using a differential double balun configuration to drive the CW9653 provides excellent performance and flexibility for baseband applications . interface ( see Figure 10.1 ) . When the input frequency is in the second or higher Nyquist zone, the noise performance of most amplifiers cannot meet the requirements to achieve CW9653 True SNR performance, differential transformer coupling is the recommended input configuration ( see Figure 10.2 ) . Regardless of the configuration, the parallel capacitor C1 The value of depends on the input frequency and may need to be reduced or removed.

Use the input network method of connecting VIN- to the common mode voltage and VIN+ to the input signal. This input method will cause the chip SNR to Therefore, it is not recommended to drive CW9653 single-ended.

enter.

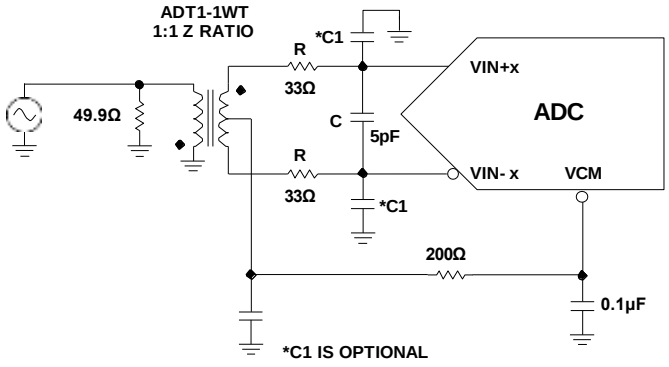


Figure 10.1 Differential Dual Balun Input Configuration



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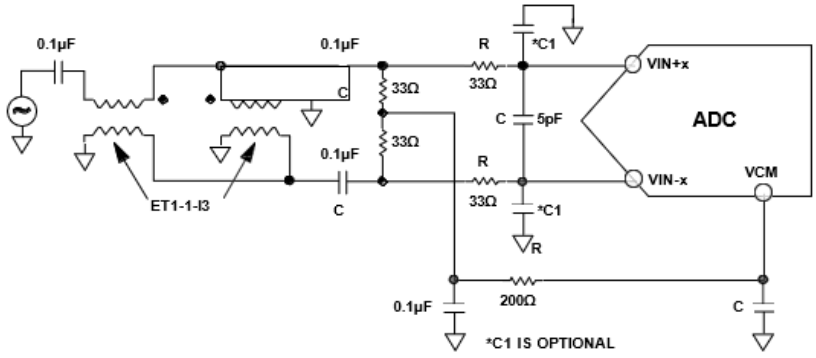


Figure 10.2 Differential Transformer Coupled Input Configuration

**10.2** Input common mode

CW9653 The analog inputs of the DAC have no internal DC bias. Therefore, in AC-coupled applications, the user must provide external bias. For best performance, it is recommended that the user set the device so that VCM = AVDD/2 ; however, the device will provide reasonable performance over a wider range, as shown in Figure 5 . and Figure 5 3 The chip provides an internal common-mode reference voltage through the VCM pin . A 0.1 μF Capacitance to VCM Bypass the A/D C pin to ground as described in the Applications Information section . Setting it to the maximum range can achieve the highest SNR performance. For CW9653 , the input range depends on the reference voltage and supports a maximum of 2Vp - p Input range.

**10.3** Clock Input

the chip, a differential signal should be used as CW9653 The sampling clock input ( CLK+/- ) clock signal. The input clock pin has an internal bias and does not require an external bias. The recommended sampling RF transformer configuration is shown in Figure 1 0 .3 The back-to-back Schottky diodes connected across the transformer can connect the input to the CW9653 middle

The clock signal is limited to approximately 0.8V differential This prevents the large voltage swing of the clock from feeding through to other parts, while also preserving the fast rise and fall times of the signal.

This is very important for low jitter performance.



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CW 9653 Flexible clock input structure. CMOS , LVDS , LVPECL Either a sine wave or a sinusoidal signal can be used as the clock input signal. Regardless of which signal is used, the clock source jitter must be considered ( see the jitter consideration section for details ) . and1 0 .4 MCW9653 The preferred method for providing a clock signal ( clock rate before internal clock division can reach 1 GHz) . Using an RF transformer or RF balun, the single - ended signal of the low-jitter clock source can be converted into a differential signal . M Z to1 GH For clock frequencies of 2 0 MHz to 2 0 0 M Z The back-to-back Schottky diodes across the transformer / balun secondary winding can provide a high clock frequency for the CW9653 . The clock signal in the V This prevents the large voltage swing of the clock from feeding through to other parts of the CW9653 while preserving the fast rise and fall times of the signal, which is important for achieving low jitter performance. However, when the frequency is above 500 M Z The diode capacitance becomes an issue when the signal is limited. Care must be taken to select the appropriate signal limiting diode.

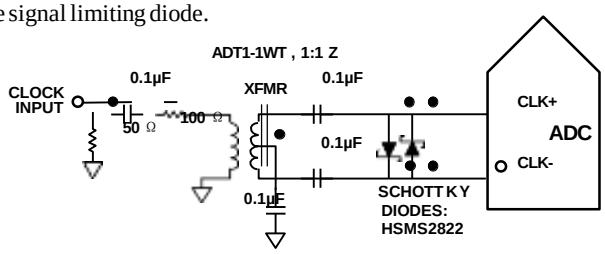


Figure 10.3 Transformer coupled differential clock

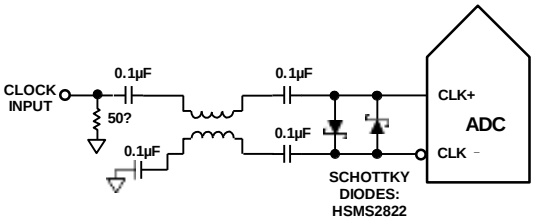


Figure 10.4 Balun coupled differential clock

**10.4** Input clock divider

CW9653 A built-in input clock divider can be used to divide the input clock by 1 to8 Integer frequency division. Using external SYNC Input signal, can synchronize Clock divider. By register 0x109 Bit 0 and bit 1 for writing, you can set each time you receive SYNC signal or only the first time SYNC is received The clock divider is resynchronized after the SYNC signal. This synchronization allows the clock dividers of multiple devices to be aligned, ensuring that the inputs are sampled simultaneously.

**10.5** Clock Duty Cycle

Typical high speed ADC The internal timing signals are generated using two clock edges and are therefore very sensitive to the clock duty cycle . Dynamic

Yes, the clock duty cycle tolerance should be ±5% .

CW 9653 duty cycle stabilizer (DCS) is built in to retime the non-sampling edge ( falling edge ) and provide an internal clock signal with a nominal 50% duty cycle. This feature minimizes performance degradation when the clock input duty cycle deviates from the nominal 50% by more than ±5 % . W h e n the DCS When enabled, noise and distortion performance are nearly flat.

edge is still very important and cannot be reduced by the internal stabilization circuit . M Z The duty cycle control loop fails when In applications where the clock rate changes dynamically, the time constants associated with the loop must be considered. A 1.5 ms wait is required before the DCS loop relocks to the input signal . µs to5 µs CW 9653 DCS It is disabled by default and can be enabled via SPI interface to turn it on, **CW9653** When the chip uses the frequency division function, the duty cycle stabilizer must be turned on to work properly.

**10.5** Benchmark configuration

The CW 9653 has a built-in stable, accurate voltage reference. The VREF can be configured with an internal 1.0 V reference voltage, an externally applied 1.0 V to 1.3 V reference voltage, or an external resistor applied to the internal reference voltage to produce a reference voltage according to the user's choice. For a summary of the various reference modes, see the Internal Reference Connection section and the External Reference Configuration section. The VREF pin should be bypassed to ground by an external parallel combination of a low ESR 0.1 uF ceramic capacitor and a low ESR 1.0 uF capacitor.

CW9653 The built-in comparator can detect the SENSE pin , thereby configuring the reference voltage into one of three possible modes ( see Table 10.1) . If the SENSE pin is grounded, the reference amplifier switch is connected to the internal resistance divider (see Figure 10.4), thus setting the voltage VREF of the VREF pin to 1.0 V. If SENSE is connected to an external resistive divider (see Figure 10.5), VREF is defined as follows: VREF = 0.5 × (1 + R2/R1)



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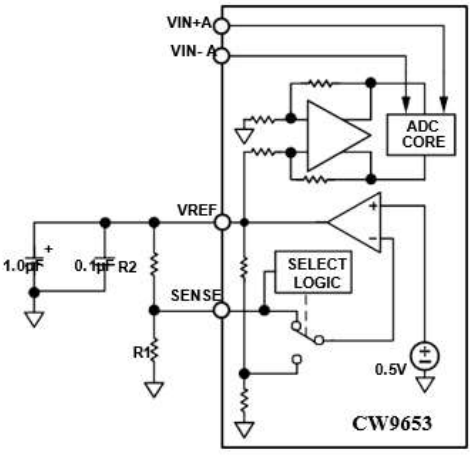


Figure 10.5 1.0V Internal Reference Voltage Configuration

It is possible to further increase the A/D C by using an external reference voltage. Gain accuracy and thermal drift characteristics . Pin and AVD D When connected, the internal reference voltage can be disabled , allowing the use of an external reference voltage. The internal reference buffer is equivalent to 7.5 kΩ The internal buffer generates positive and negative full-scale reference voltages for the ADC core . It is not recommended to leave SENSE floating. Pin.

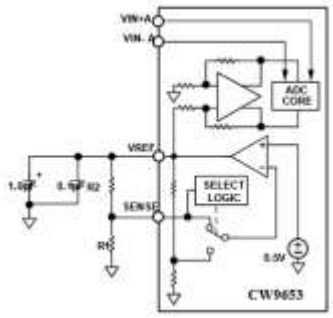

Figure 10.5 Programmable Internal Reference Configuration

Table 10.1 Reference Voltage Configuration Summary

| Selected Mode | SENSE Voltage | The corresponding VREF ( V ) | Corresponding differential range ( Vpp ) |
|---|---|---|---|
| Fixed external reference voltage | AVDD to 0.2 | 1.0 , internal | 2.0 |
| Programmable internal voltage reference | External Resistor Configuration | 0.5 × ( 1 + R2/R1 ) | 2 × V REF |
| Fixed internal reference voltage | AGND to 0.2 | 1.0 to 1.3 , by external V REF Pins provided | 2.0~2.6 |



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## **10.4** Digital output format

CW9653 Output driver is LVDS Interface, timing as shown in Figure 9.1 The output driver should be able to provide sufficient output current to drive various logic circuits, and the driving force can be adjusted through the register. However, large drive current may cause glitch pulses in the power supply signal, affecting the performance of the converter. Therefore, external buffers or latches may be required in applications that require an ADC to drive large capacitive loads or large fan-outs. The default format of the output data is binary complement. An example of the output encoding format is shown in Table 11.2. To change the output data format to offset binary code, please refer to the "Memory Mapping" section.

See Table 11.2 for an example . To change the output data format to offset binary code, refer to the “Memory Map” section.

In DDR In this mode, from each ADC The data is serialized and provided through different channels. The data rate of each serial stream is equal to 1 6 bits multiplied by the sampling clock rate , maximum 5 0 0 per channel Mbps [( 16 Bit × 125 MSPS)/(2 × 2 ) = 5 0 0 Mbps/ channel ] . The typical minimum conversion rate is 2 0 MSPS . See the Memory Map section for more information on using this feature .

To aid in capturing data from the CW9653 , the device provides two output clocks . Used to time the output data. In the default operating mode, it is equal to 4 times the sampling clock (CLK) rate. The data were obtained from CW9653 output, must be at DCO The rising and falling edges of DCO are captured; Supports double data rate (DDR) capture. The FCO is used to indicate the start of a new output byte and is equal to the sampling clock rate in

Table10.2 Data output format

| Input ( V) | condition | Offset Binary Mode | Two’s complement mode |
|---|---|---|---|
| VIN+ - VIN- | < - VREF – 0.5LSB | 0000 0000 0000 0000 | 1000 0000 0000 0000 |
| VIN+ - VIN- | = - VREF | 0000 0000 0000 0000 | 1000 0000 0000 0000 |
| VIN+ - VIN- | =0 | 1000 0000 0000 0000 | 0000 0000 0000 0000 |
| VIN+ - VIN- | =+VREF – 1LSB | 1111 1111 1111 1100 | 0111 1111 1111 1100 |
| VIN+ - VIN- | > +VREF – 0.5LSB | 1111 1111 1111 1100 | 0111 1111 1111 1100 |

When using SPI, the DCO phase can be adjusted in 60 ° increments with respect to one data period (30 ° with respect to one DCO period). This enables the user to optimize the system timing margin as needed. As shown in Figure 9.1, the default DCO ± output data edge timing is 180 ° relative to a data cycle (90 ° relative to a DCO cycle).

In the default mode, as shown in Figure 9.1, the MSB is first in the data output serial stream. This can be reversed by using SPI so that the LSB is in the first place in the data output serial stream.



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### 10.5 Output test mode

The output test options are listed in Table 10.3 and is represented by address 0 x 0 D When the output test mode is enabled, the AD C The analog portion of the ADC is disconnected from the digital backend block and the test patterns are run through the output format block. Some test patterns are constrained by the output format and some are not . Position 4 or Bit 5 , it is possible to reset the PN generator in the PN sequence test . These tests can be performed with the analog signal ( ignoring the analog signal if present ) , but require a clock signal. Table 10.3 Flexible output test modes

| Output Test Trial Mode Bit Sequence | Mode Name | Digital output word 1 | Digital output word 2 | accept data Format Selection | Notes |
|---|---|---|---|---|---|
| 0000 | Off (default) | N/A | N/A | N/A | |
| 0001 | Mid-level short code | 1000 0000 0000 0000 (16- bit) | N/A | Yes | Offset Binary Code |
| 0010 | Positive full scale | 1111 1111 1111 1111(16- bit) | N/A | Yes | Offset Binary Code |
| 0011 | Negative full scale | 0000 0000 0000 0000 (16- bit) | N/A | Yes | Offset Binary Code |
| 0100 | Chessboard | 1010 1010 1010 1010 (16- bit) | 0101 0101 0101 0101 (16- bit) | No | |
| 0101 | PN code long sequence | N/A | N/A | Yes | PN23<br>ITU 0.150<br>$X^{23} + X^{18} + 1$ |
| 0110 | PN code short sequence | N/A | N/A | Yes | PN9<br>ITU 0.150<br>$X^{9} + X^{5} + 1$ |
| 0111 | 1/0 word flip | 111 1111 1111 1111(16- bit) | 0000 0000 0000 0000 (16- bit) | No | |
| 1000 | User Input | Register 0x19 to Register 0x1A | Register 0x1B to Register 0x1C | No | |
| 1001 | 1/0 bit flip | 1010 1010 1010 1010 (16- bit) | N/A | No | |
| 1010 | 1×sync | 0000 0001 1111 1111 (16- bit) | N/A | No | |
| 1011 | 1 bit high level | 1000 0000 0000 0000 (16- bit) | N/A | No | Related to external pins<br>Test code |
| 1100 | Mixing frequency | 1010 0001 1001 1100 (16- bit) | N/A | No | |

Table10.4 PN Sequence

| sequence | Initial Value | The next three output samples ( MSB Two 's complement |
|---|---|---|
| PN Code short sequence | 0x7F83 | 0x5F17 , 0xB209 , 0xCED1 |
| PN Code length sequence | 0x7FFF | 0x7E00 , 0x807C , 0x801F |

How to use SPI See the Register Listing for information on changing the timing characteristics of these additional digital outputs.

### 10.6 CSB Pin

For applications that do not require SPI For applications that require SDIO mode operation, theCSB pin should be tied to AVDD . By setting CSB high, all SCLK andSDIO information will be ignored. Pin connected to AVDD When, CW9653 , DCS It is enabled by default and remains enabled until the device enters SPI mode and through SPI control.

### 10.7 RBIAS Pin

CW9653 requires the user to set a 10 kΩ Resistor placed at RBIAS pin and ground. This resistor is used to set the ADC The resistor tolerance is at least 1% .



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**10.8** Serial Port Interface ( **SPI** )

The CW9653 serial port interface ( SPI ) allows the user to configure the A/ D C The corresponding internal function registers can meet the needs of specific functions and operations. The address space can be accessed and read and written through the serial port . SPI It consists of three parts: SCLK Pin, SDIO Pin and CSB The SCLK ( serial clock ) pin is used to synchronize the A/ D The SDIO (serial data input / output) dual-function pin allows data to be sent to or read from the internal registers ; the CSB (chip select signal ) pin is a low-level active control pin that can enable or disable the read and write cycles. The timing requirements are shown in Figure 9.4 shown.

**11.0** Application Information

**11.1** Power and Grounding Recommendations

It is recommended to use two independent 1.8V Power supply is CW9653 Power supply: one for analog terminal AVDD , one for digital output terminal DRVDD .and DRVDD , multiple different decoupling capacitors should be used to support high and low frequencies. The decoupling capacitors should be placed close to the PCB The entry point should be located close to the device pins and the trace length should be kept as short as possible. CW9653 Only one PCB required Ground plane . Reasonable decoupling and clever separation of analog, digital and clock modules can easily achieve the best performance.

**11.2** Exposed Pad Heatsink Recommendations

To achieve the best electrical and thermal performance, the AD C The exposed pad on the bottom is connected to the analog ground AGND . The exposed continuous copper plane on the PCB should match the exposed pad of the CW9653 . There should be multiple vias in the copper plane to obtain the lowest possible thermal resistance path for heat dissipation through the bottom of the PCB . These vias should be filled or plugged to prevent tin seepage from the vias and affect the connection performance. To maximize the A/D C With PCB The coverage and connection between them should be on the PCB A silk screen layer is covered on the PCB to The continuous plane on the A/D C is divided into multiple equal parts. In this way, during the reflow process, A continuous, undivided plane only guarantees multiple connection points betweenthe A/D C There is one connection point tothe PCB .

**11.3 VCM**

VCM The pin should be connected through a 0.1uF Capacitor decoupling to ground.

**11.4** Reference Decoupling

VREF pin should be connected to an external low ESR 0.1uF ceramic capacitor and a low ESR 1.0uF Parallel decoupling capacitor to ground.

**11.15 SPI** port

When the full dynamic performance of the converter is required, the SPI should be disabled. port. Usually SCLK Signal, CSB Signals and SDIO Signal and ADC The clocks are asynchronous, so noise in these signals can degrade converter performance. bus, you may need to connect the bus to the CW9653 A buffer is connected between the two to prevent these signals from changing at the input of the converter during the critical sampling period.



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## 12.0 Register List

The register map is roughly divided into the following sections: chip configuration registers, device index registers and transfer registers, and global ADC function registers, including setup, control and test functions.

| address (HEX) | Register Name | Bit 7 (MSB) | Position 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | default value (HEX) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Chip Configuration Register | | | | | | | | | | | |
| 0x00 | SPI Interface Configuration ( Global ) 1 | 0 | LSB priority | Soft Reset | 1 | 1 | Soft Reset | LSB excellent First | 0 | 0x18 | Recommended power-up Post-Write 3C , soft reset once |
| 0x01 | Chip ID ( full Bureau ) | 8 -bit chip ID[7:0] ( CW9653 = 0x95 ) | | | | | | | | 0x00 | Read-only |
| 0x02 | Chip level ( Global ) | Disable | Speed Class ID 100 = 125MSPS | | | Disable | Disable | Disable | Disable | 0x60 | Read-only |
| Channel Index and Transfer Registers | | | | | | | | | | | |
| 0x05 | Channel Index | Disable | Disable | Clock channel DCO | Clock channel FCO | Data Channel D | Data Channel C | Data Channel B | Data Channel A | 0x0F | The default four channels and DCO , FCO Select All |
| **ADC** Function | | | | | | | | | | | |
| 0x08 | Power Mode ( Global ) | Disable | Disable | External power-down pin Function ( Partial ) 0 = Power off 1 = Standby | Disable | Disable | Disable | Internal power down mode ( local ) 00 = normal operation 01 = Complete power down 10 = Standby 11 = Reserved | | 0x00 | Determines the general operating mode of the chip |
| 0x09 | Global clock (Global ) | Disable | Disable | Disable | Disable | Disable | Disable | Disable | Duty Cycle Stabilizer **1** = On **0** = Off | 0x01 | Differences from imported products |
| 0x0B | Clock Divider (Global ) | Disable | Disable | Disable | Disable | Disable | Clock division ratio 000 = 1 Frequency division 001 = 2 Frequency division 010 = 3 Frequency division 011 = 4 Frequency division 100 = 5 Frequency division 101 = 6 Frequency division 110 = 7 Frequency division 111 = 8 Frequency division | | | 0x00 | |
| 0x0D | Test Mode ( Partial ) | User Input Test Mode 00 = Single 01 = Alternate | | Generate reset PN Long Sequence | Generate reset PN short sequence | Output test pattern [3:0] ( local ) 0000 = Off ( default ) 0001 = mid-scale short sequence 0010 = Positive FS 0011 = Negative FS 0100 = Alternating chessboard pattern 0101 = PN twenty three sequence 0110 = PN 9 sequence 0111 = 1/0 Word Reversal 1000 = User input 1001 = 1/0 Bit Reversal 1010 = 1× sync 1011 = 1 High level 1100 = Mixed bit frequency | | | | 0x00 | For detailed information on how to configure the test code, see "Digital Test Code Configuration Method" |
| 0x10 | Offset Adjustment ( Partial ) | 8 -bit device offset adjustment, bits [7:0] Offset adjustment in LSB Units, from +127 to -128 ( two's complement format ) | | | | | | | | 0x00 | Offset Error Adjustment |
| 0x14 | Data output mode | Disable | LVDS Amplitude 0 = 350mv 1 = 200mv | Disable | Disable | Disable | Output reverse | Disable | Output Format (Global ) 0 = Offset binary 01 = Two's complement | 0x01 | Configuring output and data formats |
| 0x15 | Output Adjustment | Disable | Disable | Output driver terminals 00 = None | | Disable | Disable | Disable | Output drive strength ( local ) | 0x00 | LVDS Output Configuration |



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| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 01 = 200 Ω<br>10 = 100 Ω<br>11 = 100 Ω | | | | 0 = 1 × drive<br>1 = 2 × drive | | |
| 0x16 | Output Phase | Disable | Input clock phase adjustment [6:4] ( value is the number of input clock cycles for phase delay ) | Output clock phase adjustment [3:0] (0000 to 1011) | | | | | 0x03 | In utilizing the whole Local clock frequency division device, decide to use frequency division Which phase of the output supply Output The internal latch does not Affected. |
| 0x18 | VREF Adjustment | Disable | Disable | Disable | Disable | Disable | VREF Adjustment plan [2:0]<br>000=1.0Vpp ( 1.3Vpp )<br>001=1.14Vpp ( 1.48Vpp )<br>010=1.33Vpp ( 1.73Vpp )<br>011=1.6Vpp ( 2.08Vpp )<br>100=2.0Vpp ( 2.6 Vpp ) | | | 0x04 | Adjust the interior VREF value |
| 0x19 | USER_PATT 1LSB( global ) | | | | | | | | | 0x00 | User defined Test 1LSB |
| 0x1A | USER_PATT 1MSB ( global ) | | | | | | | | | 0x00 | User defined Test 1MSB |
| 0x1B | USER_PATT 2LSB( global ) | | | | | | | | | 0x00 | User defined Test 2LSB |
| 0x1C | USER_PATT 2MSB ( global ) | | | | | | | | | 0x00 | User defined Test 2MSB |
| 0x21 | Serial output data control ( global ) | LVDS Input LSB priority | SDR/DDR Single / dual channel, bit by bit / bit by bit<br>Byte [6:4]<br>000 = SDR Dual channel, bit by bit<br>001 = SDR Dual channel, byte by byte<br>010 = DDR Dual channel, bit by bit<br>011 = DDR Dual channel, byte by byte<br>100 = DDR Single channel, verbatim | | | Disable | Select 2X frame | Serial output bits<br>00=16 Bit | | 0x30 | User defined Test 2MSB |
| 0x22 | Serial channel status ( local ) | Disable | Disable | Disable | Disable | Disable | Disable | Channel output reset | Channel power down | 0x30 | Serial flow control The default is MSB priority |
| 0x109 | synchronous | Disable | Disable | Disable | Disable | Disable | Disable | Synchronizes only with the next sync pulse | Use Synchronization | 0x00 | |



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**13.0** Packaging information

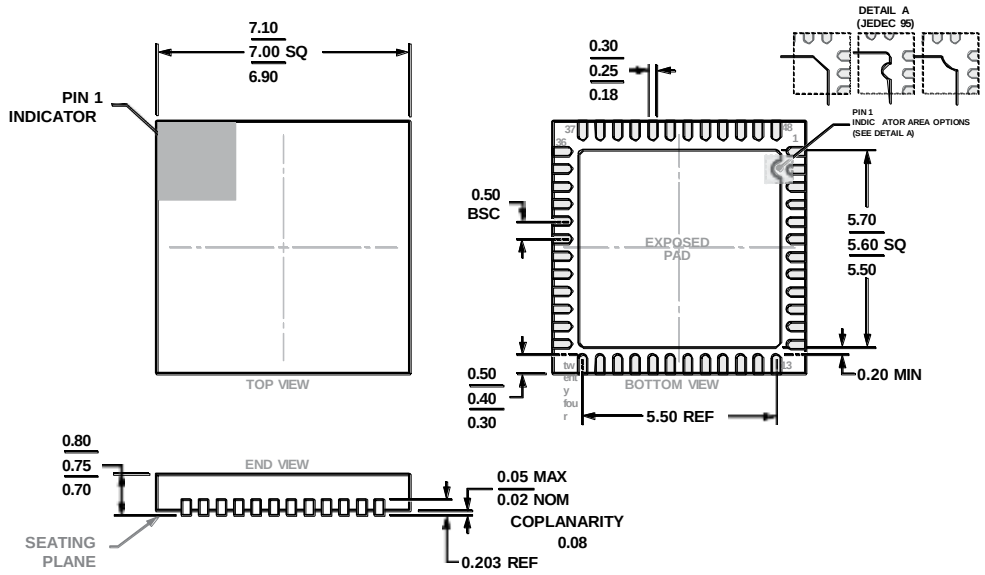


Figure 10.1 CW9653 QFN- 48 Package Outline

**10.1** Ordering Information

| Order Model | Operating temperature | Package | Implementation standards ( quality levels ) |
|---|---|---|---|
| CW9653 | -55℃~+125℃ | QFN- 48 | Military temperature level |



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