CW12D1800 Data Sheet

Dual Channel 12-bit, 1.8 GSPS High Speed ADC

1.Overview

The CW12D1800 is a 12-bit high-speed ADC product with two built-in 12-Bits.

1.8 GSPS high-speed ADC, each channel ADC has independent DDR data clocks (DCLKI and DCLKQ). When both channel ADC are operating, DCLKI and DCLKQ are always in phase, so only one of them can be used to collect all data. If 1:2 Demux mode is selected, another set of 12-Bit LVDS buses are enabled so that the data rate of each set of LVDS changes to 1/2 of the Non-Demux mode to reduce the timing requirements for data capture.

The CW12D1800 supports AutoSync function and can be used for multi-chip cascade. The product package is plastic-sealed BGA292 package, with an operating temperature of -55℃ ~ 105℃. The CW12D1800 achieves excellent dynamic performance with low power consumption below 2.4W.

The data output format of the CW12D1800 can be programmed to offset binary code and complement code, and output data using an LVDS interface that complies with international common standards. The output common mode can be adjusted at two voltages: 0.8V and 1.2V.

CW12D1800 and CW12D1600/ CW12D1000/CW10D1500/ CW10D1000 pin compatible.

2 Applications

- RF direct down-conversion
- High-speed data acquisition system
- Ultra-wideband satellite data reception
- Automatic test equipment
- High-speed test instrument
- Wideband radar
- Electronic countermeasures

3 Features

- Built-in dual-channel 1.8 GSPS ADC
- Low power consumption, no heat sink required
- Built-in terminal resistor (automatic calibration), buffer
- Provides test sequences for system debugging and batch testing
- 1:1 Non-Demux or 1:2 Demux LVDS data output
- Multi-chip automatic synchronization function
- Single power supply 1.9 V
- 292-BGA (27mm × 27mm × 1.7mm, 1.27mm ball spacing)
- Pin and CW12D1600/CW12D1000/CW10D1500/CW10D1000 compatible

4 Performance indicators

- Full power bandwidth: 3.0 GHz
- Data delay: 28 master clock cycles
- Static performance: DNL -0.9/+1.5 LSB, INL -2.3/+2.8 LSB
- Dynamic performance (fs = 1.8 GSPS, input signal power -1 dBFS)
  - fin=248MHz
    ENOB = 8.7 Bit, SFDR = 64.7 dBFS, SNR = 54.1 dBFS
  - fin=498MHz
    ENOB = 8.5 Bit, SFDR = 64.8 dBFS, SNR = 52.8 dBFS
  - fin = 998 MHz
    ENOB = 8.0 Bit, SFDR = 60.1 dBFS, SNR = 49.9 dBFS
  - fin=1147 MHz
    ENOB = 7.9 Bit, SFDR = 60.1 dBFS, SNR = 49.4 dBFS
  - fin=1448 MHz
    ENOB = 7.7 Bit, SFDR = 59.3 dBFS, SNR = 48.5 dBFS

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5 Simplified block diagram

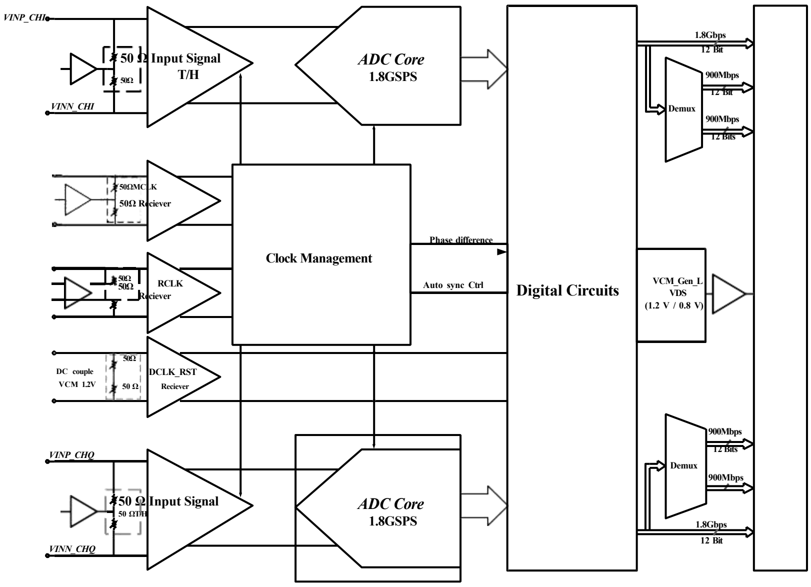

Figure 5.1 CW12D1800 system block diagram

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6 Typical Performance

Table 6-1 Chip usage conditions

Parameter	Symbol	Comments	Value	Units
Power supply voltage	V_A	Analog circuit power supply	1.9	V
	V_{TC}	Sample hold and clock circuit power supply	1.9	V
	V_{DR}	Output driver circuit power supply	1.9	V
	V_E	Digital circuit power supply	1.9	V
Power-on sequence		No power-on sequence requirement		
Ground	GND	Analog circuit ground	0	V
	GND_{TC}	Sample hold and clock circuit ground	0	V
	GND_{DR}	Output driver circuit ground	0	V
	GND_E	Digital circuit ground	0	V
Differential input analog signal amplitude	VinIp –VinIn VinQp –VinQn	Channel analog input signal differential amplitude	800	mVpp
Logic input high level	V_I		VA	V
Logic input low level	V_{IL}		GND	
Clock differential input signal amplitude	$V_{CLKP} - V_{CLKN}$	Clock input signal differential amplitude	600	mVpp
Clock frequency	f_{CLK}		$0.5 \le f_{CLK} \le 1.8$	GHz
Operating temperature range	T_C		$-55 \le T_C \le 105$	℃

Table 6-2 Thermal resistance parameters

parameter	**symbol**	**Typical values**	**unit**
Thermal resistance between the junction and the environment	$\mathbf{R_{\theta JA}}$	22.9	℃/W
Thermal resistance between the junction and the top of the package	$\mathbf{R_{\theta JC}}$	7.7	℃/W
Thermal resistance between the junction and the circuit board	$\mathbf{R_{\theta JB}}$	17.9	℃/W

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Table 6-3 Electrical characteristics of power supply, input and output

The chip operates in Demux and Non-DES modes, and $V_A = V_{DR} = V_{TC} = V_E = +1.9V$, AC coupled signal input, unused channel termination is connected to "AC ground", AC coupled sine wave sampling clock, f_{CLK} = 1.8 GHz; $R_{ext} = R_{trim}$ = 3300 Ω ± 0.1%; input source impedance 50 Ω; TA = 25 °C.

parameter	symbol	Minimum value	Typical values	Maximum value	unit
Resolution			12		
Power supply voltage:					
Analog circuit power supply	V_A	1.8	1.9	2.0	V
Sampling and holding and clock circuit source	V_{TC}	1.8	1.9	2.0	V
Output drive circuit	V_{DR}	1.8	1.9	2.0	V
power supply					
Digital circuit power supply	V_E	1.8	1.9	2.0	V
Power supply current:					
Analog circuit power supply	I_A		19		mA
Sampling and holding and clock circuit source	I_{TC}		680		mA
Output drive circuit power supply	I_{DR}		370		mA
Digital circuit power supply	I_E		185		mA
Power consumption	P_D				
PDI = PDQ = GND			2.38		W
PDI = GND, PDQ = V_A			1.2		W
PDI = V_A, PDQ = GND			1.2		W
PDI = V_A, PDQ = V_A			1.9		mW
Data input					
Input differential analog signal amplitude	VinIp – VinIn		800		mVpp
	VinQp – VinQn		800		mVpp
Differential input resistance	R_{IN}	95	100	105	Ω

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Table 6-4 Electrical characteristics of power supply, input and output (continued)

Parameter	Symbol	Minimum value	Typical value	Maximum value	Unit
Clock input					
Clock source type					Differential sine wave
Clock input differential swing	$V_{CLKP} - V_{CLKN}$	400	600	1000	mVpp
Clock differential input resistance	R_{CLK}	95	100	105	Ω
External clock jitter requirement	Jitter			100	fs
Clock duty cycle requirement	Duty Cycle	40	50	60	%
Multi-chip DCLK_RST Sync signal					
Logic compatibility	LVDS				
Input voltage:					
Logic low	V_{IL_DRST}			1.1	V
Logic high	V_{IH_DRST}	1.3			V
Swing	V_{ID_DRST}		350		mV
Common-mode voltage	V_{CM_DRST}		1.20		V
Input resistance	R_{DRST}	95	100	105	Ω
Multi-chip RCLK synchronization signal					
Logic compatibility	LVDS				
Input voltage:					
Logic low	V_{IL_RCLK}			1.1	V
Logic high	V_{IH_RCLK}	1.3			V
Swing	V_{ID_RCLK}		350		mV
Common-mode voltage	V_{CM_RCLK}		1.20		V
Input resistance	R_{RCLK}	95	100	105	Ω
SPI					
Low-level input voltage	V_{IL_SPI}	0		$0.3 \times V_A$	V
High-level input voltage	V_{IH_SPI}	$0.7 \times V_A$		V_A	V
Low-level output voltage	V_{OL_SPI}			0.3	V
High-level output voltage	V_{OH_SPI}	1.6			V
Serial clock frequency	f_{SCLK}			10	MHz

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Digital signal output (including data, clock and over-range indication; 50Ω transmission line, 100Ω differential termination)					
Logic compatibility	LVDS				
Swing (single-sided)	V_{OD}	300	350	400	mVpp
Common-mode voltage	V_{CM_LVDS}		1.2/0.8		V
Output data delay	t_{LAT}		28		Sampling clock period
Data output rising edge (20 pF)	t_{LHT}		220		ps
Data output falling edge (20 pF)	t_{HLT}		220		ps
Clock data output deviation	t_{OSK}	180		350	ps
Clock data setup time (90°)	t_{SU}		350		ps
Clock data hold time (90°)	t_H		400		ps

Table 6-5 Static characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Differential nonlinearity	DNL	-0.84		1.16	LSB
Integral nonlinearity	INL	-2.54		2.85	LSB
Output offset error (offset error)	VOS		8		LSB
Full scale error (full scale error)	PFSE/NFSE		±15		mV

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Table 6-6 Dynamic characteristics

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Full power bandwidth:		FPBW		3.0		GHz
fs = 1.8 GSPS, Vin = -1 dBFS						
Effective number of bits	fin = 248 MHz	ENOB		8.7		bit
	fin = 498 MHz			8.4		bit
	fin = 998 MHz			8.0		bit
	fin = 1147 MHz			7.9		bit
	fin = 1448 MHz			7.7		bit
Signal to Noise and Distortion Ratio	fin = 248 MHz	SNDR		54.1		dBFS
	fin = 498 MHz			52.6		dBFS
	fin = 998 MHz			49.8		dBFS
	fin = 1147 MHz			49.2		dBFS
	fin = 1448 MHz			48.1		dBFS
Signal to Noise Ratio	fin = 248 MHz	SNR		54.1		dBFS
	fin = 498 MHz			52.8		dBFS
	fin = 998 MHz			49.9		dBFS
	fin = 1147 MHz			49.4		dBFS
	fin = 1448 MHz			48.5		dBFS
Total Harmonic Distortion	fin = 248 MHz	|THD|		70.8		dBFS
	fin = 498 MHz			64.7		dBFS
	fin = 998 MHz			65.8		dBFS
	fin = 1147 MHz			63.8		dBFS
	fin = 1448 MHz			59.1		dBFS
Spurious Free Dynamic Range	fin = 248 MHz	|SFDR|		64.7		dBFS
	fin = 498 MHz			64.8		dBFS
	fin = 998 MHz			60.1		dBFS
	fin = 1147 MHz			60.1		dBFS
	fin = 1448 MHz			59.3		dBFS
Second Harm	fin = 248 MHz	|2nd Harm|		79.3		dBFS
	fin = 498 MHz			83.1		dBFS
	fin = 998 MHz			82.7		dBFS
	fin = 1147 MHz			82.8		dBFS
	fin = 1448 MHz			76.7		dBFS
Third Harm	fin = 248 MHz	|3rd Harm|		83.2		dBFS
	fin = 498 MHz			74.5		dBFS
	fin = 998 MHz			75.4		dBFS
	fin = 1147 MHz			70.6		dBFS
	fin = 1448 MHz			67.5		dBFS

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Table 6-7 Calibration characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Calibration period	t_{CAL}		8×10^5		Sampling clock period
Calibration low time	t_{CAL_L}	1000(1)			Sampling clock period
Calibration high time	t_{CAL_H}	1000(1)			Sampling clock period
Calibration delay time	t_{CalDly}		1600		Sampling clock period

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7 Pin configuration and function description

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	V_A	SDO	TPM	NDM	V_A	GND	V_E	GND_E	DId0p	V_DR	DId3p	GND_DR	DId6p	V_DR	DId9p	GND_DR	DId11p	DId11n	GND_DR	A
B	VCM_LVDS	GND	ECEb	SDI	CalRun	V_A	GND	GND_E	V_E	DId0n	DId2p	DId3n	DId5p	DId6n	DId8p	DId9n	DId10p	DI0p	DI1p	DI1n	B
C	Rtrimp	DC_AC	Rextp	SCSb	SCLK	V_A	NC	V_E	GND_E	DId1p	DId2n	DId4p	DId5n	DId7p	DId8n	DId10n	DI0n	V_DR	DI2p	DI2n	C
D	DNC	Rtrimn	Rextn	GND	GND	CAL	DNC	V_A	V_A	DId1n	V_DR	DId4n	GND_DR	DId7n	V_DR	GND_DR	V_DR	DI3p	DI4p	DI4n	D
E	V_A	Tdiodep	DNC	GND													GND_DR	DI3n	DI5p	DI5n	E
F	V_A	GND_TC	Tdioden	DNC													GND_DR	DI6p	DI6n	GND_DR	F
G	V_TC	GND_TC	V_TC	V_TC													DI7p	DI7n	DI8p	DI8n	G
H	VinIp	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				DI9p	DI9n	DI10p	DI10n	H
J	VinIn	GND_TC	V_TC	TE_VREFT				GND	GND	GND	GND	GND	GND				V_DR	DI11p	DI11n	V_DR	J
K	GND	TE_VREFT	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				ORIp	ORIn	DCLK_Ip	DCLK_In	K
L	GND	TE_VREFB	V_TC	GND_TC				GND	GND	GND	GND	GND	GND				ORQp	ORQn	DCLK_Qp	DCLK_Qn	L
M	VinQn	GND_TC	V_TC	TE_VREFB				GND	GND	GND	GND	GND	GND				GND_DR	DQ11p	DQ11n	GND_DR	M
N	VinQp	V_TC	GND_TC	V_A				GND	GND	GND	GND	GND	GND				DQ9p	DQ9n	DQ10p	DQ10n	N
P	V_TC	GND_TC	V_TC	V_TC													DQ7p	DQ7n	DQ8p	DQ8n	P
R	V_A	GND_TC	V_TC	V_TC													V_DR	DQ6p	DQ6n	V_DR	R
T	V_A	GND_TC	GND_TC	GND													V_DR	DQ3n	DQ5p	DQ5n	T
U	GND_TC	CLKp	PDI	GND	GND	RCOUT_1n	DNC	V_A	V_A	DQd1n	V_DR	DQd4n	GND_DR	DQd7n	V_DR	V_DR	GND_DR	DQ3p	DQ4p	DQ4n	U
V	CLKn	DCLK_RSTp	PDQ	CalDly	DES	RCOUT_2p	RCOUT_2n	V_E	GND_E	DQd1p	DQd2n	DQd4p	DQd5n	DQd7p	DQd8n	DQd10n	DQ0n	GND_DR	DQ2p	DQ2n	V
W	DCLK_RSTn	GND	DNC	DDRPh	RCLKn	V_A	GND	GND_E	V_E	DQd0n	DQd2p	DQd3n	DQd5p	DQd6n	DQd8p	DQd9n	DQd10p	DQ0p	DQ1p	DQ1n	W
Y	GND	V_A	FSR	RCLKp	RCOUT_1p	V_A	GND	V_E	GND_E	DQd0p	V_DR	DQd3p	GND_DR	DQd6p	V_DR	DQd9p	GND_DR	DQd11p	DQd11n	GND_DR	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 7.1 Pin Configuration of CW12D1800 (Top View)

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Table 7-1 Pin function description

Pin number	Symbol	Function
H1, J1 N1, M1	VinIp, VinIn VinQp, VinQn	I/Q channel differential signal input
U2, V1	CLKp, CLKn	Differential sampling clock signal input
V2, W1	DCLK_RSTp, DCLK_RSTn	Differential clock reset. Positive pulse reset DCLKI and DCLKQ output
C2	DC_AC	AC Couple selection port, chip internal default pull-down
B1	VCM_LVDS	LVDS output VCM Select, the chip defaults to pull-up
E2, F3	Tdiodep, Tdioden	Temperature sensor diode positive and negative ports
J4, K2	TE_VREFT	REFT channel test output
L2, M4	TE_VREFB	REFB channel test output
D1, D7, E3, F4, W3, U7	DNC	Floating pin, cannot be connected to any potential
C7	NC	Null pin
C3, D3	Rextp, Rextn	External 3.3kΩ precision resistor port 1
C1, D2	Rtrimp, Rtrimn	External 3.3kΩ precision resistor port 2
Y4, W5	RCLKp, RCLKn	Synchronous reference clock input
Y5, U6 V6, V7	RCOut1p, RCOut1n RCOut2p, RCOut2n	Reference clock output 1 and output 2
V5	DES	Double-edge sampling mode selection, when the input is set to logic high, DES (Double Edge Sample) operating mode is selected, which means sampling the I-channel and Q-channel inputs in a time interleaving manner. When this input is set to logic low, the chip is in Non-DES operating mode, i.e., the I channel and Q channel operate independently. In Extended Control Mode (ECM, Extended Control Mode), this input is ignored, and the DES mode selection is controlled by the DES bit (address: 0h, bit 7) through the control register; the default is Non-DES mode operation. Internal chip silent Recognize pull down.
V4	CalDly	Calibration delay selection, the internal chip is pulled down by default.

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D6	CAL	Calibration initialization. The user can have the chip perform self-calibration by keeping the input high at least tCAL_H after keeping the input low at least tCAL_L. If this input remains high on power-on, automatic power-on calibration will be disabled. This pin is valid in both ECM and Non-ECM. In ECM, this pin is logical or operational with the CAL bit (address: 0h, bit 15) in the control register. Therefore, both pins and bits must be set to low and then either one mustbesettohigh toperform Command calibration. The chip internal drop-down is pulled down by default.
B5	CalRun	Calibrationflag output, this output is logically high power when performing the calibration process. flat. Otherwise this output is logic low.
U3 V3	PDI PDQ	I/Q channel shutdown control. Setting any input to logic high will turn off Close the corresponding I or Q channel. Set either input to logic low Will cause the corresponding I or Q channels to enter the working state after a certain time delay state. This pin is valid in both ECM and Non- ECM. In ECM In this case, each pin performs logic or operation with its respective bits. Therefore, no Whether this pin or the PDI and PDQ bits in the control register are available Used to close I and Q channels respectively (address: 0h, bit 11 and bit 10). The chip internal drop-down is pulled down by default.
A4	TPM	Test mode selection, when the input is logic high, the chip continuouslyoutputs a set of repeated fixed digital sequences. In ECM, this input is ignored, and the test mode can only control the register TPM bits (address: 0h, bit 12) control. The chip internal drop-down is pulled down by default.

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A5	NDM	Non-Demux mode selection, setting this input to logic high will set the digital output bus to 1:1 Non-Demuxed mode. Setting this input to logic low will set the digital output bus to 1:2 Demuxed mode. This function is only controlled by pins and in ECM and
		Stay active during Non-ECM. The chip internal drop-down is pulled down by default.
Y3	FSR	Full scale input range selection. In Non-ECM, this input must be set to logic high; the full-scale differential input range for the I and Q channel inputs is set by this pin. In ECM, this input is ignored, and the full scale range of I and Q channel inputs is set by Addr:3h and Addr:Bh, respectively. Set to determine independently. The chip is pulled up by default.
W4	DDRPh	DDR phase selection. This input selects the 0°Data- to-DCLK phase relationship when the logic is low. When logic is high, it selects the 90°Data-to- DCLK phase relationship, i.e. the DCLK conversion indicates the middle of the valid data output. This pin is only valid when the chip is in 1:2 Demux mode, i.e. the NDM pin is set to logic low. In ECM, this input is ignored and the DDR phase is passed by the DPS bit (address: 0h, bit 14) Control register selection; default is 0° mode. The chip internal drop-down is pulled down by default.
B3	ECEb	Extended control enable. When this signal is valid (logic low), the extended function control is performed through the SPI interface. In this case, most direct control pins do not work. When the signal is invalid (logic high), the SPI interface is disabled and all SPI registers are reset to their default values.All available settings are controlled via the control pin. The chip is pulled up by default.

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C4	SCSb	SPI chip selection, the internal chip is pulled up by default.
C5	SCLK	SPI serial clock, the chip internal drive is pulled down by default.
B4	SDI	SPI serial data input, the chip internal drop-down is pulled down by default.
A3	SDO	SPI serial data output
A2, A6, B6, C6, D8, D9, E1, F1, H4, N4, R1, T1, U8, U9, W6, Y2, Y6	V_A	Analog circuit power supply
G1, G3, G4, H2 J3, K3, L3, M3 N2, P1, P3, P4 R3, R4	V_TC	Sampling and hold and clock circuit power supply
A11, A15, C18 D11, D15, D17 J17, J20, R17 R20, T17, U11 U15, U16, Y11 Y15	V_DR	Output Driver power

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Table 7-1 Pin Function Description (continued)

Terminal number	symbol	Function
A8, B9, C8, V8 W9, Y8	V_E	Digital encoding circuit power supply
A1, A7, B2, B7 D4, D5, E4, K1 L1, T4, U4, U5 W2, W7, Y1, Y7 H8:N13	GND	Analog circuit ground
F2, G2, H3, J2 K4, L4, M2, N3 P2, R2, T2, T3 U1	GND_TC	Sample and Hold and Clock Circuitry Ground
A13, A17, A20 D13, D16, E17 F17, F20, M17 M20, U13, U17 V18, Y13, Y17 Y20	GND_DR	Output Driver Ground
A9, B8, C9, V9 W8, Y9	GND_E	Digital encoding circuit ground
K19, K20 L19, L20	DCLKIp, DCLKIn DCLKQp, DCLKQn	I/Q channel data clock LVDS output
K17, K18 L17, L18	ORIp,ORIn ORQp,ORQn	I/Q channel overrange LVDS output
J18, J19 H19, H20 H17, H18 G19, G20 G17, G18 F18, F19 E19, E20 D19, D20 D18, E18 C19, C20 B19, B20 B18, C17	DQ11p，DQ11n DQ10p，DQ10n DQ9p，DQ9n DQ8p，DQ8n DQ7p，DQ7n DQ6p，DQ6n DQ5p，DQ5n DQ4p，DQ4n DQ3p，DQ3n DQ2p，DQ2n DQ1p，DQ1n DQ0p，DQ0n	I/Q channel data LVDS output

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Table 7-1 Pin Function Description (Continued)

Pin Number	Symbol	Function
M18, M19	DQ11p, DQ11n	I/Q channel data LVDS output
N19, N20	DQ10p, DQ10n	
N17, N18	DQ9p, DQ9n	
P19, P20	DQ8p, DQ8n	
P17, P18	DQ7p, DQ7n	
R18, R19	DQ6p, DQ6n	
T19, T20	DQ5p, DQ5n	
U19, U20	DQ4p, DQ4n	
U18, T18	DQ3p, DQ3n	
V19, V20	DQ2p, DQ2n	
W19, W20	DQ1p, DQ1n	
W18, V17	DQ0p, DQ0n	
Pin Number	**Symbol**	**Function**
A18, A19	DId11p, DId11n	I/Q Channel data delay LVDS output
B17, C16	DId10p,DId10n	
A16, B16	DId9p, DId9n	
B15, C15	DId8p,DId8n	
C14, D14	DId7p, DId7n	
A14, B14	DId6p,DId6n	
B13, C13	DId5p, DId5n	
C12, D12	DId4p,DId4n	
A12, B12	DId3p, DId3n	
B11, C11	DId2p,DId2n	
C10, D10	DId1p, DId1n	
A10, B10	DId0p, DId0n	
Y18, Y19	DQd11p, DQd11n	
W17, V16	DQd10p,DQd10n	
Y16, W16	DQd9p, DQd9n	
W15, V15	DQd8p, DQd8n	
V14, U14	DQd7p,DQd7n	
Y14, W14	DQd6p, DQd6n	
W13, V13	DQd5p, DQd5n	
V12, U12	DQd4p,DQd4n	
Y12, W12	DQd3p, DQd3n	
W11, V11	DQd2p, DQd2n	
V10, U10	DQd1p,DQd1n	
Y10, W10	DQd0p, DQd0n	

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8 Typical performance test curve

Chip works at Demux and Non-DES mode, and VA = VDR = VTC = VE = +1.9V, AC-coupled signal input, unused channels terminated to “AC ground”, AC-coupled sine wave sampling clock, fCLK = 1.8 GHz; Rext = Rtrim = 3300 Ω ± 0.1%; input signal source impedance 50 Ω; TA = 25°C.

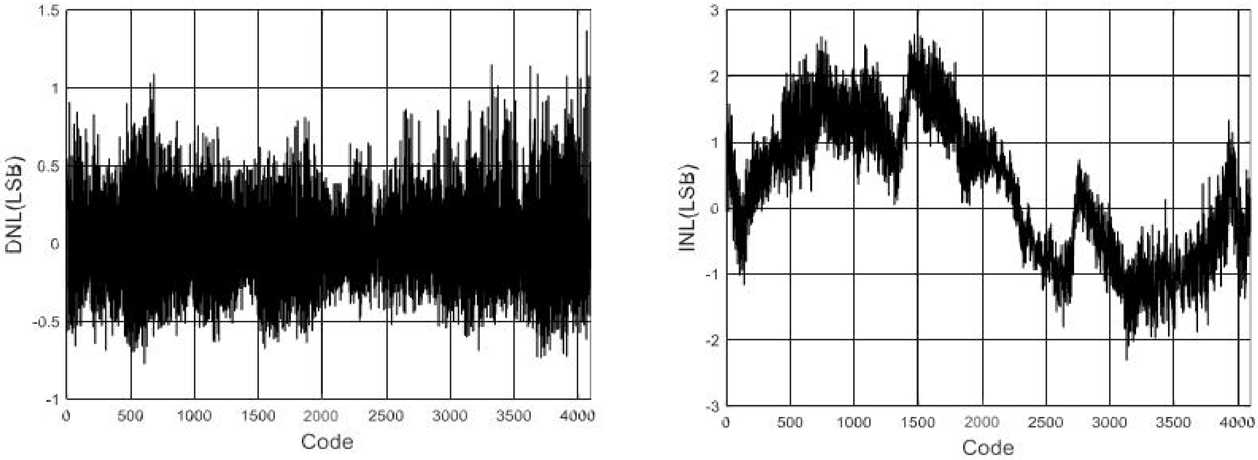
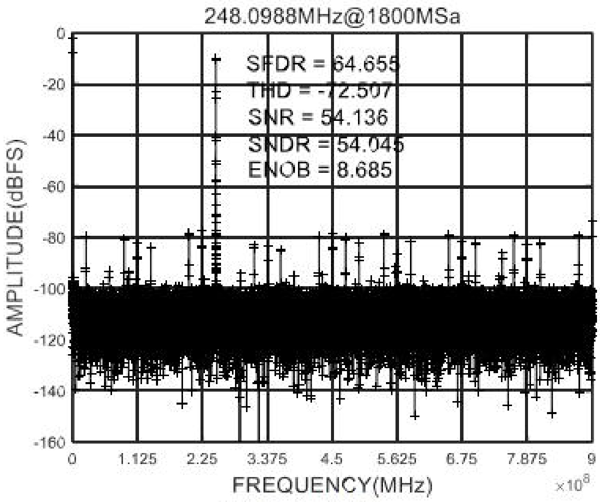
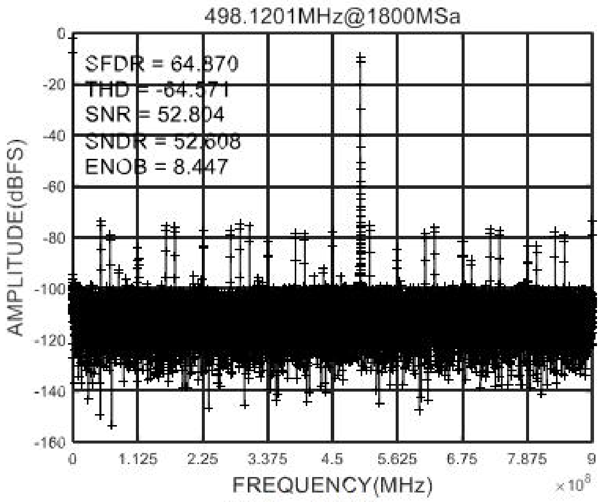


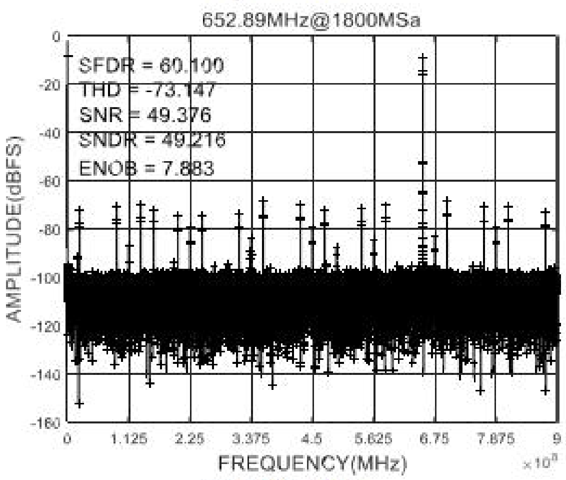
Figure 8.1 CW12D1800 Linear Error



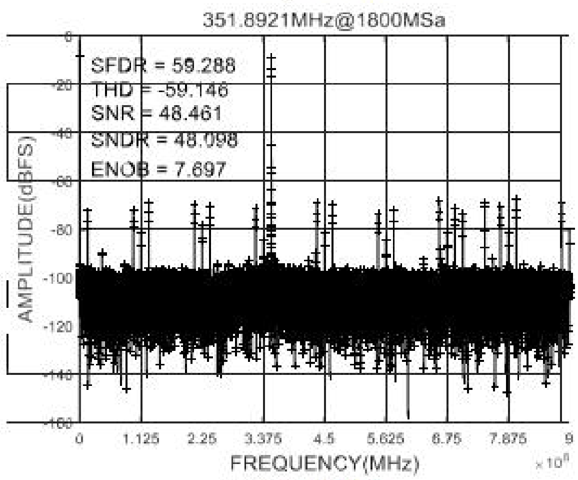
（a） f_{in} = 248MHz



（b） f_{in} = 498MHz



（c） f_{in} = 1147MHz



（d） f_{in} = 1448MHz

Figure 8.2 Dynamic Characteristics of CW12D1800D (FS=1.8GHz)

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9 Timing diagram

1. Data timing

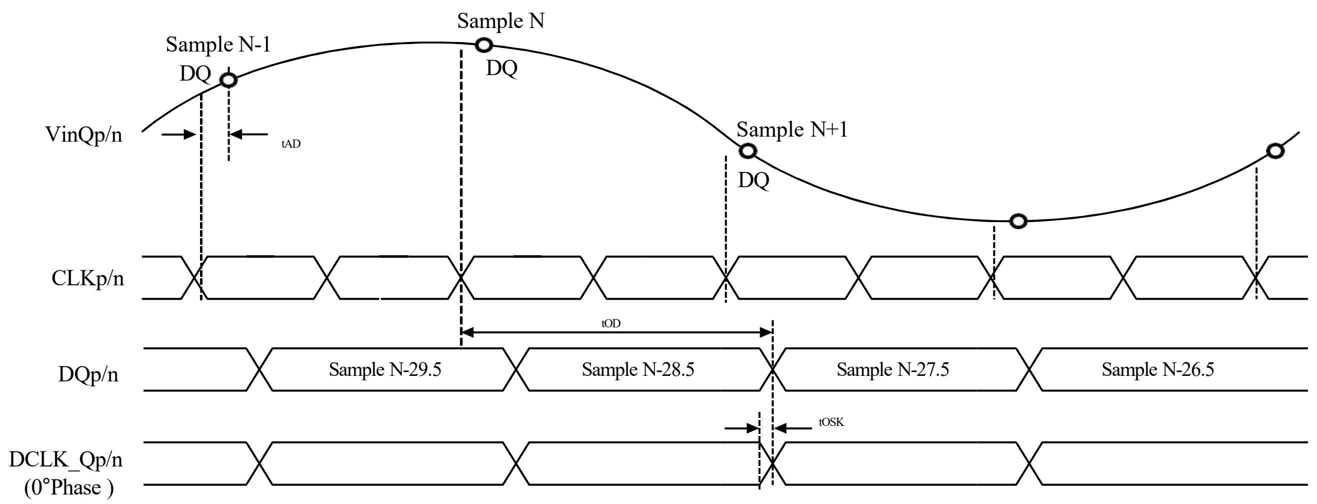

Figure 9.1 CW12D1800 data timing in Non-Demux Non-DES mode

Description:

The I channel data timing is exactly the same as the Q channel.

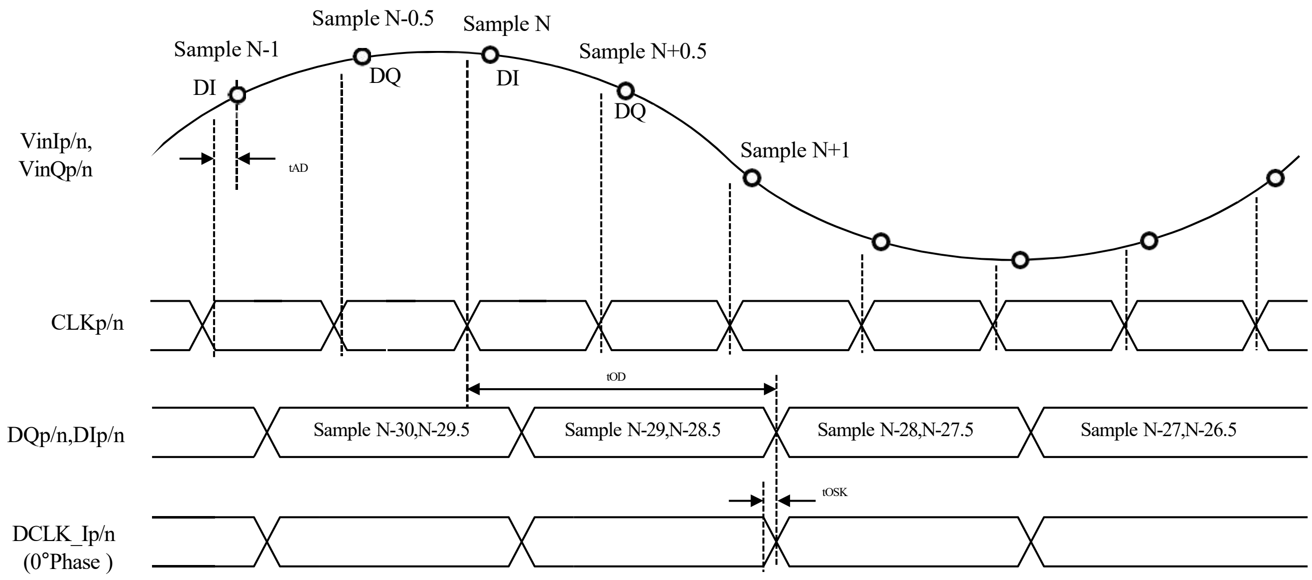

Figure 9.2 CW12D1800 data timing in Non-Demux DES mode

Description:

In this mode, VinIp/n and VinQp/n must be "short-circuited" at the ADC input; I channel input is sampled at the rising edge of CLK, and Q channel input is sampled at the falling edge of CLK; I Channel output delay 27.5 Cycles, Q channel output delay 28 Cycles;

Data is output on both edges of DCLK, the time sequence is DQ, DI (FDCLK = 1/2 FS)

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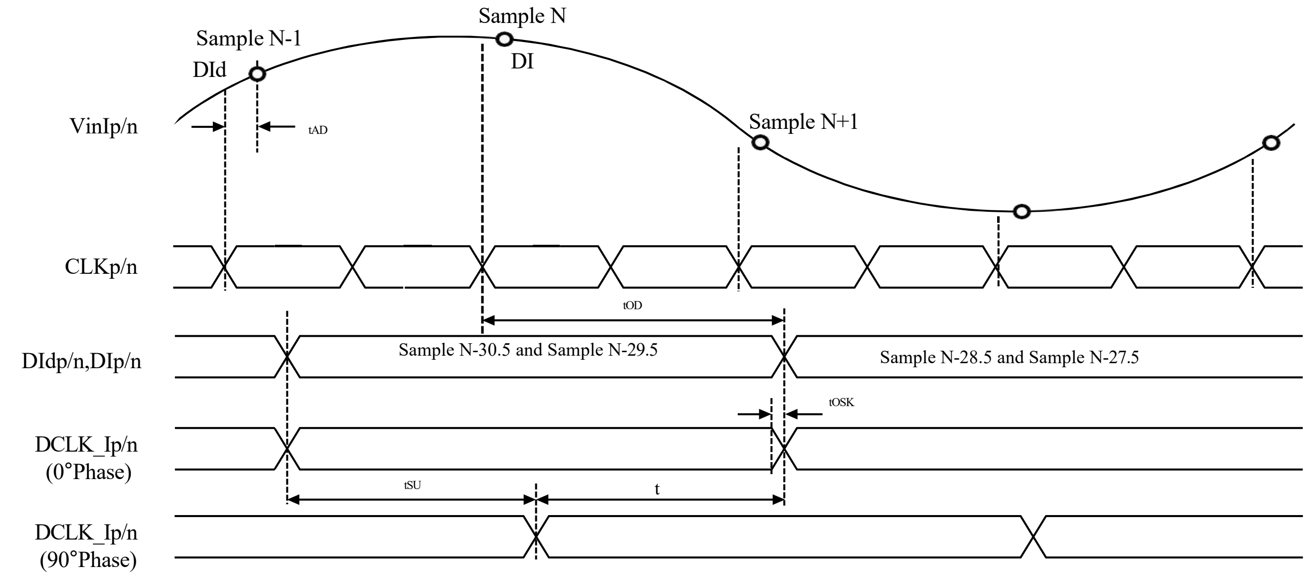

Figure 9.3 CW12D1800 data timing in 1:2 Demux Non-DES mode

Description:

I channel input is sampled on the rising edge of CLK; I channel output is delayed by 27.5 cycles;

Data is output on both edges of DCLK, the time sequence is DId, DI (FDCLK = 1/4 FS)

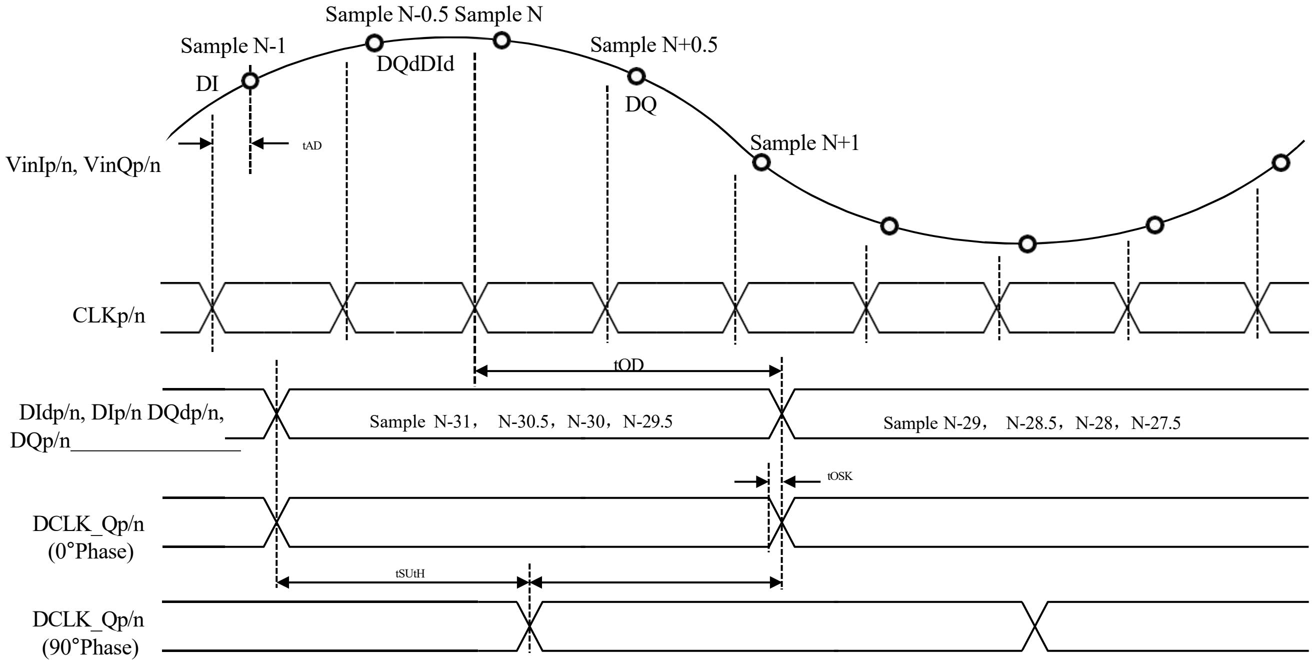

Figure 9.4 CW12D1800 Data Timing in 1:4 Demux DES Mode

Description:

In this mode, VinIp/n and VinQp/n must be "shorted" at the ADCinput; I channel input is sampled at the rising edge of CLK, and Q channel input is sampled at the falling edge of CLK; I channel output delay is 27.5 cycles, Q channel output delay is28 cycles;

Data is output at both edges of DCLK, the time sequence is DQ, DI (FDCLK = 1/4 FS)

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9.2 Calibration Timing

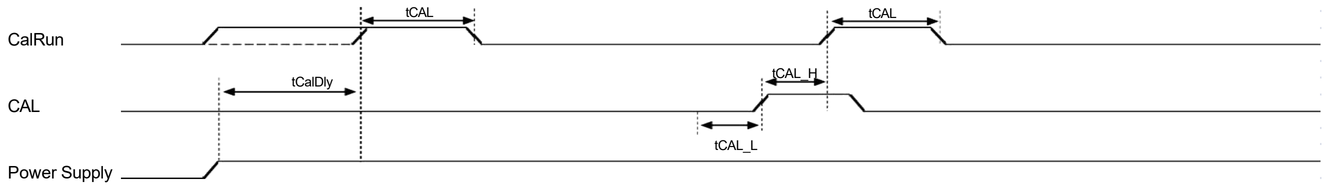

Figure 9.5 Power-on Calibration and On-Command Calibration Timing

9.3 SPI Interface Timing

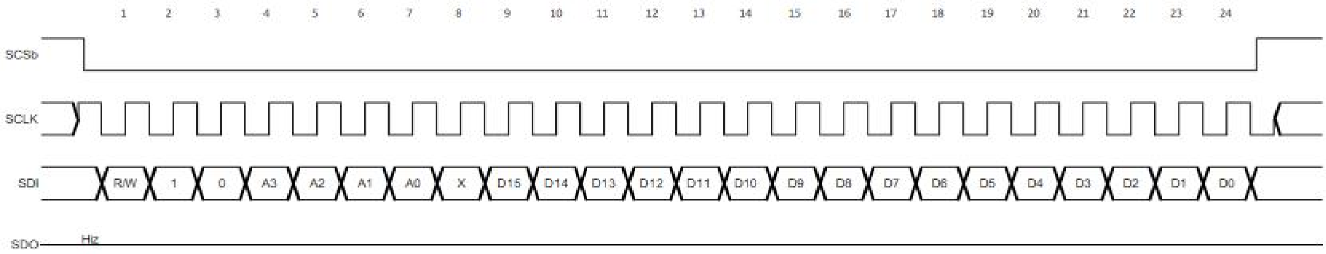

Figure 9.6 SPI write timing

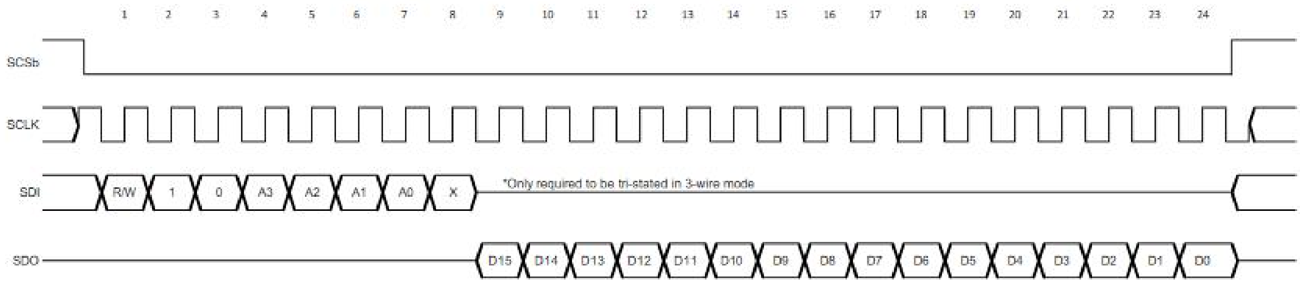

Figure 9.7 SPI read timing

Table 9.1 SPI interface command and data field definition

Bit	Definition	Description
1	Read/write control bit	1b: read operation 0b: write operation
2~3	Reserved	Default setting is 10b
4~7	Address bit A[3:0]	Register address, address order is MSB first
8	X	Reserved
9~24	Data bit D[15:0]	Data is written to or read from the register

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10 Package information

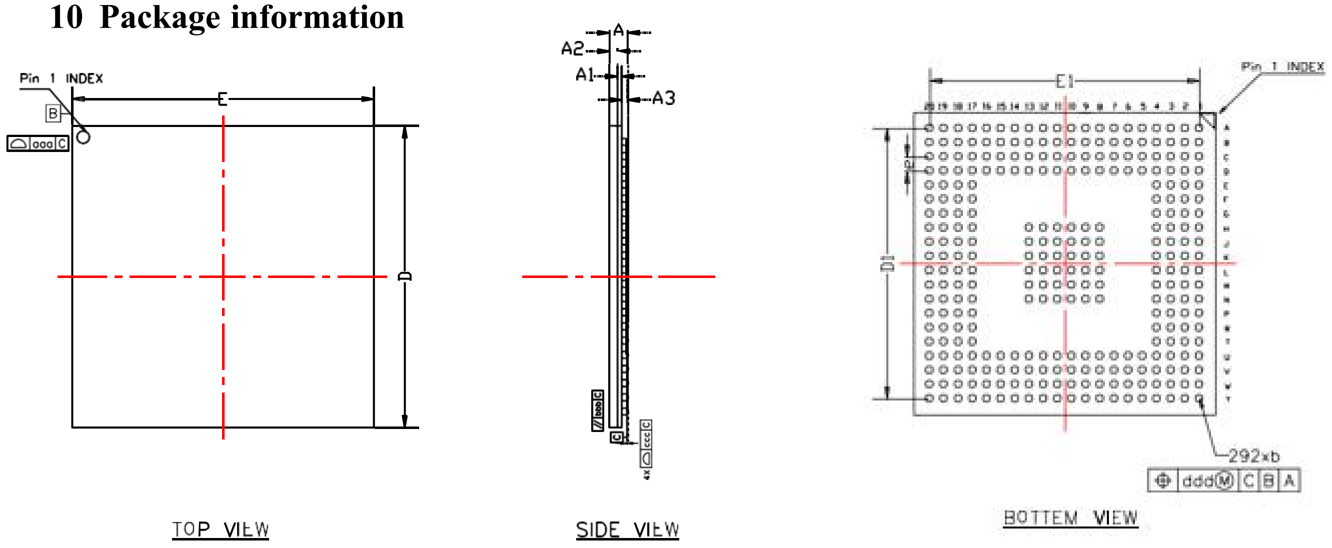

Figure 10.1 CW12D1800 package outline

Table 10.1 CW12D1800 package outline dimensions

Dimension symbol	Unit: mm		
	Minimum	Typical	Maximum
A	1.56	1.66	1.76
A1	0.32	0.36	0.40
A2	-	0.7	-
A3	0.55	0.6	0.65
D	-	27.0	-
E	-	27.0	-
D1	-	24.13	-
E1	-	24.13	-
e	-	1.27	-
b	0.71	0.76	0.81

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11 Multi-chip synchronization function

CW12D1800 has two functions for synchronizing multiple ADC chips (AutoSync and DCLK Reset). The AutoSync function has two working modes: master-slave and full-slave. It is recommended to use the full-slave mode, use all CW12D1800 as Slave ADC, and use the clock board to provide the synchronous clock RCLK (CLK/16) to drive the RCLKp/RCLKn of each CW12D1800 through the equal length line to achieve synchronization of multiple CW12D1800. The DCLK Reset function is consistent with AutoSync, but has stricter requirements on the timing of use, so it is not recommended to use this function for multi-chip synchronization. The default configuration of CW12D1800 does not enable this function.

When using the AutoSync function for multi-chip synchronization, it is recommended to use the full-slave mode, use all CW12D1800 as Slave ADC, and use the clock board to provide the synchronous clock RCLK (CLK/16) to drive the RCLKp/RCLKn of each CW12D1800 through the equal length line to achieve synchronization of multiple CW12D1800. In order to synchronize the DCLK (including data) of multiple ADCs, all DCLKs must be in phase. Since the DCLK of CW12D1800 is generated by the RCLK inside the chip and retimed by the master clock CLK, the CLK signals of the synchronized ADCs must be in phase, that is, the master clock CLK arrives at the CW12D1800 at the same time. The enabling of the AutoSync function must be configured through the control register.

The figure below shows an example of synchronization of two Slave ADCs, where DCLKI and DCLKQ are not distinguished and are both represented by DCLK.

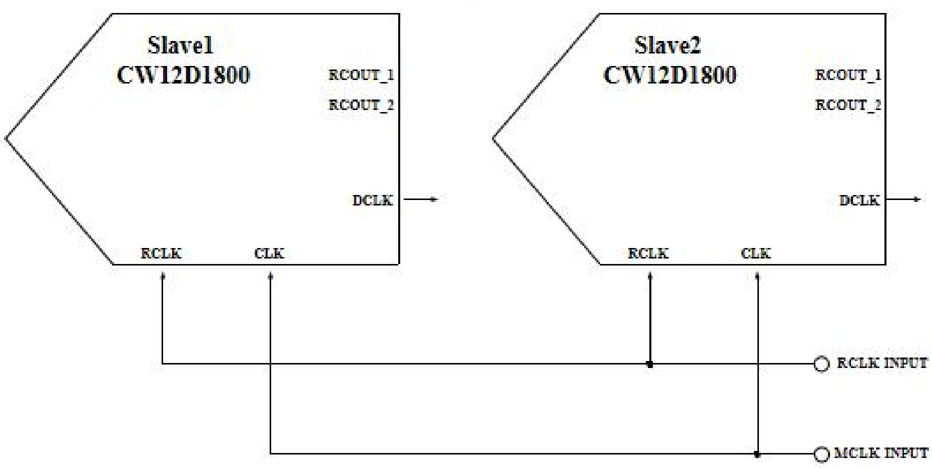

Figure 11.1 CW12D1800 AutoSync function connection

example If the AutoSync and DCLK Reset functions are not used, it

is recommended to connect unused PINs according to the table below.

Table 11.1 Recommendations for port connections when the AutoSync and DCLK Reset functions are not used

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port	Connection suggestions
RCLKp/RCLKn	Floating
RCOUT1p/RCOUT1n	Floating
RCOUT2p/RCOUT2n	Floating
DCLK_RST+	Connect to GND via a 1kΩ resistor
DCLK_RST-	Connect to VA via 1kΩ resistor

12 Register list

Configuration Register 1

Addr: 0h (0000b)																POR state: 2000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAL	DPS	OVS	TPM	PDI	PDQ	Res	Res	DES	Res	Res	SC	Res			
POR	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	CAL, calibration enable bit Setting CAL=1 will trigger a correction process. Since this control bit will not be automatically cleared, when the user triggers correction, CAL=0 must be set in advance Both this control bit and the CAL pin can trigger the correction process, which is functionally a "or" relationship, and has no polarity requirement between each other.
Bit 14	DPS, DDR phase difference selection bit When DPS=0, the DDR Data-to-DCLK phase relationship is 0˚ When DPS=1, the DDR Data-to-DCLK phase relationship is 90˚ In Non-Demux mode, this bit setting is invalid and is always in DDR 0° mode.
Bit 13	OVS, output voltage selection bit When OVS=0, the output voltage is 0.8V. When OVS=1, the output voltage is 1.2V. This control bit is the LVDS output pin (DATA, OR and DCLK), and different voltages are selected
Bit 12	TPM, test mode enable bit When TPM=0, normal working mode When TPM=1, the device's LVDS output pin (Digital DATA, OR) will continuously output a fixed digital pattern
Bit 11	PDI, I channel power-off enable bit When PDI=0, the I channel is in normal working mode When PDI=1, the I channel is in shutdown working mode This control bit and the PDI pin are functionally "OR" related. As long as any signal is valid (high level), the I channel will be in power-off mode
Bit 10	PDQ, Q channel power-off enable bit When PDQ=0, the Q channel is in normal working mode When PDQ=1, the Q channel is in shutdown working mode This control bit and the PDQ pin are functionally "OR" related. As long as any signal is valid (high level), the Q channel will be in power-off mode

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Addr: 0h (0000b)									POR state: 2000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAL	DPS	OVS	TPM	PDI	PDQ	Res	Res	DES	Res	Res	SC	Res			
POR	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 9	Reserved															
Bit 8	Reserved															
Bit 7	DES, dual-edge sampling enable bit When DES=0, the device works in single-edge sampling mode (Non-DES Mode） When DES=1, the device works in dual-edge sampling mode (DESIQ Mode), and the I/Q channels need to be shorted															
Bit 6	DEQ, reserved word, Reserved															
Bit 5	DIQ, reserved word, Reserved															
Bit 4	SC, binary complement enable bit When SC=0, the LVDS data output format is offset binary format (Offset Binary format) When SC=1, the LVDS data output format is binary complement format (Two's Complement format)															
Bit 3:0	Reserved															

Reserved word

Addr: 1h (0001b)									POR state: 7335h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	1	1	1	0	0	1	1	0	0	1	1	0	1	0	1
Bit 15:0	Reserved															

I channel offset configuration word

Addr: 2h (0010b)									POR state: 0000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM<11:0>											
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:13	Reserved															
Bit 12	OS, offset direction When OS=0, Bits 11:0 represent the ADC output positive offset When OS=1, Bits 11:0 represent the negative offset of ADC output															
Bit 11:0	OM, offset size 1/4 LSB															

I channel full amplitude calibration configuration word

Addr: 3h (0011b)									POR state: 0280h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res						FM<9:0>									
POR	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
Bit 15:10	Reserved															
Bit 9:0	FM, full scale amplitude setting, positive and negative adjustable 16mV, step length is about 63uV 0180 600mV 0280 800mV 0380 1000mV															

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Calibration Configuration Word

Addr: 4h (0100b)																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res								SSC	Res						
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:8	Reserved															
Bit 7	SSC, SPI write enable bit When SSC=0, the user is prohibited from changing the calibration value (stored in 05h and 06h) When SSC=1, the user is allowed to change the calibration value (stored in 05h and 06h)															
Bit 6:0	Reserved															

I channel calibration value

Addr: 5h (0101b)																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:0	Reserved															

Q channel calibration value

Addr: 6h (0110b)																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 3:0	Reserved															

DES timing adjustment word

Addr: 7h (0111b)																POR state: 8000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DES1<9:0>										Res					DSL
POR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:6	DES phase setting, range 25ps, step length ~25fs															
Bit 5:1	Reserved															
Bit 0	DSL, Q channel DES phase selection 0: Select the value written to DES1 (default I/Q channel writes the value of DES1) 1: Select the value written to DES2															

Reserved word

Addr: 8h (1000b)																POR state: 7335h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	1	1	1	0	0	1	1	0	0	1	1	0	1	0	1
Bit 15:0	Reserved															

Addr: 9h (1001b)																POR state: 7335h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	1	1	1	0	0	1	1	0	0	1	1	0	1	0	1
Bit 15:0	Reserved															

Q channel offset configuration word

Addr: Ah (1010b)																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			OS	OM<11:0>											
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:13	Reserved															
Bit 12	OS, offset direction When OS=0, Bits 11:0 represent the ADC output positive offset. When OS=1, Bits 11:0 represent the ADC output negative offset.															
Bit 11:0	OM, offset size 1/4 LSB															

Q channel full amplitude calibration configuration word

Addr: Bh (1011b)																POR state: 0280h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res						FM<9:0>									
POR	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
Bit 15:10	Reserved															
Bit 9:0	FM, full scale amplitude setting, positive and negative adjustable 16mV, step length is about 63uV 0180 600mV 0280 800mV 0380 1000mV															

Aperture delay coarse adjustment control word (reserved word)

Addr: Ch (1100b)																POR state: 0400h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAS1<5:0>						Res									CTS
POR	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit 15:10	tAD coarse adjustment configuration, range 115ps, step length 23ps															
Bit 9:1	Reserved															
Bit 0	CTS, Q channel tAD coarse adjustment configuration selection 0: Select the configuration written to CAS1 (I channel always uses CAS1) 1: Select the configuration written to CAS2															

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Aperture delay fine adjustment control word

Addr: Dh (1101b)									POR state: 8000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FAS1<9:0>										Res					FTS
POR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit 15:6	tAD fine adjustment configuration, range 25ps, step length is about 25fs															
Bit 5:1	Reserved															
Bit 0	FTS, Q channel tAD fine adjustment configuration selection 0: Select the configuration written to FAS1 (I channel always uses FAS1) 1: Select the configuration written to FAS2															

AutoSync control word

Addr: Eh (1110b)									POR state: 0003h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res		DRC<5:0>						Res	SP<3:0>				ES	DOC	DR
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Bit 15:14	Reserved															
Bit 13:8	DRC<5:0>, reference clock RCLK internal delay control word, 64 configurations in total, 20ps as a step															
Bit 7	Reserved															
Bit 6:3	SP<3:0>, phase selection Used to select the phase difference of the reference clock RCLK, step size 22.5°															
Bit 2	ES, slave enable bit When ES=0, the device works in the host mode When ES=1, the device works in the slave mode															
Bit 1	DOC, disable the output of reference clock RCLK When DOC=0, enable the output of reference clock RCLK of RCOut1/2 ports. When DOC=1, disable the output of reference clock RCLK of RCOut1/2 ports.															
Bit 0	DR, disable DCLK_RST function When DR=0, enable DCLK_RST function. When DR=1, disable DCLK_RST function.															

Reserved word

Addr: Fh (1111b)									POR state: 7335h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															
POR	0	1	1	1	0	0	1	1	0	0	1	1	0	1	0	1
Bit 15:0	Reserved															

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