CW9694 Data Sheet

Quad-Channel 14-Bit, 500MSPS High-Speed ADC

1.0 Overview

The CW9694 is a quad-channel, 14-bit, 500MSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample/hold circuit designed for low power, small size, and ease of use. The CW9694 has a −3dB input bandwidth of 1.4GHz and has the advantages of high sampling rate, good linearity, small package, and low power consumption. The ADC core of CW9694 adopts a multi-stage differential pipeline structure, integrating output error correction logic. Each ADC has wide bandwidth inputs that support a variety of user-selectable input ranges. The analog input and clock signal are differential inputs. The ADC data output is connected to four digital downconverters (DDCs) via an internal multiplexer. Each DDC consists of multiple cascaded signal processing stages, including: a 48-bit frequency converter (Digital Controlled Oscillator (NCO)) and up to four half-band decimation filters.

The switching between DDC modes of the CW9694 can be controlled via SPI programmably.

2.0 application

- Multi-mode digital transceiver
- Software Radio
- 3G/4G digital communication
- Phased array system
- Automatic testing equipment
- High-speed testing instrument

3.0 Features

- Programmable over-range rapid detection
- JESD204B encoded serial output, speed up to 13.1Gbps
- Analog input bandwidth 1.4GHz (-3dB)
- Low power consumption, no heat sink required
- 4 integrated data processing channels (DDC)
- Multi-chip automatic synchronization
- Plastic seal QFN72 (10mm × 10mm)

4.0 Performance metrics

- Full power bandwidth: 1.4GHz
- Dynamic performance (fs=500MSPS)
  - fin=5.1MHz
    ENOB=10.4Bit, SFDR=82.2dBc, SNR=65.8dBFS
  - fin=70.1MHz ENOB=10.4Bit, SFDR=81.3dBc, SNR=65.7dBFS
  - fin=305MHz
    ENOB=10.2Bit, SFDR=80.9dBc, SNR=65.3dBFS
  - fin=765MHz
    ENOB=10.1Bit, SFDR=77dBc, SNR=64dBFS
  - fin=985MHz
    ENOB=9.9Bit, SFDR=75.5dBc, SNR=63.4dBFS

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5.0 Simplified block diagram

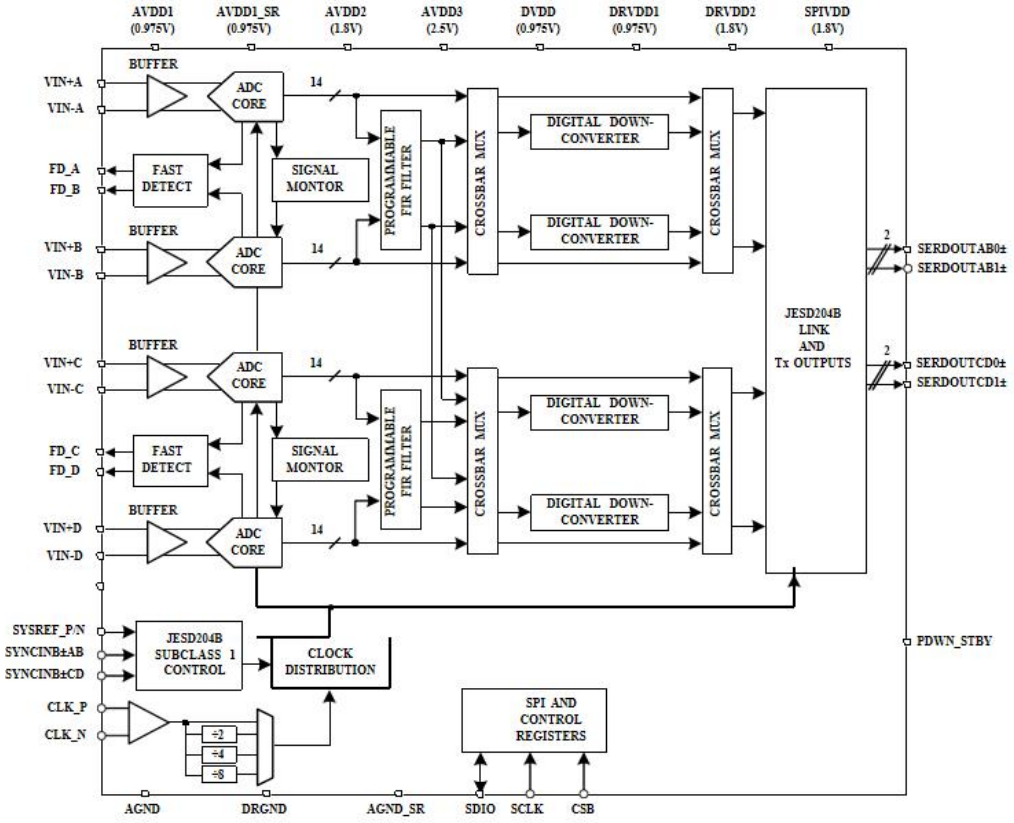

Figure 1 CW9694 principle block diagram

6.0 Product Overview

CW9694 is a four-channel, 14-bit, 500MSPS analog-to-digital converter (ADC). The device features an on-chip buffer and sample-holding circuit, designed for low power consumption, small size and ease of use. The product is designed to support communication applications that can directly sample broadband analog signals up to 1.4GHz. ADC input-3dB bandwidth 2GHz. The CW9694 has wide input bandwidth, high sampling rate, excellent linearity and low power consumption in small packages.

The four-channel ADC core adopts a multi-stage differential pipeline architecture and integrates output error correction logic. Each ADC has wide bandwidth inputs, supporting a variety of user-selectable input range. The analog input and the clock signal are differential inputs. The ADC data output is connected internally to four digital downconverters via a cross multiplexer (DDC). Each DDC consists of multiple signal processing stages: a 48-bit frequency converter (NCO)) and a half-band decimation filter. NCO can select up to 16 preset bands via the General-purpose Input/Output (GPIO) pin. Or use the phase continuous fast frequency hopping mechanism for band selection. The operation of the CW9694 between DDC modes is selectable via the SPI programmable configuration file.

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In addition to the DDC module, the CW9694 has several functions that simplify the design of AGC functions in communication receivers. Programmable threshold detectors are allowed The fast detection control bit in the ADC register monitors the input signal power. If the input signal level exceeds a programmable threshold, the fast detection indicator signal becomes high. Since this threshold indicates low latency, the user can quickly lower the system gain to avoid overrange situations of ADC input. In addition to fast detection output, CW9694 Signal monitoring function is also provided. The signal monitoring module provides additional information about the signals digitized by the ADC.Users can configure JESD204B based on the DDC configuration and receive the channel rate acceptable to the logic device using single, dual or quad-channel configurations Subclass1 High-speed serial output. Multi-chip synchronization is supported through SYSREF± and SYNCINB±AB, SYNCINB±CD input pins.The CW9694 features flexible power-down selection, which can significantly save power when needed. All of these features can be used with 3-wire serial interface (SPI) or PDWN/STBY pin is controlled. The CW9694 is available in a 72-pin lead-free QFN package with a rated operating temperature range of -55°C to +125°C.

Product Highlights

1. Low power consumption per channel.
2. JESD204B channel rates support up to 13.1Gbps.
3. Full power bandwidth supports mid-frequency (IF) sampling signals up to 2GHz.
4. Buffered input simplifies the design and implementation of filters.
5. Four integrated broadband decimation filters and NCO modules support multi-band receivers.
6. Programmable over-range rapid detection.

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7.0 Typical performance

Table 1 Chip use conditions

Parameter	Symbol	Note	Value	Unit
Power supply voltage	AVDD1	Analog power supply voltage 1	0.975	V
	AVDD2	Analog power supply voltage 2	1.8	V
	AVDD3	Analog power supply voltage 3	2.5	V
	AVDD1_SR	SYSREF analog power supply voltage	0.975	V
	DVDD	Digital power supply voltage	0.975	V
	DRVDD1	SERDES power supply voltage 1	0.975	V
	DRVDD2	SERDES power supply voltage 2	1.8	V
	SPIVDD	SPI power supply voltage	1.8	V
Power-on sequence		No power-on sequence requirement		
Ground	AGND	Analog circuit ground	0	V
	AGND_SR	SYSREF analog power supply ground	0	V
	DGND	Digital circuit ground	0	V
	DRGND	SERDES digital ground	0	V
Differential input analog signal amplitude		Input signal differential amplitude	1.8	Vpp
Logic input high level	V_{IH}		$0.8V_{in}$	V
Logic input low level	V_{IL}		GND	
Clock differential input signal amplitude	$V_{CLKP} - V_{CLKN}$		800	mVpp
Operating temperature range	T_A		$-55 \le T_A \le 125$	℃

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Table 2 Power supply, input electrical characteristics

Unless otherwise specified, AVDD1 = 0.975V, AVDD1_SR = 0.975V, AVDD2 = 1.8V, AVDD3 = 2.5V, DVDD = 0.975V, DRVDD1 = 0.975V, DVDD2 = 1.8V, SPIVDD = 1.8V, fs = 500MSPS, full-scale 1.8Vp-p input range, -55℃≤TA≤+125℃.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage:					
Analog power supply voltage 1	AVDD1	0.95	0.975	1.0	V
SYSREF analog power supply voltage	AVDD1_SR	0.95	0.975	1.0	V
Analog power supply voltage 2	AVDD2	1.71	1.8	1.89	V
Analog power supply voltage 3	AVDD3	2.44	2.5	2.56	V
SYSREF analog power supply voltage	AVDD1_SR	0.95	0.975	1.0	V
Digital power supply voltage	DVDD	0.95	0.975	1.0	V
SERDES power supply voltage 1	DRDVDD1	0.95	0.975	1.0	V
SERDES power supply voltage 2	DRDVDD2	1.71	1.8	1.89	V
SPI power supply voltage	SPIVDD	1.71	1.8	1.89	V
Power supply current:					
Analog power supply current 1	I_{AVDD1}		360	480	mA
Analog power supply current 2	I_{AVDD2}		330	380	mA
Analog power supply current 3	I_{AVDD3}		126	150	mA
Digital power supply current	I_{DVDD+} I_{DRVDD1}		226	360	mA
SPI power supply current	I_{SPIVDD}+ I_{DRVDD1}		9	15	mA
Resolution:			14		Bits
Power consumption: (full scale)				1.9	
Normal operation			1.6		W
Power-Down mode			500		mW
Analog input:					
Differential input signal amplitude		1.44	1.8	2.16	Vpp
Common mode voltage			1.55		V
Differential input capacitance			1.75		pF
Full Power Bandwidth			1.4		GHz

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Clock Input					
Logic Compatibility	LVDS/LVPECL				
Clock Source Type		Differential Sine Wave			
Differential Input Voltage Swing	$V_{CLKP} - V_{CLKN}$	600	800	1600	mVpp
Clock frequency	CLK	0.24		2.4	GHz
Common-mode voltage			0.69		V
Resistance of clock differential input	R_{MCLK}		100		Ω
System reference input (SYSREF±)					
Logic compatibility	LVDS/LVPECL				
Differential input voltage swing		400	800	1800	mVpp
Common-mode voltage		0.6	0.675	2	V
Input resistance			22		kΩ
Logic inputs (SDIO, SCLK, CSB, PDWN/STBY, FD_A/GPIO_A0, FD_B/GPIO_A1, FD_C/GPIO_B0, FD_D/GPIO_B1,)					
Logic compatibility	CMOS				
Logic low		0		0.35 × SPIVDD	V
Logic high		0.65 × SPIVDD			V
Input resistance			10		MΩ
Logic outputs (SDIO, FD_A, FD_B)					
Logic compatibility	CMOS				
Logic low Logic high		0 SPIVDD − 0.45V		0.45	V V
Synchronous Input (SYNCINB±AB/SYNCINB±CD)					
Logic Compatibility	LVDS/LVPECL/CMOS				
Differential Input Voltage Swing Common Mode Voltage Input Resistance		400 0.6	800 0.675 22	1800 2.2	mVpp V kΩ
Digital Output (SERDOUTABx±/SERDOUTCDx±)					
Logic Compatibility	CML				
Differential Output Voltage Swing Differential Termination Impedance Matching		80	455 100	120	mVpp Ω

Table 3 AC Characteristics

Unless otherwise noted, AVDD1 = 0.975V, AVDD1_SR = 0.975V, AVDD2 = 1.8V, AVDD3 = 2.5V, DVDD = 0.975V, DRVDD1 =0.975V, DVDD2 = 1.8V, SPIVDD = 1.8V, fs = 500MSPS, clock divide ratio = 2, full-scale 1.8Vp-p input range, -55℃≤TA≤+125℃.

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Parameter	Symbol	Minimum value	Typical value	Maximum value	Unit
CLOCK					
Clock frequency Sampling rate		0.24 2402		2.4 6001	GHz MSPS
Output parameters					
PLL lock time Data rate per channel		 1.6875	5 10	 13.1	ms Gbps
Delay parameters					
Pipeline delay Fast detection delay Aperture delay (tA)			54 160	 30 	cycles cycles ps
Wake-up time					
From STBY From Power-Down			3 10		ms ms

1. The maximum sampling rate is the clock frequency after the divider.
2. The minimum sampling rate works at 240 MSPS with L=2 or L=1.

Table 4 Static Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential Nonlinearity	DNL	-0.3	±0.1	+0.3	LSB
Integral Nonlinearity	INL	-2	±1.6	2	LSB
Offset Error	VOS		0		LSB

Table 5 Dynamic Characteristics 1

Unless otherwise specified, AVDD1 = 0.975V, AVDD1_SR = 0.975V, AVDD2 = 1.8V, AVDD3 = 2.5V, DVDD = 0.975V, DRVDD1 =0.975V, DVDD2 = 1.8V, SPIVDD = 1.8V, fs = 500MSPS, clock divider ratio = 2, full-scale 1.8Vp-p input range, -55℃≤TA≤+125℃.

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Parameter	Symbol	Min.	Typ.	Max	Unit
Full Power Bandwidth:	FPBW		1.4		GHz
fs = 500MSPS					
Effective Number of Bits					
fin = 5.1 MHz	ENOB		10.48		bit
fin = 70.1 MHz			10.42		bit
fin = 275.3 MHz			10.38		bit
fin = 385.3 MHz			10.32		bit
fin = 475.3 MHz			10.25		bit
fin = 985.3 MHz			10.05		bit
Signal-to-Noise Ratio					
fin = 5.1 MHz	SNR		65.89		dBFS
fin = 70.1 MHz			65.76		dBFS
fin = 275.3 MHz			65.34		dBFS
fin = 385.3 MHz			65.12		dBFS
fin = 475.3 MHz			64.87		dBFS
fin = 985.3 MHz			63.71		dBFS
Spurious Free Dynamic Range					
fin = 5.1 MHz	|SFDR|		84.4		dBc
fin = 70.1 MHz			82.1		dBc
fin = 275.3 MHz			81.45		dBc
fin = 385.3 MHz			81.14		dBc
fin = 475.3 MHz			78.83		dBc
fin = 985.3 MHz			76.16		dBc
Second Harmonic					
fin = 5.1 MHz	|2^{nd} Harm|		82.6		dBc
fin = 70.1 MHz			81.25		dBc
fin = 275.3 MHz			81.44		dBc
fin = 385.3 MHz			80.51		dBc
fin = 475.3 MHz			78.63		dBc
fin = 985.3 MHz			75.88		dBc
The highest harmonic (excluding the second and third harmonics)					
fin = 5.1 MHz	|Worst Harm|		85.2		dBc
fin = 70.1 MHz			84.53		dBc
fin = 275.3 MHz			84.86		dBc
fin = 385.3 MHz			83.77		dBc
fin = 475.3 MHz			84.42		dBc
fin = 985.3 MHz			85.14		dBc

1. All test results are based on our test environment. Changes in test conditions may cause certain differences in test results.

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Table 6 Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
CLK+ to SYSREF+ Timing Requirements (Figure 5)					
t_{SU_SR}	CLK+ to SYSREF+ Setup Time		100		ps
t_{H_SR}	CLK+ to SYSREF+ Hold Time		65		ps
SPI Timing Requirements (Figure 6)					
t_{DS}	Data to SCLK Rising Edge Setup Time	4			ns
t_{DH}	Data to SCLK Rising Edge Hold Time	2			ns
t_{CLK}	SCLK time period	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum SCLK high time	10			ns
t_{LOW}	Minimum SCLK low time	10			ns
t_{ACCESS}	Maximum time delay between SCLK falling edge and output data during read operation		6	10	ns
t_{DIS_SDIO}	Time required for SDIO pin to switch from output to input relative to CSB rising edge	10			ns

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8.0 Pin configuration and functional description

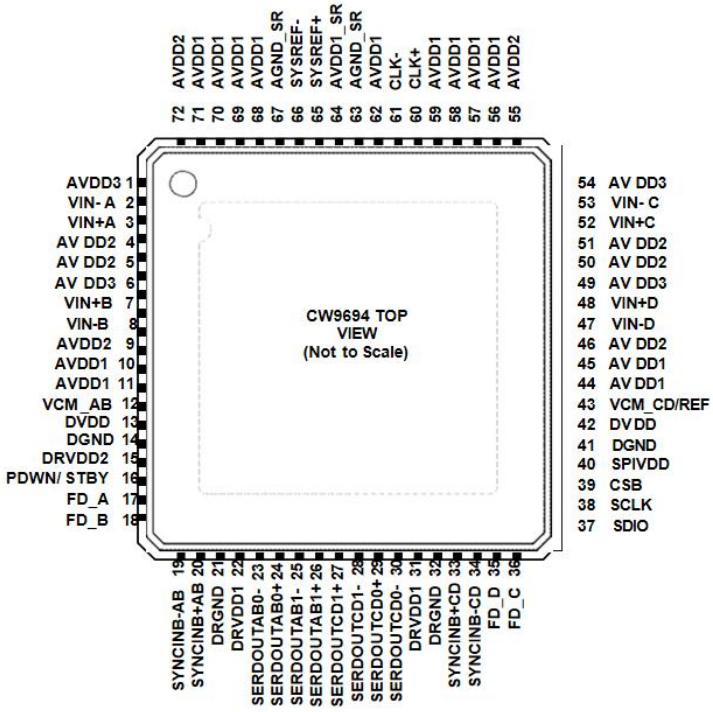

Figure 2 Pin Configuration of CW9694

Table 7 Pin function description

Pin number	Name	Function
Power supply pin		
10, 11, 44, 45, 56, 57, 58, 59, 62, 68, 69, 70, 71	AVDD1	Analog power supply voltage, default 0.975V.
4, 5, 9, 46, 50, 51, 55, 72	AVDD2	Analog power supply voltage, default 1.8V.
1, 6, 49, 54	AVDD3	Analog power supply voltage, default 2.5V.
64	AVDD1_SR	SYSREF±Analog power supply voltage, default 0.975V.
22, 31	DRVDD1	Digital drive power supply 1, default 0.975V.
15	DRVDD2	204B interface driver power 2, default 1.8V.
40	SPIVDD	SPI digital power supply voltage, default 1.8V.
13, 42	DVDD	Digital power supply voltage, default 0.95V.
0	AGND/EPAD	Analog ground/heat dissipation pad, EPAD must be grounded for normal operation
63, 67	AGND_SR	SYSREF± analog reference ground.
14, 41	DGND	Digital ground, reference ground for DVDD and SPIVDD
21, 32	DRGND	Digital ground, reference ground for DRVDD1 and DRVDD2.
Analog		
2, 3	VIN_A, VIP_A	ADC A analog input
7, 8	VIP_B, VIN_B	ADC B analog input

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52, 53	VIP_C, VIN_C	ADC C analog input
47, 48	VIN_D, VIP_D	ADC D analog input
60, 61	CLK_P, CLK_N	Clock input
12	VCM_AB	Common mode level bias outputs for analog input channels A and channel B
43	VCM_CD/VREF Output	Common mode level bias outputs for analog input channels C and D. (0.5V reference power pressure input). This pin can be configured as an output or input via SPI. If using an internal reference, use this pin as the common mode bias voltage output. If an external voltage reference source is used, this pin requires a 0.5 V reference voltage input

CMOS input/output		
17	FD_A/GPIO_A0	A channel fast detection output (FD_A).
36	FD_C/GPIO_A1	C channel fast detection output (FD_C).
18	FD_B/GPIO_B0	B-channel fast detection output (FD_B).
35	FD_D/GPIO_B1	D Channel Quick Detection Output (FD_D).
Digital input		
65, 66	SYSREF_P, SYSREF_N	SYSREF Reference Differential Signal Input (Low Valid)
20, 19	SYNCINB+AB/ SYNCINB-AB	204B interface (A/B channel) synchronous signal input (low valid)
33, 34	SYNCINB+CD/ SYNCINB-CD	204B interface (C/D channel) synchronous signal input (low valid)
Data output		
23, 24	SERDOUTAB0-/ SERDOUTAB0+	Lane 0 data output for channels A and B
25, 26	SERDOUTAB1-/ SERDOUTAB1+	Lane 1 data output for channels A and B
30, 29	SERDOUTCD0-/ SERDOUTCD0+	Lane 0 data output for channels C and D
28, 27	SERDOUTCD1-/ SERDOUTCD1+	Lane 1 data output for channels C and D
Digital control		
16	PDWN/STBY	Shutdown input (highly effective), the operation of this pin depends on SPI mode and can be configured For shutdown or standby, this pin requires an external 10kΩ pull-down resistor.
37	SDIO	SPI data input/output
38	SCLK	SPI serial clock
39	CSB	SPI chip selection (low valid)

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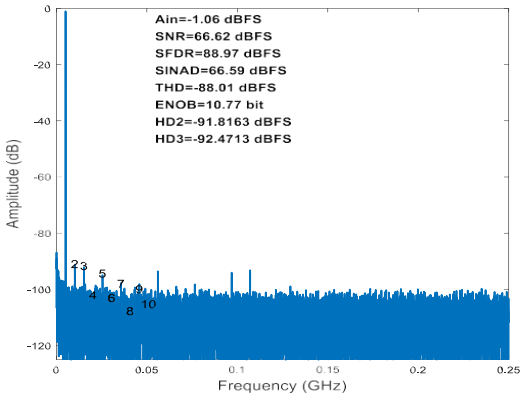
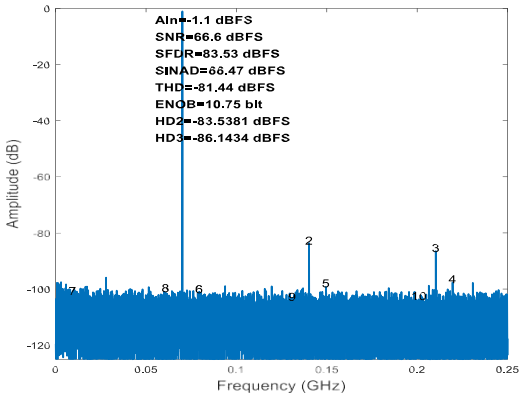
Typical performance test curve

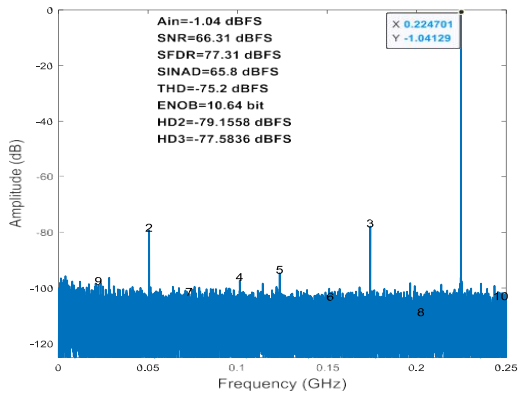
Typical scenario test, AVDD1 = 0.975V, AVDD1_SR = 0.975V, AVDD2 = 1.8V, AVDD3 = 2.5V, DVDD = 0.975V, DRVDD1 =0.975V, DVDD2 = 1.8V, SPIVDD = 1.8V, fs = 500MSPS, clock division ratio = 2, full-scale 1.8Vp-p input range, -55℃≤TA≤+125℃.



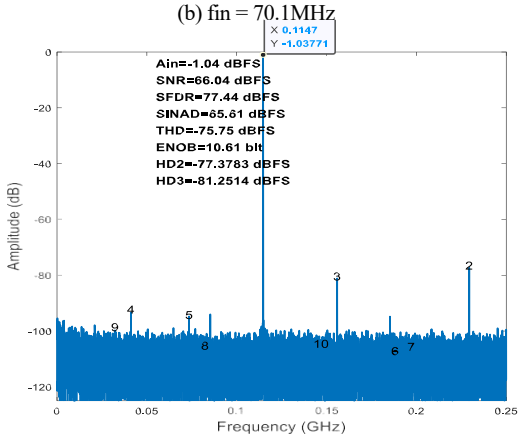
(a) fin = 5.1MHz



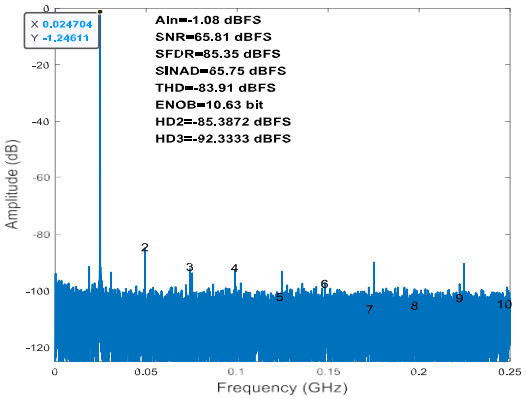
(b) fin = 70.1MHz



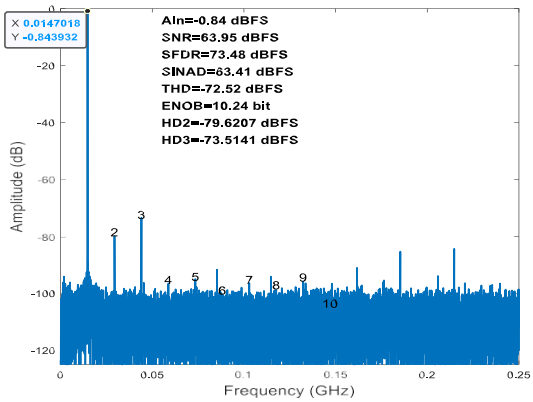
(c) fin = 275.3MHz



(d) fin = 385.3MHz



(e) fin = 475.3MHz



(f) fin = 985.3MHz

Figure 3 CW9694 dynamic characteristics test spectrum (fs = 500MSPS)

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10.0 Timing diagram

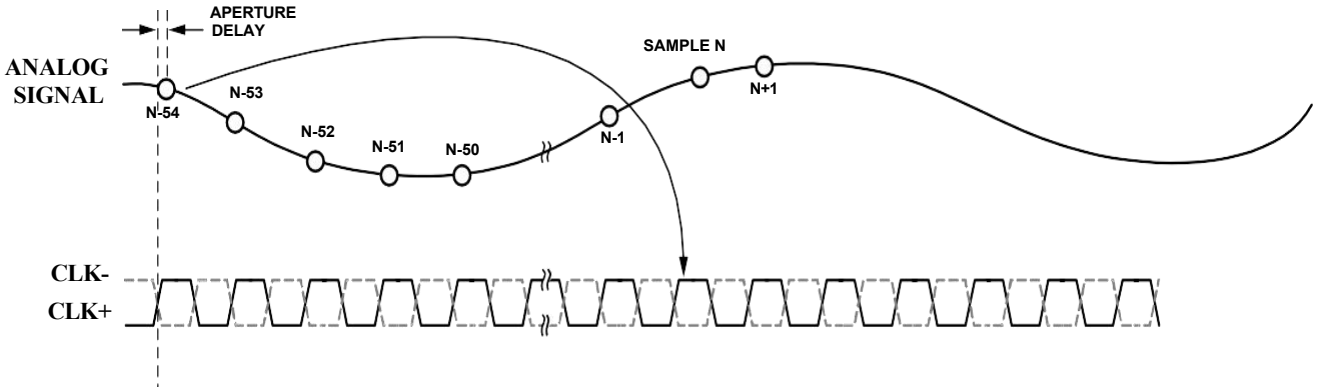

Figure 4 CW9694 data output timing diagram

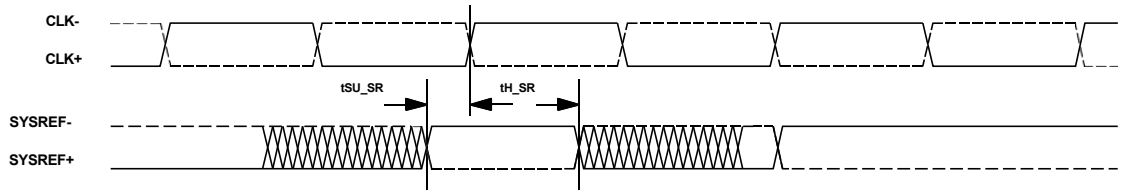

Figure 5 System synchronization reference signal establishment and maintenance timing diagram

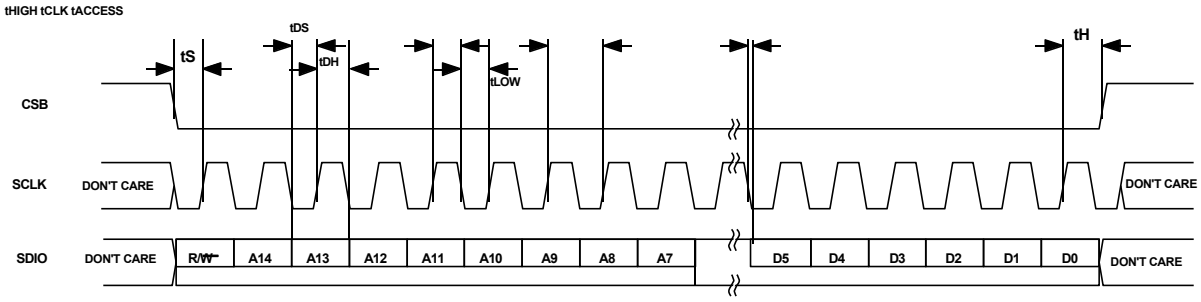

Figure 6 SPI interface timing diagram

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11.0 Basic working principle

11.1 Chip Architecture

The architecture of the CW9694 includes an input buffer pipeline ADC. The input buffer provides an analog input signal terminal impedance with a value of 200Ω, and the input signal buffering further optimizes the chip's linearity, noise and power consumption over a wide bandwidth.

Input buffers provide linear high input impedance (to simplify drive) and reduce Low ADC backlash. The buffer is optimized for high linearity, low noise and low power consumption. Quantitative outputs at each stage are combined to finally form a 14-bit conversion result in the digital correction logic. The rising edge of the clock is sampled, and the pipeline architecture allows the first stage to process new input samples, while other stages continue to process previous samples.

11.2 Analog input

The analog input of the CW9694 is a differential buffer. The internal common mode voltage of the buffer is 1.55V. The clock signal alternately switches the input circuit between the sampling mode and the hold mode.

A differential capacitor or two single-ended capacitors (or a combination of both) can be placed at the input to provide a matching passive network. These capacitors end up forming a low-pass filter that limits unnecessary broadband noise.

To obtain optimal dynamic performance, the source impedance of the drive VIN+x must be guaranteed. The source impedance of the drive VIN−x is matched to ensure that the common mode establishment error is symmetric. These errors are weakened by the common mode suppression of the ADC. In differential configurations, setting the ADC to the maximum range allows for the highest SNR performance.

11.2.1 Differential input configuration

The CW9694 has a variety of active or passive methods to drive, but differentially drives analog inputs to achieve optimal performance. In applications where SNR and SFDR are key parameters, since the noise performance of most amplifiers is not sufficient to achieve the true performance of the CW9694, differential transformer coupling is recommended in the input configuration, see Figures 7 and 8. For low and medium frequencies, dual-barron or dual-transformer networks are recommended for optimal performance of the CW9694. For higher frequencies in the second or third Nyquist zone, it is best to remove some front-end passive components to ensure they operate on broadband.

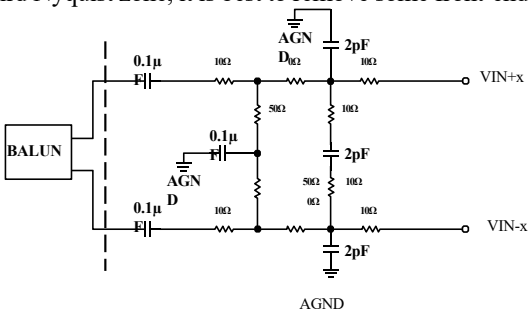

Figure 7 The input signal is in the first and second Nyquist zones (<500MHz) peripheral matching circuit

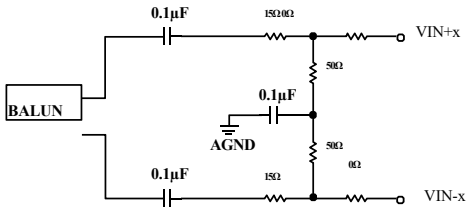

Figure 8 The input channel peripheral matching circuit when the input signal is in the third and fourth Nyquist zones (>500MHz)

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11.3 Clock input

For best performance, the CW9694 sample clock inputs (CLK+ and CLK−) are driven with a differential signal. This signal is usually coupled to the CLK+ and CLK− pins via the transformer or clock driver AC. These pins have internal biases and no additional bias is required.

Figure 9 shows the preferred method of clocking the CW9694. Use a RF transformer to convert a low jitter clock source from a single-ended signal to a differential signal.

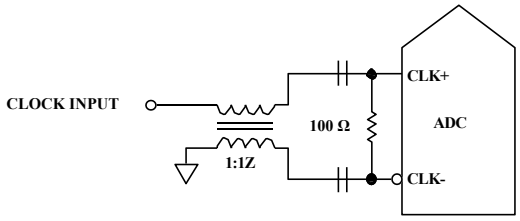

Figure 9 Transformer coupling differential clock

Another option is to AC-couple the differential CML or LVDS signal to the sampling clock input pin, as shown in Figures 10 and 11.

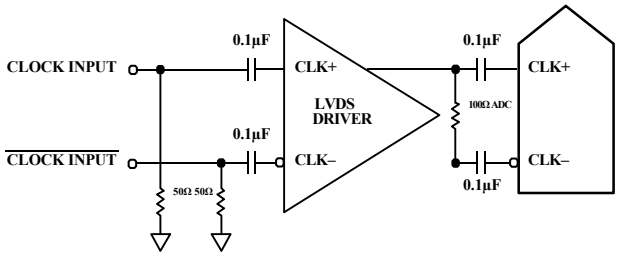

Figure 10 Differential LVDS sampling clock

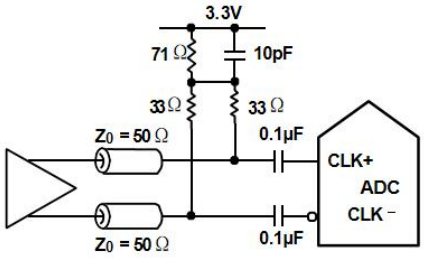

Figure 11 Differential CML Sampling Clock

11.3.1 Clock duty cycle

A typical high-speed ADC uses two clock edges to generate different timing signals.CW9694 includes an internal clock allocator and a duty cycle stabilizer(DCS), in applications where the clock duty cycle cannot be guaranteed to be 50%, it is recommended to use a higher multi-frequency clock and clock divider.

The output of the divider provides a 50% duty cycle, high conversion rate (fast edge) clock signal to the internal ADC. Turning on DCS requires SPI to perform a write operation. related For more information, see the Register Mapping section.

11.3.2 Input Clock Divider

The CW9694 contains an input clock divider that can divide the input clock by 1, 2, 4, or 8. Use register 0x0108 to select the divider ratio, see Figure 12.

In applications where the clock input is a multiple of the sample clock, be careful to set the appropriate frequency division ratio into the clock divider before applying the clock signal; this ensures that the transient current during device startup does not exceed the design redundancy.

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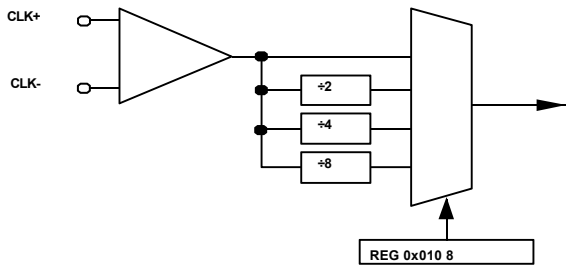

Figure 12 Clock Divider Circuit

The CW9694 clock divider can be synchronized using an external SYSREF± input signal. A valid SYSREF± signal resets the clock divider to a programmable state. This synchronization feature allows the clock dividers of multiple devices to be aligned to ensure synchronized input sampling. For more information, see the Register Mapping Table section.

Note: The 1-divider register is different from the AD9694. In addition to configuring 0x0108, you also need to configure 0x1C8B (write 0x01)

11.3.3 Clock Jitter

High-speed, high-resolution ADCs are very sensitive to the quality of the clock input. The SNR degradation due to aperture jitter (tJ) alone at a given input frequency (fIN) is calculated as follows:

$$SNR_{JITTER} = -20 \times \log10(2 \times \pi \times f_{IN} \times t_J)$$

Where the RMS of aperture jitter represents the RMS of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter. IF undersampling applications are particularly sensitive to jitter (see Figure 13).

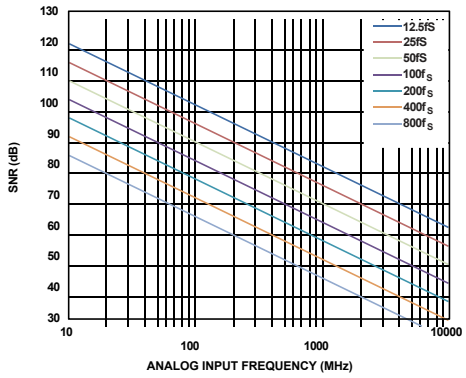

Figure 13 Ideal SNR vs. Input Frequency and Jitter

When aperture jitter may affect the dynamic range of the CW9694, the clock input should be treated as an analog signal. Separate the clock driver supply from the ADC output driver supply to avoid digital noise from being mixed into the clock signal. If the clock is generated by some other type of source (by gating, frequency division, or other methods), it will need to be retimed with the original clock in the last step.

Estimated SNR of CW9694 across input frequencies for different clock induced jitter values. The SNR can be estimated using the following formula:

$$SNR(dBFS) = -10\log_{10}\left(10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{JITTER}}{10}\right)}\right)$$

11.4 Power-Down/Standby Mode

The CW9694 has a PDWN/STBY pin that can be used to configure the device in power-down or standby mode, with the default configuration being PDWN. The PDWN/STBY pin is a logic high pin. In power-down mode, the JESD204B link is interrupted. Power-down mode options can also be set via Register 0x03F and Register 0x040.

In standby mode, the JESD204B link is not interrupted and all converter samples transmit 0. The transmitted value can be changed via Register 0x0571, Bit 7, Select K Character.

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12.0 ADC over-range and fast detection

In receiver applications, a reliable mechanism is needed to determine when a converter clamps occur. The standard overrange bits in the JESD204B output provide limited effect on analog input status information. Therefore, it is preferred to set a programmable threshold below the full scale to reduce the gain before clamping occurs. Additionally, since the slew rate of the input signal can be very high, the delay time of this function is critical. However, highly pipelined converters have very large delays. The CW9694 has a built-in detection circuit that can be used by each channel to monitor the threshold and set the FD_A, FD_B, FD_C and FD_D pins.

12.1 ADC overrange

The ADC overrange indicator will be set when an overrange is detected at the input of the ADC. The overrange indicator can be embedded as a control bit into the JESD204B link (when CS > 0), and the delay of the overrange indicator is consistent with the sampling delay.

12.2 Fast threshold detection (FD_A, FD_B, FD_C and FD_D)

As long as the absolute value of the input signal exceeds the programmable threshold limit, the Quick Detection bit in register 0x0040 is set immediately (4 channels are in the same configuration). The FD bit is cleared to 0 only if the absolute value of the input signal drops below the lower threshold limit and the duration exceeds the programmable residence time. This feature provides hysteresis to prevent FD bits from switching too frequently.

The operation of the upper and lower threshold registers and the dwell time registers

As shown in Figure 14.

The FD indicator is set when the input signal amplitude exceeds the setting value of the Fast Detection Threshold Upper Registers (Registers 0x247 and 0x248). The value of the selected threshold register is compared with the signal amplitude output by the ADC. The fast threshold upper limit detection has a delay of 28 clock cycles (maximum). The upper limit amplitude of the approximate threshold is defined by the following formula:

Upper threshold amplitude (dBFS) = 20 log (threshold amplitude/213)

The FD indicator will not be cleared until the signal drops below the lower threshold limit and the hold time exceeds the set dwell time. The lower threshold limit is set in the Quick Detection threshold limit registers (Registers 0x249 and 0x24A). The value of the 13-bit fast detection threshold lower limit register is compared with the signal amplitude output by the ADC. This comparison is controlled by the ADC pipeline delay; the comparison accuracy depends on the converter resolution. The lower limit range of the threshold is defined by the following formula:

Lower Threshold Amplitude (dBFS) = 20 log (Threshold Amplitude/2^{13})

For example, to set the upper threshold limit for −6 dBFS, 0xFFF should be written to register 0x247 and register 0x248; to set the lower threshold limit for −10 dBFS, 0xA1D should be written to register 0x249 and register 0x24A. The dwell time can be set in the range of 1 to 65535 sample clock cycles by writing the required value to the Quick Detection dwell time register (Registers 0x24B and 0x24C) and the program ranges from 1 to 65535 sample clock cycles.

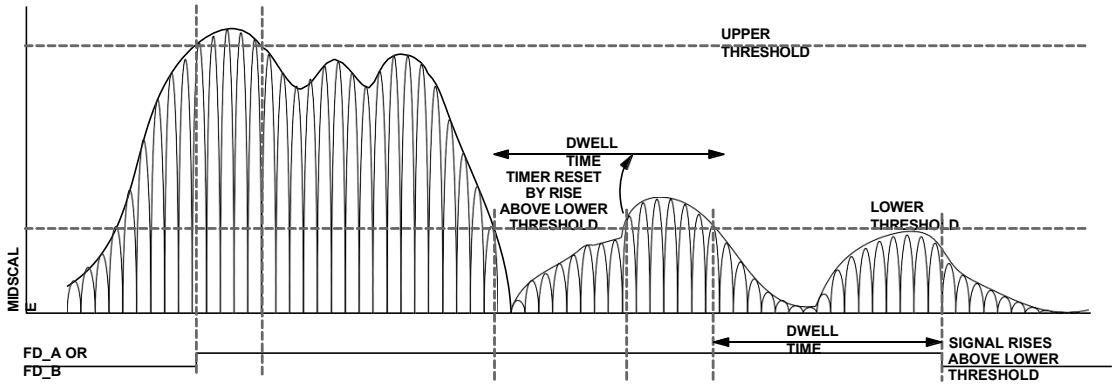

Figure 14 Threshold settings for FD_A and FD_B signals (FD_C and FD_D are also the same settings)

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13.0 Digital downconversion (DDC)

The CW9694 includes 4 digital downconverters (DDC0 to DDC3) that provide filtering and decimation to reduce output data rates. This digital processing section includes an NCO, multiple decimation FIR filters, a gain stage and a complex-real conversion stage. These processing modules have control lines that can be enabled or disabled individually to provide the required processing functions. By configuring a digital down-inverter, real or complex data can be output.

DDC outputs a 16-bit data stream. To enable this operation, the number of bits of the converter N must be set to 16, even if the analog core outputs only 14 bits. In full bandwidth operation mode, the ADC output is 14 data bits plus 2 bits 0 unless the control bit is used for other purposes.

13.1 DDC I/Q Input Selection

The CW9694 has 4 ADC channels and 4 DDC channels. Each DDC channel has two input ports that can be paired through an I/Q cross multiplexer to support real and complex inputs.

For real signals, the same input port must be selected for DDC connection ADC channel (i.e., DDC input port I=ADC channel A, DDC input port Q=ADC channel A).

For complex signals, a different ADC channel must be selected for each DDC input port (i.e., DDC input port I=ADC channel A DDC input port Q=ADC channel B or DDC input port I=ADC channel C DDC input port Q=ADC Channel D).

The inputs to each DDC are controlled jointly by the DDC input select register (Register 0x0311, Register 0x0331) and pair index register 0x0009.

13.2 DDC I/Q output selection

Each DDC channel has 2 output ports that can be paired to support real or complex outputs. For real output signals, only DDC output port I is used (DDC output port Q is not active). For complex I/Q output signals, both DDC output port I and DDC output port Q are used.

The I/Q output of each DDC channel is jointly controlled by the DDC complex to real enable bit (bit 3) in the DDC control register (register 0x310, register 0x330) and the pair index register 0x0009.

Chip Q Ignore bit in the Chip Application Mode Register (Register 0x200) (Bit 5) Controls the chip output complex for all DDC channels. When all DDC channels are using real outputs, this bit must be set high to ignore all DDC Q output port.

When setting any DDC channel to use complex I/Q outputs, the user must clear this bit to use both DDC output port I and DDC output port Q.

13.3 DDC Overview

The four DDC blocks are used to extract a portion of the fully digital spectrum captured by the ADC for use in mid-frequency sampled or oversampled baseband radio applications that require a wide bandwidth input signal.

Each DDC module contains the following signal processing stages:

- Frequency conversion stage (optional)
- filter level
- Gain stage (optional)
- Reconversion phase (optional)

13.3.1 Frequency conversion stage (optional)

The frequency conversion stage consists of a 48-bit complex NCO and a quadrature mixer that can be used for frequency conversion of real or complex input signals. This stage moves a portion of the available digital spectrum down to baseband.

13.3.2 Filter stage

After moving down to baseband, the filtering stage uses multiple low-pass finite impulse response (FIR) filters for rate conversion. The decimation process reduces the output data rate, thereby reducing the output interface rate.

13.3.3 Gain stage (optional)

Since there is a loss in mixing the real input signal to baseband, the gain stage compensates by adding an additional 0 dB or 6 dB of gain.

13.3.4 Complex to real conversion stage (optional)

When a real output is required, the complex-to-real conversion stage performs an fS/4 mixing operation and filters out the complex component of the signal, thereby converting the complex output back to a real output. Figure 15 shows a detailed block diagram of the DDC implemented in the CW9694.

Figure 16 shows an example of one of the DDC blocks in use with a real input signal and four half-band filters (HB4, HB3, HB2, and HB1).

Both complex (decimation by 16) and real (decimation by 8) output options are shown.

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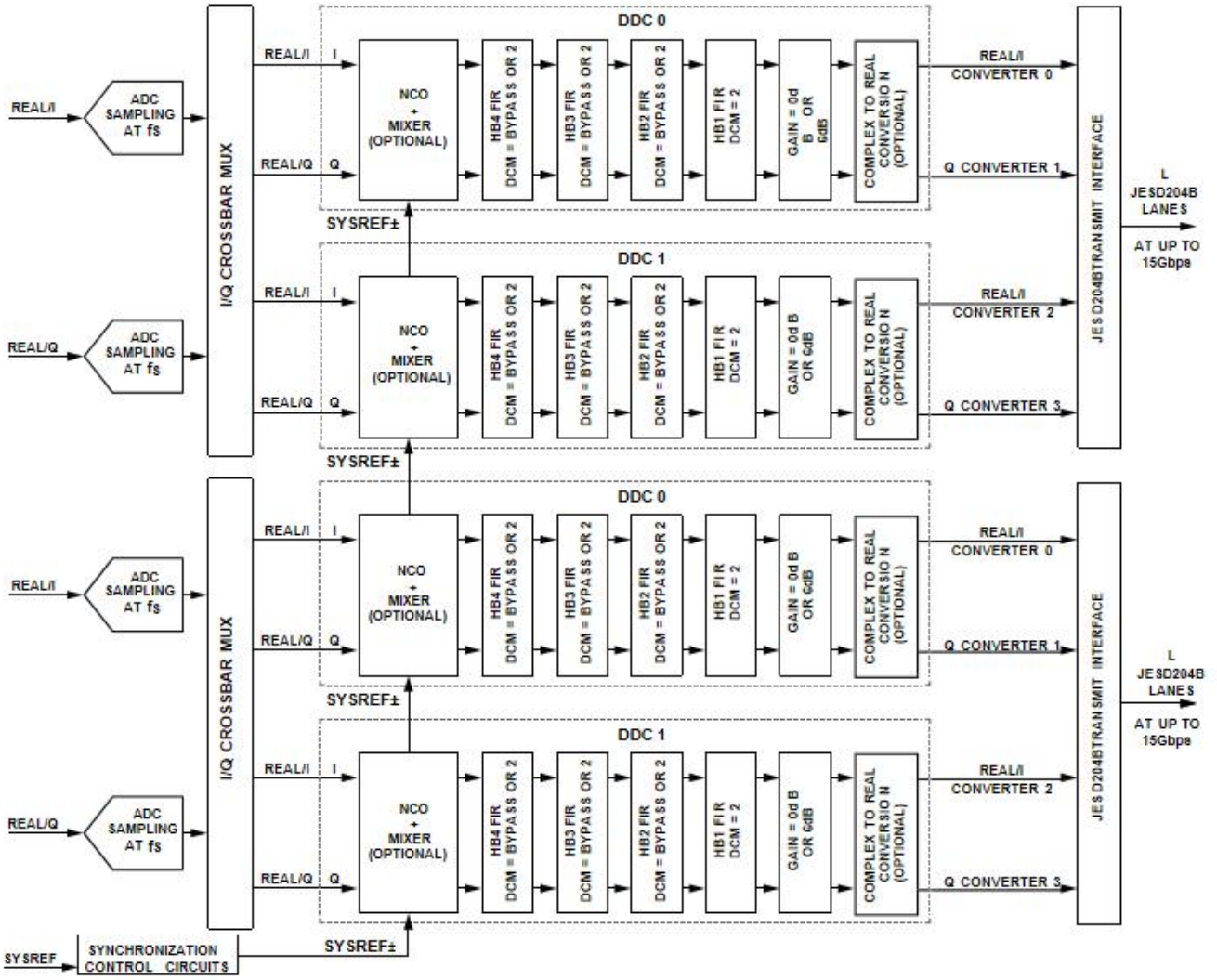

Figure 15 DDC detailed block diagram

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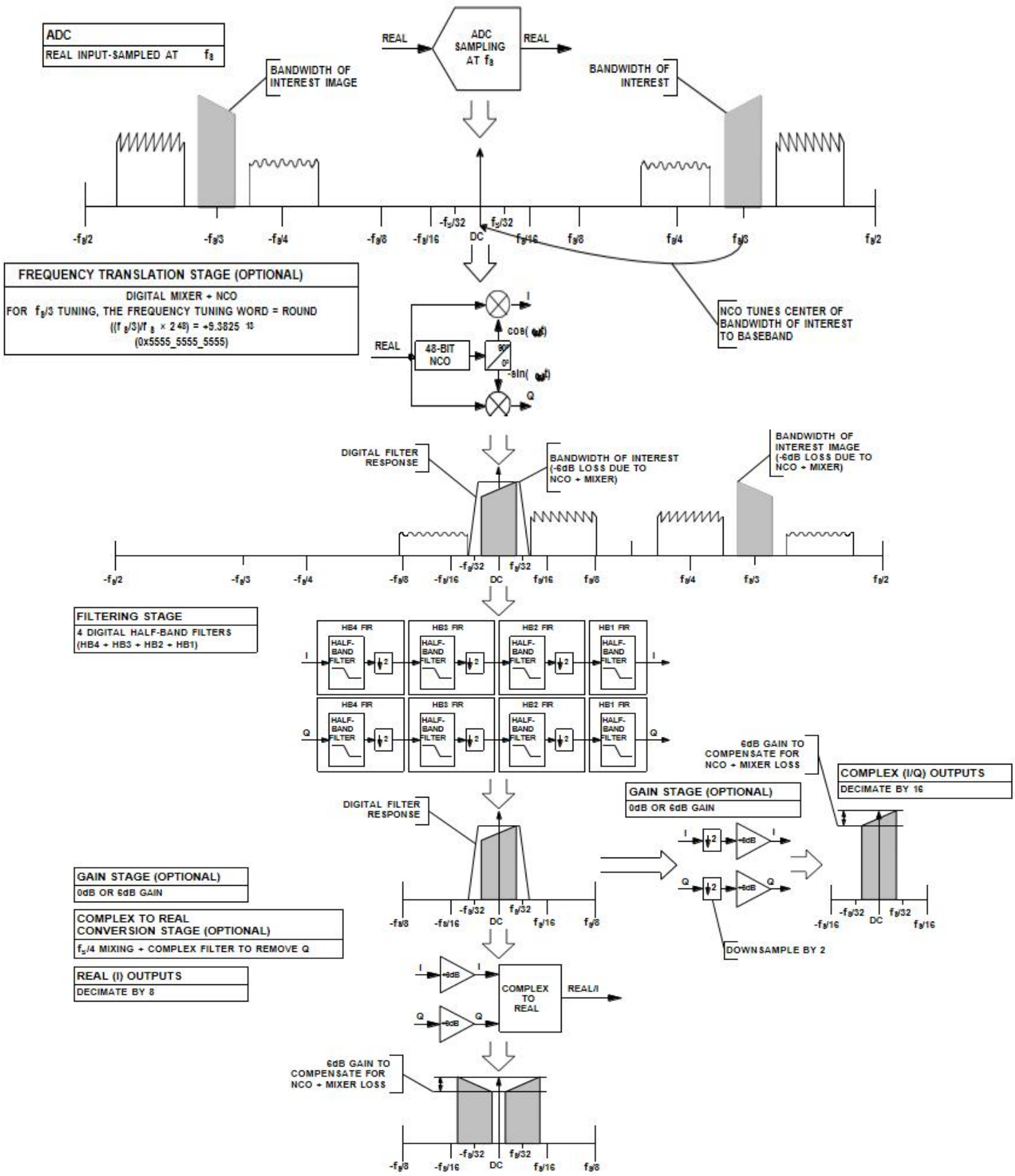

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Table 8 When chip extraction rate=1 DDC samples in each JESD204B link when

Real (I) Output (Complex to Real Enabled)				Complex (I/Q) Outputs (Complex to Real Disabled)			
HB1 FIR (DCM1= 1)	HB2 FIR+ HB1 FIR (DCM1 = 2)	HB3 FIR+ HB2 FIR+ HB1 FIR (DCM1 = 4)	HB4 FIR+ HB3 FIR+ HB2 FIR+ HB1 FIR (DCM1 = 8)	HB1 FIR (DCM1 = 2)	HB2 FIR+ HB1 FIR (DCM1 = 4)	HB3 FIR+ HB2 FIR+ HB1 FIR (DCM1 = 8)	HB4FIR+ HB3 FIR+ HB2 FIR+ HB1 FIR (DCM1 = 16)
N	N	N	N	N	N	N	N
N+1	N	N	N	N	N	N	N
N + 2	N + 1	N	N	N+1	N	N	N
N+3	N+1	N	N	N+1	N	N	N
N + 4	N + 2	N+1	N	N + 2	N+1	N	N
N+5	N + 2	N+1	N	N + 2	N+1	N	N
N + 6	N+3	N+1	N	N+3	N+1	N	N
N+7	N+3	N+1	N	N+3	N+1	N	N
N+8	N + 4	N + 2	N+1	N + 4	N + 2	N+1	N
N+9	N + 4	N + 2	N+1	N + 4	N + 2	N+1	N
N+10	N+5	N + 2	N+1	N+5	N + 2	N+1	N
N+11	N+5	N + 2	N+ 1	N + 5	N + 2	N+1	N
N+12	N + 6	N+3	N+1	N + 6	N+3	N+1	N
N+13	N + 6	N+3	N+1	N + 6	N+3	N+1	N
N+14	N+7	N+3	N+1	N+7	N+3	N+1	N
N+15	N+7	N+3	N+1	N+7	N+3	N+1	N
N+16	N+8	N + 4	N + 2	N+8	N + 4	N + 2	N+1
N+17	N+8	N + 4	N + 2	N+8	N + 4	N + 2	N+1
N+18	N+ 9	N + 4	N + 2	N+9	N + 4	N + 2	N+1
N+19	N+9	N + 4	N + 2	N+9	N + 4	N + 2	N+1
N+20	N+10	N+5	N + 2	N+10	N+5	N + 2	N+1
N+21	N+10	N+5	N + 2	N+10	N+5	N + 2	N+1
N+22	N+11	N+5	N + 2	N+11	N+5	N + 2	N+1
N+23	N+11	N+5	N + 2	N+11	N+5	N + 2	N+1
N+24	N+12	N + 6	N + 3	N + 12	N + 6	N+3	N+1
N+25	N+12	N + 6	N+3	N+12	N + 6	N+3	N+1
N+26	N+13	N + 6	N+3	N+13	N + 6	N+3	N+1
N+27	N+13	N + 6	N+3	N+13	N + 6	N+3	N+1
N+28	N+14	N+7	N+3	N+14	N+7	N+3	N+1
N+29	N+14	N+7	N+3	N+14	N+7	N+3	N+1
N+30	N+15	N+7	N+ 3	N + 15	N + 7	N + 3	N + 1
N+31	N+15	N+7	N+3	N+15	N+7	N+3	N+1

1. DCM: stands for Decimation

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Table 9 DDC samples per JESD204B link when chip decimation rate = 2

Real (I) Output (Complex to Real Enabled)			Complex (I/Q) Outputs (Complex to Real Disabled)			
HB2 FIR + HB1 FIR (DCM1 = 2)	HB3 FIR + HB2 FIR + HB1 FIR (DCM1 = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1 = 8)	HB1 FIR (DCM1=2)	HB2 FIR + HB1 FIR (DCM1 = 4)	HB3 FIR + HB2 FIR + HB1 FIR (DCM1 =8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1 = 16)
N	N	N	N	N	N	N
N + 1	N	N	N + 1	N	N	N
N + 2	N + 1	N	N + 2	N+1	N	N
N+3	N+1	N	N+3	N+1	N	N
N + 4	N + 2	N+1	N + 4	N + 2	N+1	N
N+5	N + 2	N+1	N+5	N + 2	N+1	N
N + 6	N+3	N+1	N + 6	N+3	N+1	N
N+7	N+3	N+1	N+7	N+3	N+1	N
N+8	N + 4	N + 2	N+8	N + 4	N + 2	N+1
N+9	N + 4	N + 2	N+9	N + 4	N + 2	N+1
N+10	N+5	N + 2	N+10	N+5	N + 2	N+1
N+11	N+5	N + 2	N+11	N+5	N + 2	N+1
N+12	N + 6	N+3	N+12	N + 6	N+3	N+1
N+13	N + 6	N+3	N+13	N + 6	N+3	N+1
N+ 14	N + 7	N + 3	N + 14	N + 7	N + 3	N + 1
N + 15	N + 7	N + 3	N + 15	N + 7	N + 3	N + 1

Table 10 DDC samples per JESD204B link when chip decimation rate = 4

Real (I) Output (Complex to Real Enabled)		Complex (I/Q) Outputs (Complex to Real Disabled)		
HB3 FIR + HB2 FIR + HB1 FIR (DCM1 = 4)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1= 8)	HB2 FIR + HB1 FIR (DCM1 = 4)	HB3 FIR + HB2 FIR + HB1 FIR(DCM1 = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1= 16)
N	N	N	N	N
N + 1	N	N + 1	N	N
N + 2	N + 1	N + 2	N + 1	N
N + 3	N + 1	N + 3	N + 1	N
N + 4	N + 2	N + 4	N + 2	N + 1
N + 5	N + 2	N + 5	N + 2	N + 1
N + 6	N + 3	N + 6	N + 3	N + 1
N + 7	N + 3	N + 7	N + 3	N + 1

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Table 11 DDC samples per JESD204B link when chip decimation rate = 8

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)	
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1= 8)	HB3 FIR + HB2 FIR + HB1 FIR (DCM1 = 8)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1 = 16)
N	N	N
N + 1	N + 1	N
N + 2	N + 2	N + 1
N + 3	N + 3	N + 1
N + 4	N + 4	N + 2
N + 5	N + 5	N + 2
N + 6	N + 6	N + 3
N+7	N+7	N + 3

Table 12 DDC samples in each JESD204B link when chip decimation rate = 16

Real (I) Output (Complex to Real Enabled)	Complex (I/Q) Outputs (Complex to Real Disabled)
HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1 = 16)	HB4 FIR + HB3 FIR + HB2 FIR + HB1 FIR (DCM1 = 16)
Not applicable	N
Not applicable	N + 1
Not applicable	N + 2
Not applicable	N + 3

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13.4 DDC frequency conversion

13.4.1 DDC Frequency Conversion Overview

Frequency conversion is achieved by using a 48-bit complex NCO with a digital orthogonal mixer. Frequency conversion transfers a real or complex input signal from the intermediate frequency (IF) Convert to baseband complex digital output (carrier frequency = 0 Hz).

The frequency conversion stage of each DDC can be controlled individually, supporting four different IF modes, using the DDC control registers (Register 0x0310, Register 0x0330, and the index register (0x0009). These IF modes The formula is as follows:

- Variable medium frequency mode
- 0 Hz IF or Zero IF (ZIF) mode
- fS/4 Hz IF mode
- Test mode

13.4.2 Variable intermediate frequency mode

The NCO and mixer are enabled. The NCO output frequency can be used to digitally modulate the IF frequency.

13.4.3 0 Hz IF or Zero IF (ZIF) Mode

The mixer is bypassed and the NCO is disabled.

13.4.4 fS/4 Hz IF Mode

The mixer and NCO operate in a special fS/4 downmixing mode to save device power.

13.4.5 Test Mode

By forcing the input samples to 0.999 times the ADC full scale and enabling the NCO, this test mode allows the NCO output to go directly to the decimation filter. Figure 17 and Figure 18 show examples of frequency conversion stages for real and complex inputs.

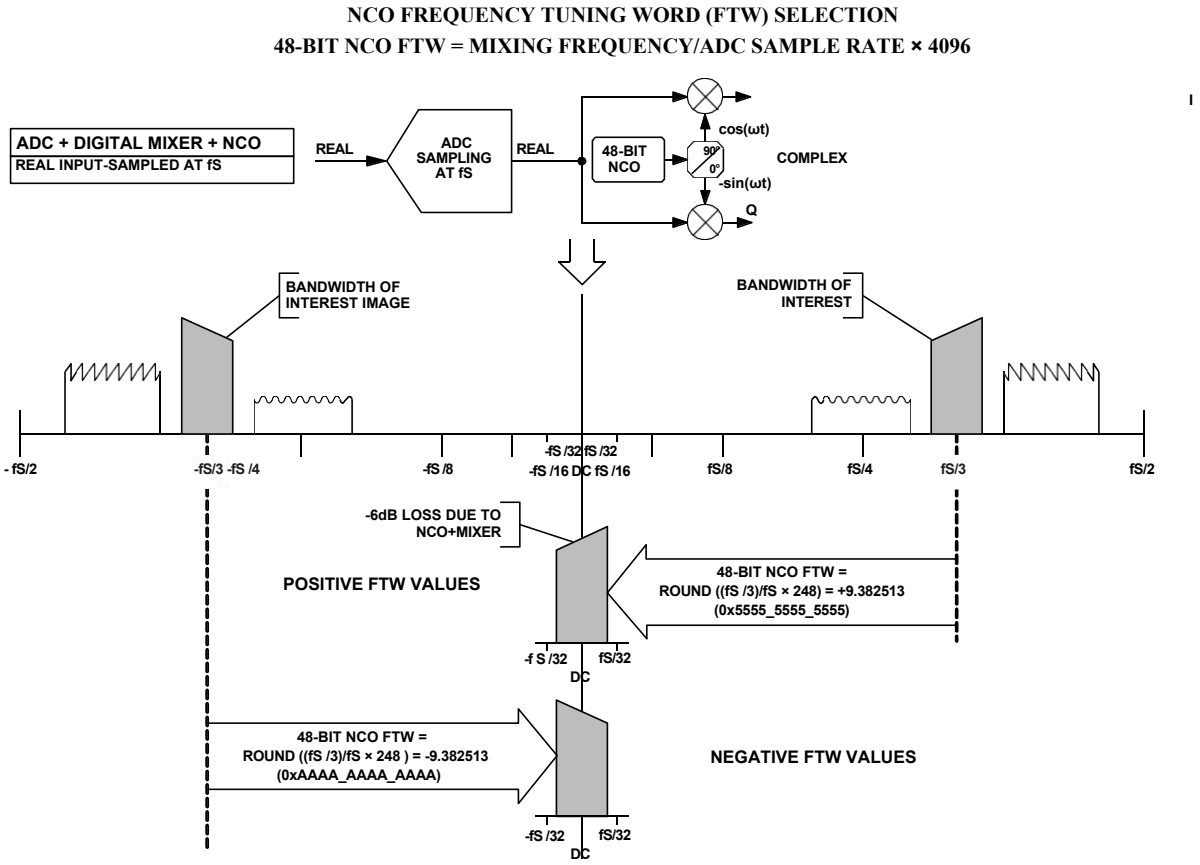

Figure 17 DDC NCO frequency tuning word selection – real input

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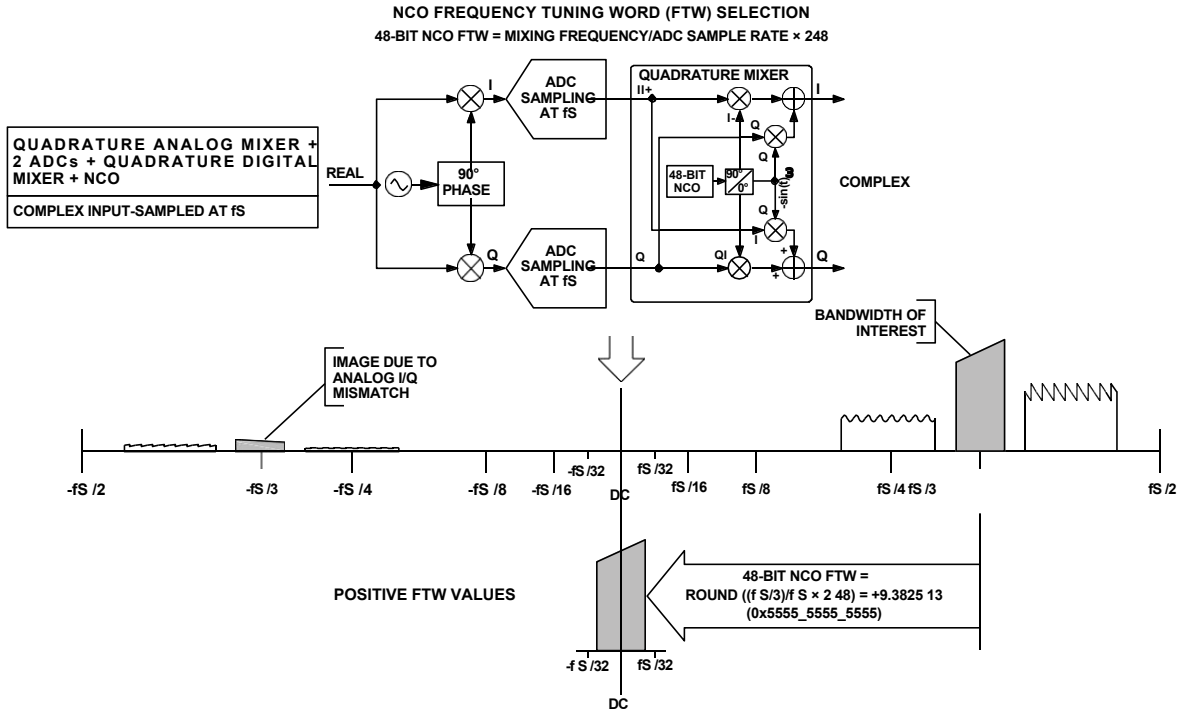

Figure 18 DDC NCO Frequency Tuning Word Selection - Complex Input

13.4.6 DDC NCO + Mixer Loss and SFDR

When mixing a real input signal to baseband, a loss of −6 dB is introduced into the signal due to filtering of negative images. The NCO additionally adds a loss of −0.05 dB. The total loss for the real input signal mixed to baseband is −6.05 dB. Therefore, it is recommended that users compensate for this loss by enabling the 6 dB gain in the DDC gain stage, thereby repositioning the dynamic range center of the signal within the full-scale range of the output bits.When mixing a complex input signal (where the DDC inputs of I and Q come from different ADCs) to baseband, the maximum value that each I/Q sample can reach after passing through the complex mixer is 1.414 times the full scale. To avoid excessive range of I/Q samples and maintain the data bit width consistent with that of the real mixer, a loss of −3.06 dB is introduced in the mixer for the complex signal. The NCO adds an additional loss of −0.05 dB. The total loss for the complex input signal mixed to baseband is −3.11 dB.

13.4.7 Numerically Controlled Oscillator

CW9694 provides a 48-bit NCO (Numerically Controlled Oscillator) for each DDC (Digital Down Converter) to enable the frequency conversion process. The NCO allows tuning the input spectrum to DC (Direct Current), where it can be effectively filtered by the subsequent filter block to prevent aliasing. The NCO can be configured by providing a Frequency Tuning Word (FTW) and a Phase Offset Word (POW).

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13.4.8 Setting NCO FTW/POW

The NCO frequency value is given by a 48-bit two's complement number input in the NCO FTW (Frequency Tuning Word), representing frequencies between $-f_S/2$ and $+f_S/2$ (excluding $+f_S/2$). Frequencies are denoted by the following settings:

- 0x800 represents a frequency of $-f_S/2$.
- 0x000 represents direct current (DC, with a frequency of 0 Hz).
- 0x7FF represents a frequency of $+f_S/2 - f_S/2^{12}$.

The NCO frequency tuning word can be calculated using the following formula:

$$NCO\_FTW = \text{round}\left(2^{48}\frac{\text{mod}(f_c, f_s)}{f_s}\right)$$

Where:

- FTW is a 48-bit two's complement code representing NCO_FTW.
- f_C is the desired carrier frequency in Hertz (Hz).
- f_S is the ADC sampling rate in Hertz (Hz).

round(x) is a rounding function where round(3.6) = 4. For negative numbers, round(–3.4) = –3.

mod(x) is a remainder function where mod(110, 100) = 10. For negative numbers, mod(–32, 10) = –2.

For example, if the ADC sampling frequency f_S is 500 MSPS and the carrier frequency f_C is 140.312 MHz, then:

$$NCO\_FTW = \text{round}\left(2^{48}\frac{\text{mod}(140.312,500)}{500}\right)$$
$$= 7.89886 \times 10^{13} Hz$$

It is then converted into a 12-bit two's complement code for NCO_FTW, resulting in 0x47D.
The actual carrier frequency F_{C_ACTUAL} is calculated using the following formula:

$$f_{C\_ACTUAL} = \frac{NCO\_FTW \times f_S}{2^{48}} = 140.312\text{MHz}$$

Each NCO can use a 48-bit POW to create known phase relationships between multiple chips or individual DDC channels within a chip.

Use the following procedure to update the FTW and/or POW registers for ensuring normal NCO operation:

Write the FTW registers of all DDCs.

Write the POW registers of all DDCs.

Synchronize the NCO by asserting the DDC NCO soft reset bit (Register 0x0300, Bit 4) accessible via SPI or through the SYSREF± pins.

It must be noted that after completing all writes to the FTW or POW registers, the NCO must be synchronized via SPI or the SYSREF± pins. This step is essential to ensure the NCO operates normally.

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13.4.9 NCO Synchronization

Each NCO contains a separate Phase Accumulator Word (PAW). The initial reset value of each PAW is set to zero, and the phase increment value of each PAW is determined by the FTW. The POW is added to the PAW to generate the NCO's instantaneous phase. For more information, refer to the "Setting NCO FTW and POW" section.

Two methods are available to synchronize multiple PAWs within the chip:

1.Using SPI:

Reset all PAWs in the chip via the DDC NCO soft reset bit in the DDC Synchronization Control Register (Register 0x0300, Bit 4). This is done by setting the DDC NCO soft reset bit to high and then to low. This method can only synchronize DDC channels within the same pair (A/B or C/D) of an CW9694 chip.

2.Using SYSREF± Pins:

When the SYSREF± pins in the SYSREF± Control Registers (Registers 0x0120 and 0x0121) are enabled, and DDC synchronization in the DDC Synchronization Control Register (Register 0x0300, Bits [1:0]) is enabled, any subsequent SYSREF± event will reset all PAWs in the chip. This method can synchronize DDC channels within the same CW9694 chip or across separate CW9694 chips.

13.4.10 Mixer Description

When enabling the DDC, the NCO mixer performs operations similar to an analog quadrature mixer. It downconverts the input signal (real or complex) by using the NCO frequency as a local oscillator.

For a real input signal, a real mixer operation (with two multipliers) is performed. For a complex input signal, a complex mixer operation (with four multipliers and two adders) is executed. The selection of real or complex input for each DDC block can be individually controlled via Bit 7 of the DDC Control Registers (0x0310, 0x0330) and the Index Register (0x0009).

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13.5 FIR filter

After frequency conversion, there are four sets of 2x decimation, low pass, half-band, and finite impulse responses

(FIR) filter: HB1 FIR, HB2 FIR, HB3 FIR, and HB4 in Figure 15 FIR, these filters are located after the frequency conversion stage. After the target carrier drops to DC (carrier frequency = 0 Hz), these filters efficiently reduce the sampling rate, while Provide sufficient aliasing suppression to prevent useless adjacent carriers around the target bandwidth from affecting the signal.

HB1 FIR is always enabled and cannot be bypassed in DDC mode. HB2,

HB3 and HB4 FIR filters are optional and can be bypassed to improve output sampling

rate.

Table 13 shows the different bandwidths that can be selected by different half-band filters. In all cases, the DDC filter stage on the CW9694 provides passband ripple less than 0.001 dB and stopband aliasing suppression greater than 100dB.

Table 14 shows multiple stopband aliasing suppression showing multiple bandpass ripple/cut-off points. The filter stage decimation of each DDC stage can be passed through the DDC control register.
(Register 0x0310 and Register 0x0330) bits [1:0] and the index registers (Register 0x0008, Register 0x0009).

Table 13 DDC filter characteristics

Half-band filter selection	Real number output		**Complex (I/Q) output**		Aliasing protection bandwidth **(MHz)**	Ideal signal-to-noise ratio Improved **(dB)**	Passband ripple **(dB)**	Aliasing suppression **(dB)**
	Draw ratio	Real output Sampling rate (MSPS)	Draw ratio	Complex (I/Q) output sampling rate (MSPS)				
HB1	1	500	2	250 (I) + 250 (Q)	200	1	<−0.0001	>100
HB1 + HB2	2	250	4	125 (I) + 125 (Q)	100	4		
HB1+HB2+HB3	4	125	8	62.5 (I) + 62.5 (Q)	50	7		
HB1+HB2+HB3 + HB4	8	62.5	16	31.25 (I) + 31.25 (Q)	25	10		

Note: Ideal SNR improves due to oversampling + filtering > 10log (bandwidth/fS/2).

Table 14 DDC filter passband and stopband

Stopband Suppression (dB)	Passband ripple (dB)	Real number output 1	**Complex (I/Q) output**
>100	<−0.0001	<40% ×f_{OUT}	<80% ×f_{OUT}
95	<−0.0002	<40.12% ×f_{OUT}	<80.12% ×f_{OUT}
90	<−0.0003	<40.23% ×f_{OUT}	<80.46% ×f_{OUT}
85	<−0.0005	<40.36% ×f_{OUT}	<80.72% ×f_{OUT}
80	<−0.0009	<40.53% ×f_{OUT}	<81.06% ×f_{OUT}
25.07	−0.5	45.17% ×f_{OUT}	90.34% ×f_{OUT}
19.3	−1.0	46.2% ×f_{OUT}	92.4% ×f_{OUT}
10.7	−3.0	48.29% ×f_{OUT}	96.58% ×f_{OUT}

Note: f_{OUT} = ADC Input sampling rate/DDC decimation.

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13.5.1 HB4 filter description

The first 2x decimation, half-band, low-pass FIR filter (HB4) uses an 11-tap, symmetric, fixed coefficient filter scheme, optimized for low power consumption. The HB4 filter is only used when complex output (16x decimation) or real output (8x decimation) is enabled, and the filter should be bypassed in other cases.

Table 15 and Figure 19 show the coefficients and responses of the HB4 filter.

Table 15 HB4 filter coefficients

HB4 Coefficient Number	Normalized Coefficient	Decimal Coefficient (15-Bit)
C1, C11	+0.006042	+99
C2, C10	0	0
C3, C9	−0.049377	−809
C4, C8	0	0
C5, C7	+0.293335	+4806
C6	+0.5	+8192

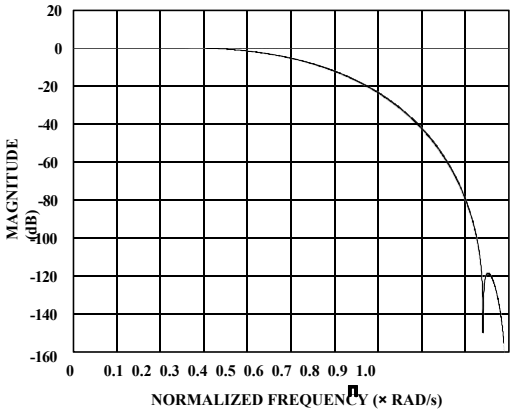

Figure 19 HB4 filter response

13.5.2 HB3 filter description

The second 2x decimation, half-band, low-pass FIR filter (HB3) uses an 11-tap, symmetric, fixed coefficient filter scheme, optimized for low power consumption. The HB3 filter is only used when the complex output (8x or 16x decimation) or real output (4x or 8x decimation) is enabled, and the filter should be bypassed in other cases. surface 16 and Figure 20 are the coefficients and responses of the HB3 filter.

Table 16 HB3 filter coefficients

HB3 Coefficient Number	Normalized Coefficient	Decimal Coefficient (17-Bit)
C1, C11	+0.006638	+435
C2, C10	0	0
C3, C9	−0.051056	−3346
C4, C8	0	0
C5, C7	+0.294418	+19295
C6	+0.500000	+32768

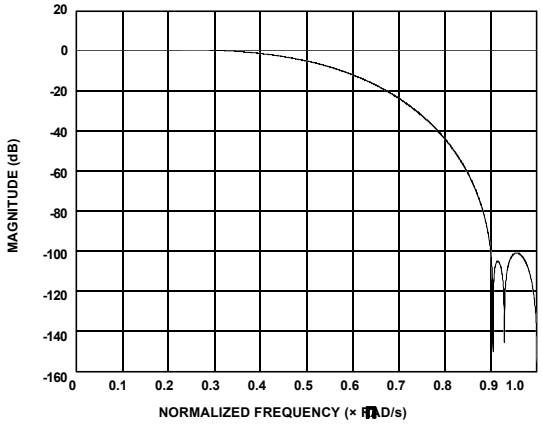

Figure 20 HB3 filter response

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13.5.3 HB2 filter description

The third 2x decimation, half-band, low-pass FIR filter (HB2) uses 19

The tap, symmetric, fixed coefficient filter solution is optimized for low power consumption.

The HB2 filter is only used when complex output or real output (4x, 8x, or 16x decimation) is enabled and should be bypassed in other cases.

Table 17 and Figure 21 show the coefficients and responses of the HB2 filter.

Table 17 HB2 filter coefficients

HB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (18-Bit)
C1, C19	+0.000671	+88
C2, C18	0	0
C3, C17	−0.005325	−698
C4, C16	0	0
C5, C15	+0.022743	+2981
C6, C14	0	0
C7, C13	−0.074181	−9723
C8, C12	0	0
C9, C11	+0.306091	+40120
C10	+0.5	+65536

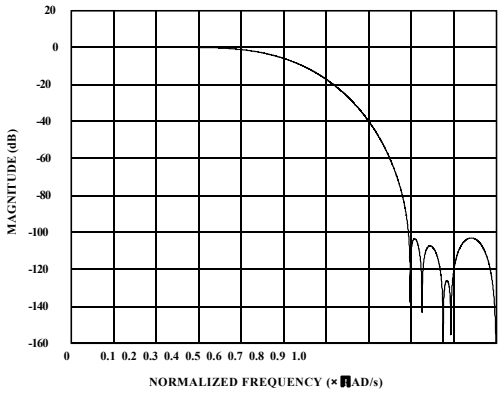

Figure 21 HB2 filter response

13.5.4 HB1 filter description

The fourth and last 2x decimation, half band, low pass FIR filter (HB1) uses a 63-tap, symmetric, and fixed coefficient filter solution, and is optimized for low power consumption.

The HB1 filter is always enabled and cannot be bypassed. Table 18 and Figure 22 are The coefficients and response of the HB1 filter.

Table 18 HB1 filter coefficients

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (20-Bit)
C1, C63	−0.000019	−10
C2, C62	0	0
C3, C61	+0.000072	+38
C4, C60	0	0
C5, C59	−0.000195	−102
C6, C58	0	0
C7, C57	+0.000443	+232
C8, C56	0	0
C9, C55	−0.000891	−467
C10, C54	0	0
C11, C53	+0.001644	+862
C12, C52	0	0
C13, C51	−0.002840	−1489
C14, C50	0	0
C15, C49	+0.004654	+2440
C16, C48	0	0
C17, C47	−0.007311	−3833
C18, C46	0	0
C19, C45	+0.011122	+5831
C20, C44	0	0
C21, C43	−0.016554	−8679
C22, C42	0	0
C23, C41	0.024420	12803
C24, C40	0	0
C25, C39	−0.036404	−19086
C26, C38	0	0
C27, C37	+0.056866	+29814
C28, C36	0	0
C29, C35	−0.101892	−53421
C30, C34	0	0
C31, C33	+0.316883	+166138
C32	+0.5	+262144

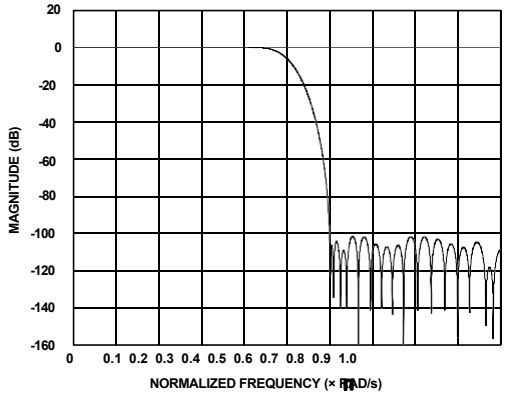

Figure 22 HB1 filter response

13.6 DDC Gain Level

Each DDC contains an independently controlled gain stage. A gain of 0 dB or 6 dB can be selected. When the real input signal is downmixed to baseband, it is recommended that the user enable 6 dB gain to reposition the center of the dynamic range of the signal within the full scale of the output bit.

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When the complex input signal is downmixed to the baseband, the mixer has repositioned the center of the dynamic range of the signal within the full scale of the output bit without the need for positioning gain. However, an optional 6 dB gain can be used to compensate for lower-strength signals. When using the complex to real conversion stage, the 2-fold downsampling portion of the HB1 FIR filter is bypassed, and the TB1 filter does not have a 6dB gain stage.

Each DDC contains an independently controlled complex to real conversion module. The complex to real conversion module reuses the last filter (HB1 FIR) of the filter stage and upconverts the signal together with an fS/4 complex mixer.

After the signal is upconverted, the Q part of the complex mixer is no longer needed and is therefore discarded. The TB1 filter does not support complex to real conversion. Figure 23 shows the revision Schematic block diagram of counting to real numbers.

13.7 DDC complex-real conversion

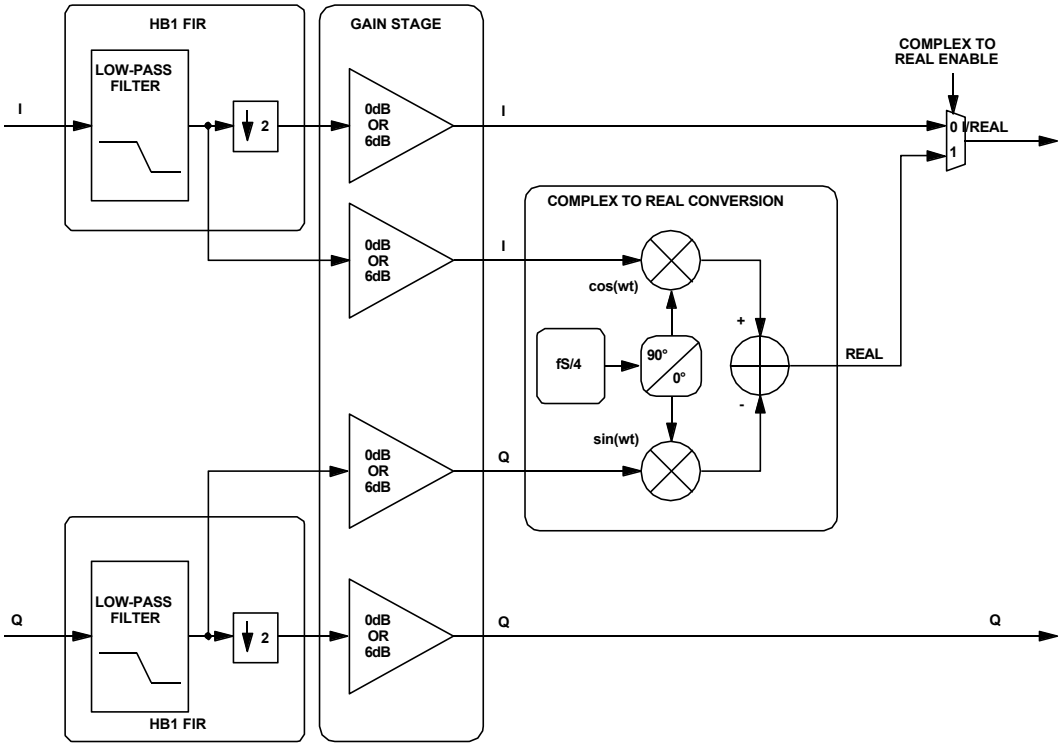

Figure 23 Block diagram of the complex to real number conversion module

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13.8 DDC configuration example

Table 19 describes the register settings for multiple DDC example configurations. Table 19 DDC configuration examples

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Input Type	Bandwidth Per DDC1	No. of Virtual Converters Required	Register Settings
One DDC	2	Complex	Complex	40%×fS	2	0x0200 = 0x01 (one DDC; I/Q selected) 0x0201 = 0x01 (chip decimate by 2) 0x0310 = 0x83 (complex mixer; 0 dB gain; variable IF; complex outputs; HB1 filter) 0x0311 = 0x04 (DDC I Input = ADC Channel A; DDC Qinput = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B,0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 =FTW and POW set as required by application for DDC0
One DDC	4	Complex	Complex	20%×fS	2	0x0009 = 0x01, 0x02, or 0x03 (pair selection) 0x0200 = 0x01 (one DDC; I/Q selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310 = 0x80 (complex mixer; 0 dB gain; variable IF; complex outputs; HB2 + HB1 filters) 0x0311 = 0x04 (DDC I input = ADC Channel A/C; DDC Q input = ADC Channel B/ Channel D) 0x0314, 0x0315,.0x0316, 0x0317, 0x0318, 0x031A, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC 0
Two DDCs	2	Real	Real	20%×fS	2	0x0009 = 0x01, 0x02, or 0x03 (pair selection) 0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x01 (chip decimate by 2) 0x0310, 0x0330 = 0x48 (real mixer; 6 dB gain; variable IF; real output; HB2 + HB1 filters) 0x0311 = 0x00 (DDC 0 I input = ADC Channel A/Channel C; DDC 0 Q input = ADC Channel A/Channel C) 0x0331 = 0x05 (DDC 1 I input = ADC Channel B/Channel D; DDC 1 Q input = ADC Channel B/Channel D 0x0314,.0x0315,0x0316,.0x0317,0x0318,0x031A, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC 0 0x0334, 0x0335, 0x0336, 0x0337, 0x0338, 0x033A, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC 1

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Two DDCs	2	Complex	Complex	40%×fS	4	0x0009 = 0x01, 0x02, or 0x03 (pair selection) 0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x01 (chip decimate by 2) 0x0310, 0x0330 = 0x4B (complex mixer; 6 dB gain; variable IF; complex output; HB1 filter) 0x0311, 0x0331 = 0x04 (DDC 0 I input = ADC Channel A/Channel C; DDC 0 Q input = ADC Channel B/Channel D) 0x0314, 0x0315, 0x0316, 0x0317, 0x0318, 0x031A, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC 0 0x0334,0x0335,0x0336,0x0337,0x0338,0x033A, 0x033D,0x033E,0x033F,0x0340, 0x0341,0x0342 = FTW and POW set as required by application for DDC 1
Two DDCs	4	Complex	Complex	20%×fS	4	0x0200 = 0x02 (two DDCs; I/Q selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x80 (complex mixer; 0 dB gain; variable IF; complex outputs; HB2+HB1 filters) 0x0311, 0x0331 = 0x04 (DDC I input = ADC Channel A;DDC Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B,0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 =FTW and POW set as required by application for DDC0
						0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B,0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 =FTW and POW set as required by application for DDC1
Two DDCs	4	Complex	Real	10%×fS	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x89 (complex mixer; 0 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) 0x0311, 0x0331 = 0x04 (DDC I Input = ADC Channel A; DDC Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1

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Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Input Type	Bandwidth Per DDC1	No. of Virtual Converters Required	Register Settings
Two DDCs	4	Real	Real	10%×fS	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x49 (real mixer; 6 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x05 (DDC1 I input = ADC Channel B; DDC1 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1
Two DDCs	4	Real	Complex	20%×fS	4	0x0200 = 0x02 (two DDCs; I/Q selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x40 (real mixer; 6 dB gain; variable IF; complex output; HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x05 (DDC1 I input = ADC Channel B; DDC1 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1
Two DDCs	8	Real	Real	5%×fS	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x05 (DDC1 I input = ADC Channel B; DDC1 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1

1 f_S represents the sampling rate of the ADC.

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14.0 Digital output

14.1 Introduction to JESD204B Interface

The CW9694 digital output is designed according to JEDEC standard JESD204B ("Data Converter Serial Interface"). JESD204B is the protocol for CW9694 to connect to digital processing devices via a serial interface (channel rates up to 13.1 Gbps). Advantages of the JESD204B interface over LVDS include less board space required for data interface cabling and smaller packages of converters and logic devices.

14.2 JESD204B Overview

The JESD204B data transmission block combines parallel data from the ADC into data frames and uses 8B/10B encoding and optional data scrambling technology to output serial data. During the initial link establishment process, channel synchronization is supported by using special control characters; subsequent synchronization is maintained by embedding additional control characters in the data stream. A JESD204B receiver needs to complete the serial link. For additional details about the JESD204B interface, see the JESD204B standard.

CW9694 JESD204B data sending module can be imaged at most on one link 4 real ADCs or 8 virtual converters (when DDC is enabled). A link can be configured to use 1, 2, or 4 JESD204B channels. The JESD204B specification references many parameters to define the link, and these parameters of the JESD204B transmitter (CW9694 output) and the JESD204B receiver (logic device input) must match.

The JESD204B link can be described by the following parameters:

- L is the number of data paths (CW9694 value = 1, 2)
- M is the number of converters (number of virtual converters) (CW9694 value = 1, 2, or 4)
- F is the number of bytes per frame (CW9694 value = 1, 2, 4, 8)
- N′ is the number of bits required to transmit 1 sample (JESD204B word length) (CW9694 value = 8 or 16)
- N is the converter resolution (CW9694 value = 7 ~ 16)
- CS is the control bit/sample number (CW9694 value = 0, 1, 2 or 3)
- K is the number of frames per multi-frame (the value of CW9694 = 4, 8, 12, 16, 20, 24, 28 or 32)
- S is the number of samples of a single converter within a single frame (CW9694 value according to Automatically set by L, M, F, N′)
- HD is high density mode (CW9694 is automatically set according to L, M, F, N′)
- CF is the control word count of a single converter within a single frame (CW9694 value = 0) Figure 24 shows a simplified block diagram of the CW9694 JESD204B link.

The CW9694 is configured by default to use four converters and four data paths. The data output of converter A and converter B is to SERDOUTAB0± and SERDOUTAB1±, and the data output of converter C and converter D is to SERDOUTCD0± and SERDOUTCD1±. CW9694 supports other matching Set, such as combining the outputs of two converters into a single channel, or changing the mapping of the digital output path. These modes can be set by the Quick Configuration Register in the SPI Register Map and provide additional customization options.

In CW9694, by default, the 14-bit data from each converter is divided into two octets (the data bits are 8 bits). The first 8-bit word pack Including bit 13 (MSB) to bit 6. The second eight contains 5th to 0th bit (LSB) and 2 end bits. The end bit can be configured as a 0 or a sequence of pseudo-random numbers, and the end bit can also be replaced with a control bit indicating an overspan, SYSREF± or fast detection output.

The generated two 8-bit words can be scrambled. Scrambling is optional, but it is recommended to use it to avoid spectrum spikes when transmitting similar digital data patterns. The scrambler uses a self-synchronous, polynomial-based algorithm defined by equation 1 + x14 + x15. The descrambler in the receiver is a self-synchronized version of the scrambler polynomial.

The two 8-bit bytes are then encoded using an 8B/10B encoder. The working principle of the 8B/10B encoder is to encode 8 bits of data (1 8 bit word) into a 10-bit symbol. Figure 25 shows how to get 14-digit numbers from the ADC How to add end bits, how to scramble two 8-bit words, and how to 8The bit code is two 10-bit symbols.

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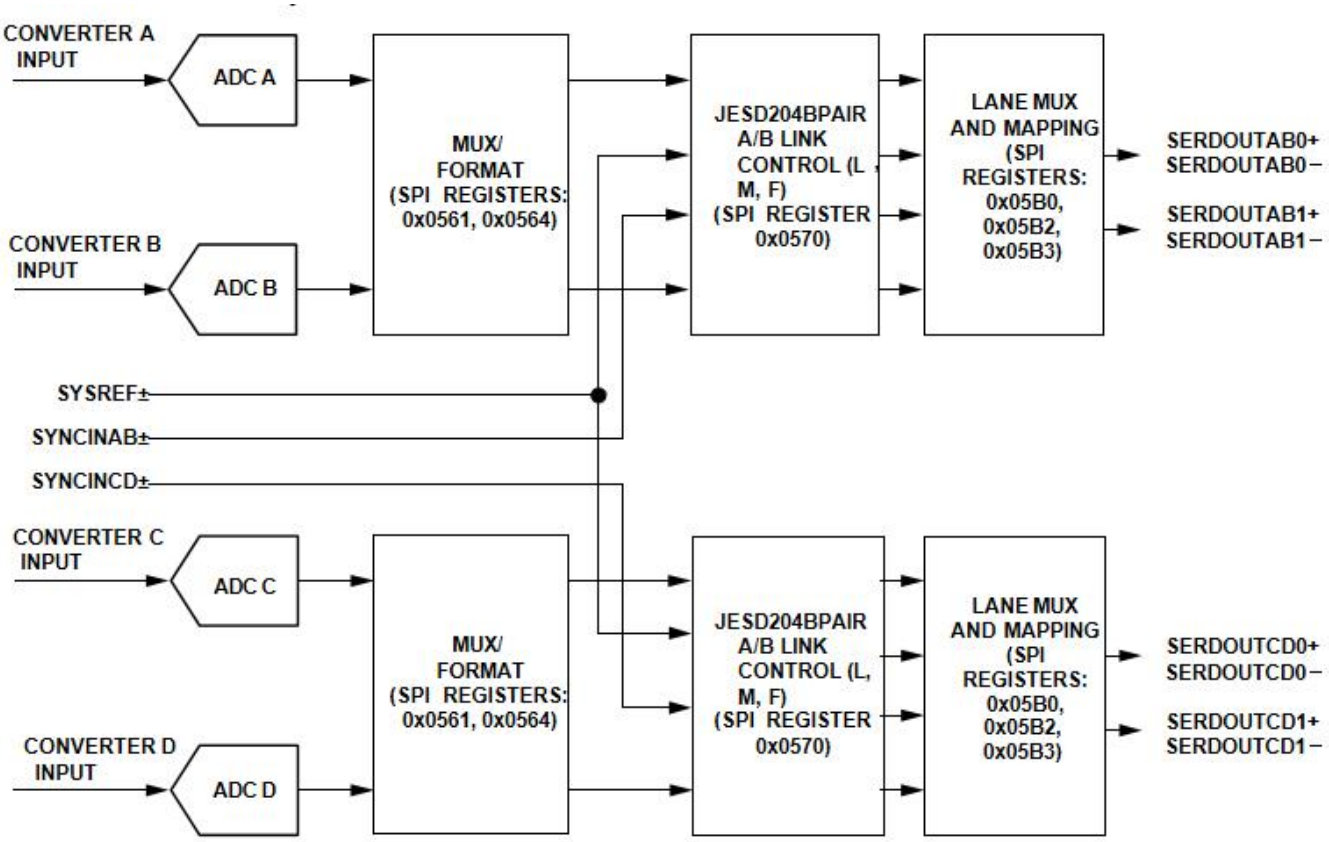

Figure 24 Simplified Block Diagram of the Transmit Link in Full Bandwidth Mode (0x200=0x00)

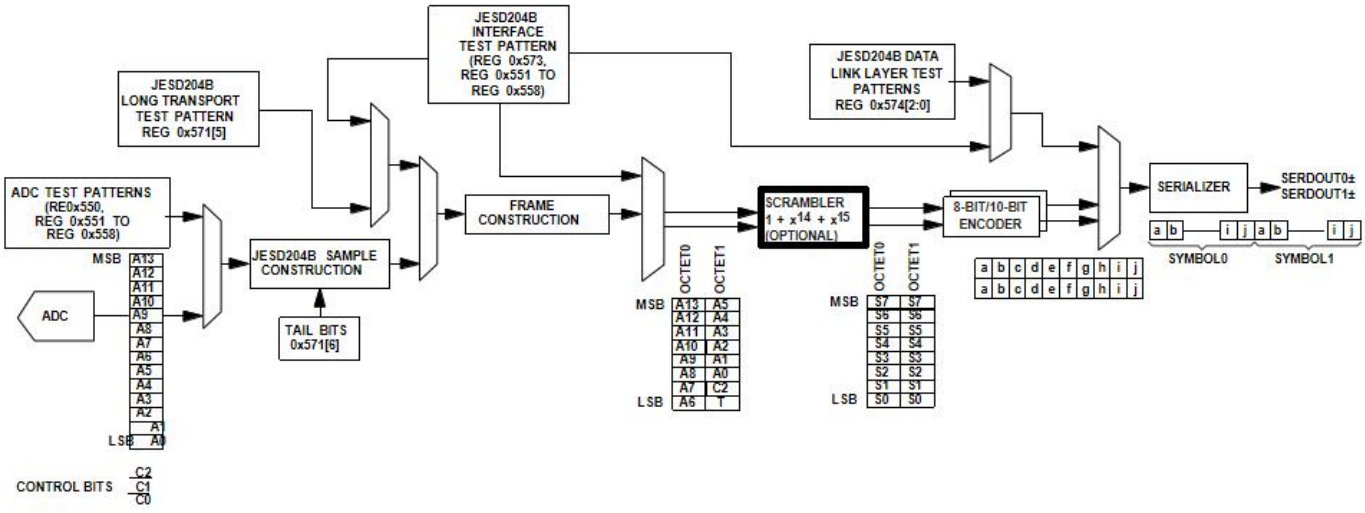

Figure 25 ADC Output Data Path for Data Frame Transmission

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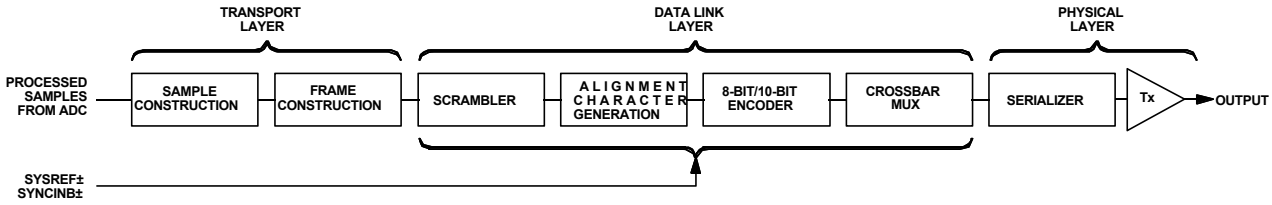

Figure 26 Data flow

14.3 Functional Overview

Figure 26 shows the JESD204B hardware data flow from sample input to physical output. Based on the OSI (Open Source Initiative) model, which is widely used to describe the abstraction layers of communication systems, the processing can be divided into multiple layers: transport layer, data link layer, and physical layer (serializer and output driver).

14.3.1 Transport Layer

The transport layer is responsible for packing the data (consisting of samples and optional control bits) into JESD204B frames mapped as 8-bit words. These 8-bit words are sent to the data link layer. Transport layer matching is controlled by the rules followed by the link parameters. Stop bits are added as needed to fill gaps. The number of stop bits in a sample (JESD204B word) can be determined using the following equation:

$$T = N' - N - CS$$

14.3.2 Data Link Layer

The data link layer is responsible for the low-level function of transmitting data over the link. This includes data scrambling, inserting control characters during the initial lane alignment sequence (ILAS) for frame and multiframe synchronization monitoring, and encoding 8-bit words into 10-bit symbols. The data link layer is also responsible for sending the ILAS, which contains the link configuration data used by the receiver to verify the transport layer settings.

14.3.3 Physical Layer

The physical layer consists of high-speed circuits clocked at the serial clock rate. In this layer, parallel data is converted into 1, 2, or 4 lanes of high-speed differential serial data.

14.4 JESD204B Link Establishment

The CW9694 JESD204B transmitter (Tx) interface works in subclass 0 or subclass 1 defined in the JEDEC standard JESD204B (July 2011 Specification). The link establishment process is divided into the following steps: code group synchronization, initial channel alignment sequence, user data and error correction.

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14.4.1 Code Group Synchronization (CGS)

CGS is the process by which the JESD204B receiver finds the boundary between 10-bit symbols in the data stream. During the CGS phase, the JESD204B transfer module transmits /K28.5/character. The receiver must use clock and data recovery (CDR) technology to locate /K28.5/chars in its input data stream.

The receiver sets the SYNCINB± pin of CW9694 low to issue a synchronization request. Then JESD204B Tx starts sending /K/ characters. Once the receiver has been synchronized, it waits for at least four consecutive /K/ symbols to be correctly received and then disconnected Assert SYNCINB±AB and SYNCINB±CD. CW9694 Next The next local multi-frame clock (LMFC) boundary sends an ILAS.

For more information on the code group synchronization phase, see the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB±AB and SYNCINB±CD pin operation can also be operated by SPI control. By default, the SYNCINB±AB and SYNCINB±CD signals are defaulted to a differential DC-coupled LVDS signal, but can also be single-ended. have For more information on configuring the SYNCINB±AB and SYNCINB±CD pin operations, see Register 0x572.

14.4.2 Initial Channel Alignment Sequence (ILAS)

The ILAS phase begins after the CGS phase with the next LMFC boundary after SYNCINB±AB and SYNCINB±CD assertions. ILAS consists of four multi-frames, starting with the /R/character marker and ending with the /A/character marker. ILAS sends a /R/ character first, followed by a multi-frame 0 to 255 ramp data. The link configuration data is sent from the third character on the second multiframe. The second character is a /Q/ character that confirms the link configuration data. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 27. These four types of multi-frames include:

- Multi-frame 1, starting with /R/character (/K28.0/) and ending with /A/character (/K28.3/).
- Multi-frame 2, starting with /R/ character, followed by a /Q/ character (/K28.4/),

Then there are 14 8-bit words of link configuration parameters (see Table 20),

End with a /A/ character. Many parameter values are represented by -1.

- Multi-frame 3, starting with /R/character (/K28.0/) and ending with /A/character (/K28.3/).
- Multi-frame 4, starting with /R/character (/K28.0/) and ending with /A/character (/K28.3/).

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14.4.3 User data and error detection

User data (ADC sample) is sent after the initial channel alignment sequence is completed. During user data transmission, a mechanism called character replacement is used to monitor frame clocks and multi-frame clock alignment. When the data meets a specific condition, the mechanism uses /F/ or/A/Alignment character replaces the last octet of a frame or multiple frames. These conditions are different for unscrambled and scrambled data. By default, scrambling is enabled, but can be disabled via SPI.

For scrambled data, any 0xFC character at the end of the frame is replaced by /F/.Any 0x7C character at the end of a multi-frame is replaced by /A/. The JESD204B receiver (Rx) checks the /F/ and /A/ characters in the received data stream and verifies that they only appear in the expected location. If an unexpected /F/ or /A/ character is found, the receiver uses

Dynamically adjust to handle this situation or assert the SYNCINB± signal over four frames to initiate resynchronization. For unscrambled data, if the last octet word of two consecutive frames is equal, if the second octet word is at the end of the frame, it is replaced by the /F/ symbol, and if it is at the end of multiple frames, it is replaced by the /A/ symbol.

SPI can be used to modify the insertion of alignment characters. By default, frame alignment

The character insertion function (FACI) is enabled. For more information about link control, see Register 0x571 in the Register Mapping section.

14.4.4 8B/10B Encoder

The 8B/10B encoder converts 8-bit words into 10-bit symbols and converts them if needed.

Control characters are inserted into the data stream. The control characters used in JESD204B are shown in Table 20 Shown. 8B/10B encoding by using the same number of 1s and 0s in multiple symbols to ensure that the signal reaches DC balance.

The 8B/10B interface has control operation. These operations include bypass and Reversal. These options are used as a troubleshooting tool for Digital Front-End (DFE) verification. For information on configuring the 8B/10B encoder, see Register 0x572[2:1] in the Register Map section.

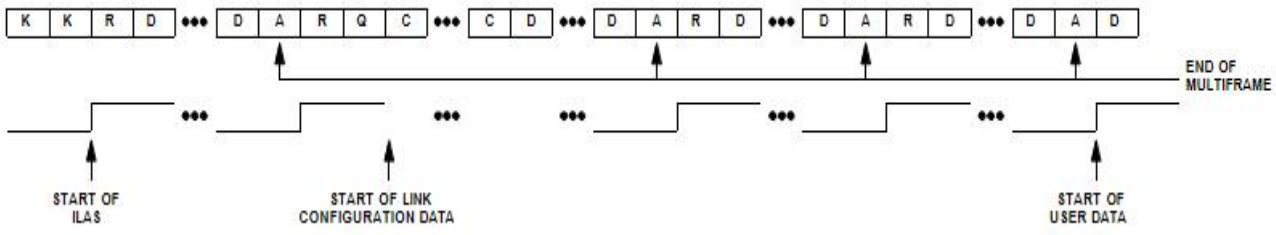

Figure 27 Initial channel alignment sequence

Table 20 CW9694 control characters used by JESD204B

abbreviation	Control symbols	8-bit value	10-bit value, RD[1] = -1	10-bit value, RD[1] = +1	illustrate
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Multi-frame start
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Channel Alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Link configuration data starts
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame Alignment

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[1] RD stands for the difference in running

14.5 Physical layer (driver) output

14.5.1 Digital output, timing and control

CW9694 Physical layer by JEDEC standard JESD204B (2011 7) the drive composition specified in the month. The default power-on is a differential digital output. The driver uses a dynamic internal termination resistor of 100 Ω to reduce reflected interference.

Place a 100Ω differential termination resistor at each receiver input to generate a nominal 300 mV p-p swing at the receiver (see Figure 28). Or it can To use a single-ended 50Ω terminal. When using a single-ended terminal, the terminal voltage is DRVDD1/2.

The CW9694 digital output can be interfaced with custom ASIC and FPGA receivers, enabling excellent switching performance in high noise environments. Recommended User List . It is recommended to use a single point-to-point network topology and place a single 100 Ω differential termination resistor as close as possible to the receiver input. The common mode of the digital output is automatically biased to half of the DRVDD1 power supply (0.76V). DC couple the output to the receiver as shown in Figure 29.If there is no remote receiver termination resistor, or the differential routing is poor, timing errors may occur. To avoid such timing errors, it is recommended that the trace length is less than 6 inches, and the differential output traces should be as close to each other and have equal lengths as possible.

Figures 30 and 31 show examples of the digital output data eye diagram and jitter histogram for an CW9694 channel operating at 13.1 Gbps. By default, the output data is in two's complement format. For information on changing the output data format, refer to the Register Map section (Register 0x0561).

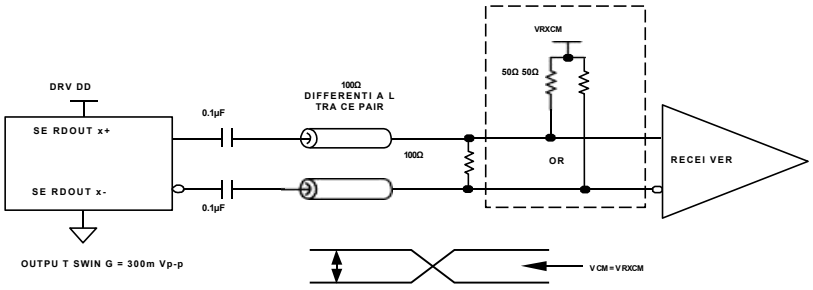

Figure 28 Example of AC-coupled digital output terminal

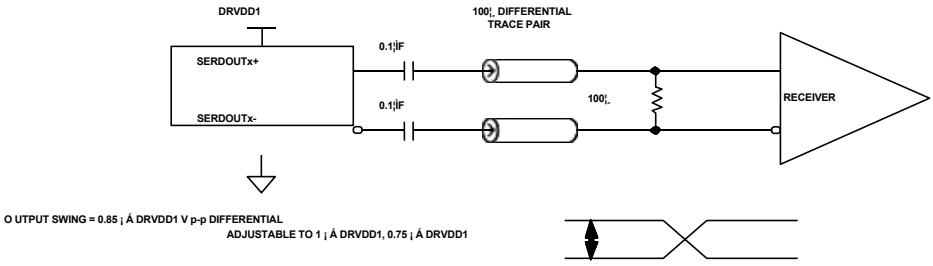

Figure 29 Example of DC-coupled digital output termination

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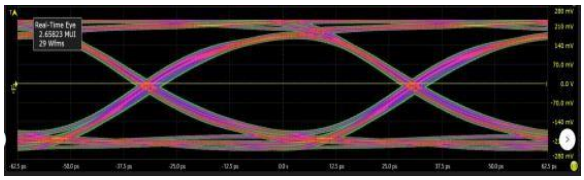

Figure 30 Digital output eye diagram (external termination at 13.1Gbps 100Ω)

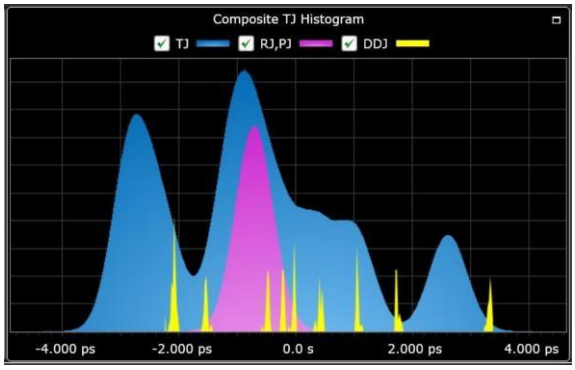

Figure 31 Digital output jitter histogram (external termination at 13.1Gbps)

14.5.2 De-heavy

De-emphasis can satisfy the receiving eye mask if the interconnect insertion loss does not comply with the JESD204B specification. The de-emphasis function is used only if the receiver cannot recover the clock due to excessive insertion loss. Generally, this feature is disabled to save power. In addition, enabling and setting too high de-emphasis values on a short link may cause the receiver eye diagram to fail. Please use the de-emphasis setting with caution as it increases electromagnetic interference (EMI). Please refer to the Register Mapping Table section (Registers 0x05C4 ~ 0x05C6 in Table 35) for more details.

14.5.3 Phase Locking Loop

A phase-locked loop (PLL) is used to generate a serial clock, which operates at the JESD204B channel rate. The locked state of the PLL can be viewed in the PLL locked status bit (bit 7 of register 0x056F). This read-only bit tells the user whether PLL lock is implemented in a specific setting.

JESD204B channel rate control, the Bits[7:4] of register 0x056E must be set to correspond to the channel rate. Table 21 shows the use register 0x056E settings

Set the channel rate supported by the CW9694.

Table 21 CW9694 Register 0x56E Supported Channel Rate

Value	Lane Rate
0x00	Lane rate = 6.75 Gbps to 13.5
0x10	Lane rate = 3.375 Gbps to 6.75 Gbps (default)
0x30	Lane rate = 13.5 Gbps to 16 Gbps
0x50	Lane rate = 1.6875 Gbps to 3.375 Gbps

14.6 CW9694 digital interface settings

In order to ensure that the CW9694 works properly on startup, some SPI writes are required to initialize the link. Additionally, these registers must be written to every time the ADC is reset. Any of the following resets guarantees the initialization routine of the digital interface:

- A soft reset of the data path is achieved by setting register 0x0001 = 0x02.
- The JESD204B link is powered up and down by setting register 0x0571, bit 0 = 0x1, then 0x0.

- Hard reset, just like power on.
- Power up using PDWN pin.
- Power up via Register 0x0002, Bits[1:0] using SPI.
- SPI soft reset is done by setting register 0x0000 = 0x81.

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The CW9694 has a JESD204B link. serial output
(SERDOUTAB0±/ SERDOUTAB1± and SERDOUTCD0±/
SERDOUTCD1±) is considered part of a JESD204B link. The basic parameters that determine the link settings are

- Number of data paths per link (L)
- Number of converters per link (M)
- Number of 8-bit bytes per frame (F)

If the internal DDC is used for on-chip digital processing, then M represents the number of virtual converters.
In the CW9694, by default, 14 bits from each converter
The converter word is divided into 2 octets (8 bits of data). Bit 13 (MSB)
Position 6 is in the 1st eight. The second octet contains bits 5 to 0
(LSB) and two end bits. The end bit can be configured as a sequence of zeros or pseudo-random numbers, or can be replaced with a control bit indicating overrange, SYSREF± or fast detection output. The control bits are populated and inserted MSB first, enabling CS = 1 activates control bit 2,
Enable CS = 2 activates control bit 2 and control bit 1, enable CS = 3 activate control bit 2, control bit 1 and control bit 0.

The maximum lane rate allowed by the CW9694 is 16Gbps. The relationship between channel rate and JESD204B parameters is as follows:

$$Lane\ Rate = \frac{M \times N' \times (\frac{10}{8}) \times f_{OUT}}{L}$$

$$f_{OUT} = \frac{f_{ADC\_CLOCK}}{Decimation\ Ratio}$$

The decimation ratio (DCM) is a parameter written to register 0x0201. The following steps can be used to configure the output:

1. Power down the link.
2. Select the JESD204B link configuration options.
3. Configure detailed options.
4. Set the output lane mapping (optional).
5. Set other driver configuration options (optional).
6. Power up the link.
7. Initialize the JESD204B link.

Register 0x056E must be written based on the calculated Lane Rate. Refer to the Phase-Locked Loop (PLL) section for more details.

Table 23 and Table 24 show the supported JESD204B output configurations for N′ = 16, and N′ = 8 for a given number of virtual converters. Care should be taken to ensure that the serial lane rate for a given configuration is within the supported range of 1.6875 Gbps to 16 Gbps.

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14.7 Mapping of JESD204B Tx Converters

To support different chip operation modes, the CW9694 design treats each sample stream (real or I/Q) as coming from a different virtual converter. I/Q samples are always mapped in pairs, with I samples mapped to the first virtual converter and Q samples mapped to the second virtual converter. With this transport layer mapping, the number of virtual converters is the same whether a single real converter is used with a digital downconversion block that produces I/Q outputs, or analog downconversion is used with two real converters that produce I/Q outputs.

Figure 32 shows a block diagram of the two scenarios described for the I/Q transport layer mapping.

The JESD204B Tx block of the CW9694 supports up to four DDC blocks. Each DDC block outputs two samples (I/Q) of complex data components (real + imaginary), or one sample stream of real (I) data. The JESD204B interface can be configured to use up to eight virtual converters, depending on the DDC configuration. Figure 33 shows the virtual converters and their relationship to the DDC outputs when complex outputs are used. Table 22 shows the virtual converter mapping for each chip application mode when lane swapping is disabled.

Table 22 Virtual Converter Mapping

Number of Virtual Converters Supported	Chip Application Mode **(Register 0x0200, Bits [3:0])**	Ignore Q **(Register 0x0200, Bit 5)**	Virtual Converter Mapping			
			1	2	3	4
1 to 2	Full Bandwidth Mode (0x0)	Real or Complex (0x0)	A/C Sampling	B/D Sampling	Unused	Unused
1	Single DDC Mode (0x1)	Real (I Only) (0x1)	DDC0 I Sample	Unused	Unused	Unused
2	Single DDC Mode (0x1)	Composite (I/Q) (0x0)	DDC0 I Sample	DDC0 Q Sample	Unused	Unused
2	Dual DDC Mode (0x2)	Real (I Only) (0x1)	DDC0 I Sample	DDC1 I Sample	Unused	Unused
4	Dual DDC Mode (0x2)	Composite (I/Q) (0x0)	DDC0 I Sample	DDC0 Q Sample	DDC1 I Sample	DDC1 Q Sample

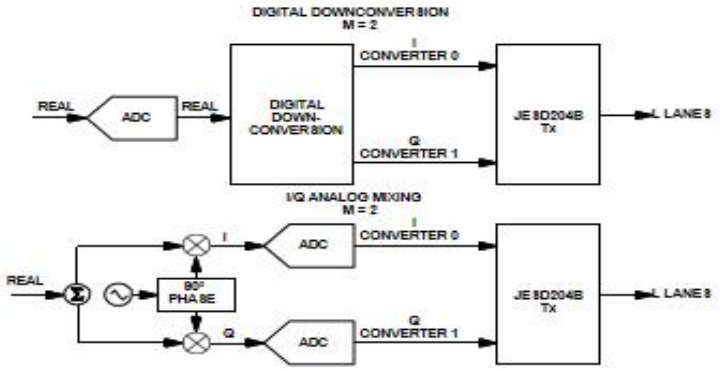

Figure 32 I/Q Transport Layer Mapping

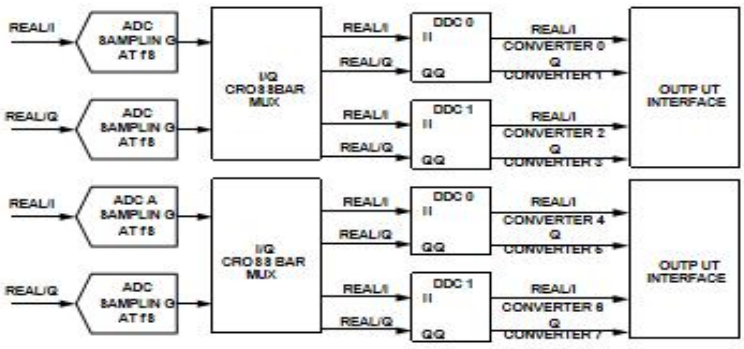

Figure 33 DDC and Virtual Converter Mapping

Table 23 N′ = 161 JESD204B output configuration

Number of virtual converters supported (same as M value)	JESD204B Quick Configuration (0x0570)	JESD204B Serial Line Rate 1	JESD204B Transport Layer Settings 2								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x01	20 ×f_{OUT}	1	1	2	1	0	8 to16	16	0 to3	Only supported Valid K value divisible by 4
	0x40	10 ×f_{OUT}	2	1	1	1	1	8 to16	16	0 to3	
	0x41	10 ×f_{OUT}	2	1	2	2	0	8 to16	16	0 to3	
2	0x0A	40 × f_{OUT}	1	2	4	1	0	8 to16	16	0 to3	
	0x49	20 ×f_{OUT}	2	2	2	1	0	8 to16	16	0 to3	
4	0x13	80 ×f_{OUT}	1	4	8	1	0	8 to16	16	0 to3	
	0x52	40 × f_{OUT}	2	4	4	1	0	8 to16	16	0 to3	

[1] fOUT=Output sampling rate=ADC sampling rate/chip extraction ratio. JESD204B serial line rate must be ≥1687.5Mbps and less than ≤15000Mbps; when the serial line rate is ≤15Gbps and ≥13.5Gbps, set bit [7:4] of 0x056E to 0x3. When the serial line rate is <13.5Gbps and ≥6.75Gbps, set bit [7:4] of 0x056E to 0x0. When the serial line rate is <6.75Gbps and ≥3.375Gbps, set bit [7:4] of 0x056E to 0x1. When the serial line rate is <3.375Gbps and ≥1678.5Mbps, set bit [7:4] of 0x056E to 0x5.

[2] JESD204B Transport layer description refers to the "Digital Interface" section.

[3] For F=1, K=20, 24, 28, and 32. For F=2, K=12, 16, 20, 24, 28, and 32. For F=4, K=8, 12, 16, 20, 24, 28, and 32. For F=8 and F=16, K=4, 8, 12, 16, 20, 24, 28, and 32.

Table 24 JESD204B output configuration when N′ = 8[1]

Number of virtual converters supported (Same as M value)	JESD204B Quick configuration (0x0570)	JESD204B Serial Line Rate 1	JESD204B Transport Layer Settings 2								
			L	M	F	S	HD	N	N′	CS	K[3]
1	0x00	10×f_{OUT}	1	1	1	1	0	7 to 8	8	0 to1	Only supports Valid K values divisible by 4
	0x01	10×f_{OUT}	2	1	2	2	0	7 to 8	8	0 to1	
	0x40	5×f_{OUT}	2	1	1	2	0	7 to 8	8	0 to1	
	0x41	5×f_{OUT}	2	1	2	4	0	7 to 8	8	0 to1	
	0x42	5×f_{OUT}	1	1	4	8	0	7 to 8	8	0 to1	
2	0x09	20×f_{OUT}	1	2	2	1	0	7 to 8	8	0 to1	
	0x48	10×f_{OUT}	2	2	1	1	0	7 to 8	8	0 to1	
	0x49	10×f_{OUT}	2	2	2	2	0	7 to 8	8	0 to1	

[1] fOUT=Output sampling rate=ADC sampling rate/chip decimation ratio. JESD204B serial line rate must be ≥1687.5Mbps and less than ≤15000Mbps; when the serial line rate is ≤15Gbps and ≥13.5Gbps, set bits [7:4] of 0x056E to 0x3. When the serial line rate is <13.5Gbps and ≥6.75Gbps, set bits [7:4] of 0x056E to 0x0. When the serial line rate is <6.75Gbps and ≥3.375Gbps, set bits [7:4] of 0x056E to 0x1. When the serial line rate is <3.375Gbps and ≥1678.5Mbps, set bits [7:4] of 0x056E to 0x5.

[2] See the “Digital Interface” section for JESD204B transport layer description.

[3] For F=1, K=20, 24, 28 and 32. For F=2, K=12, 16, 20, 24, 28 and 32. For F=4, K=8, 12, 16, 20, 24, 28 and 32. For F=8 and F=16, K=4, 8, 12, 16, 20, 24, 28 and 32.

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14.7.1 Example Setup 1: Full Bandwidth Mode

The configuration of CW9694 is shown in Figure 34, and the configuration is as follows:

- Four 14-bit converters, sampling rate 500MSPS.
- Full bandwidth application layer mode.
- No extraction.

The output configuration for JESD204B is as follows:

- Four virtual converters are required (see Table 23).
- Output sampling rate (f_{OUT})=500/1=500MSPS.
- The output configurations supported by JESD204B are as follows (see Table 23):
- N′=16 bits.
- N=16 bits.
- L=2, M=2, F=2 (quick configuration 0x48)
- CS=0 to 2.
- K = 32.
- Output serial lane rate: 10Gbps per lane.

14.7.2 Example Setup 2: ADC with DDC Option (Two ADCs plus

Two DDCs) This example shows the flexibility of the CW9694 in digital and channel configurations, with a sample rate of 500 MSPS, but the outputs are all combined in one or two lanes depending on the input/output speed capabilities of the receiving device.

The CW9694 setup is shown in Figure 35 and is configured as follows:

- Two 14-bit converters with a sample rate of 500MSPS.
- Two DDCs in application layer mode with complex outputs (I/Q).
- Chip decimation ratio = 4.
- DDC decimation ratio = 4 (see Table 23). The output configuration for JESD204B is as follows:
- Four virtual converters are required (see Table 23).
- Output sample rate (f_{OUT}) = 500MSPS/4 = 125MSPS.
- N′ = 16 bits.
- N = 14 bits.
- L = 1, M = 4, F = 8 (Quick Configuration = 0x13).
- CS = 0 to 1.
- K = 32.
- Output Serial Lane Rate = 10Gbps/Lane (L = 1), 5Gbps/Lane (L = 2)

For L = 1, control register 0x056E[7:4] is set to 0x1. For L = 2, control register 0x056E[7:4] is set to 0x5.

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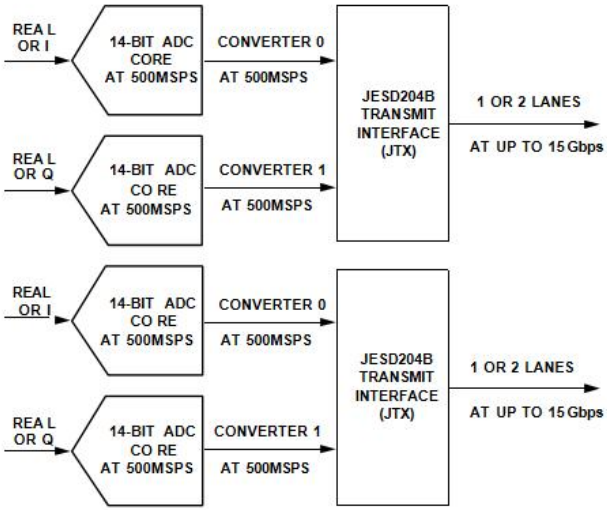

Figure 34 Full bandwidth mode

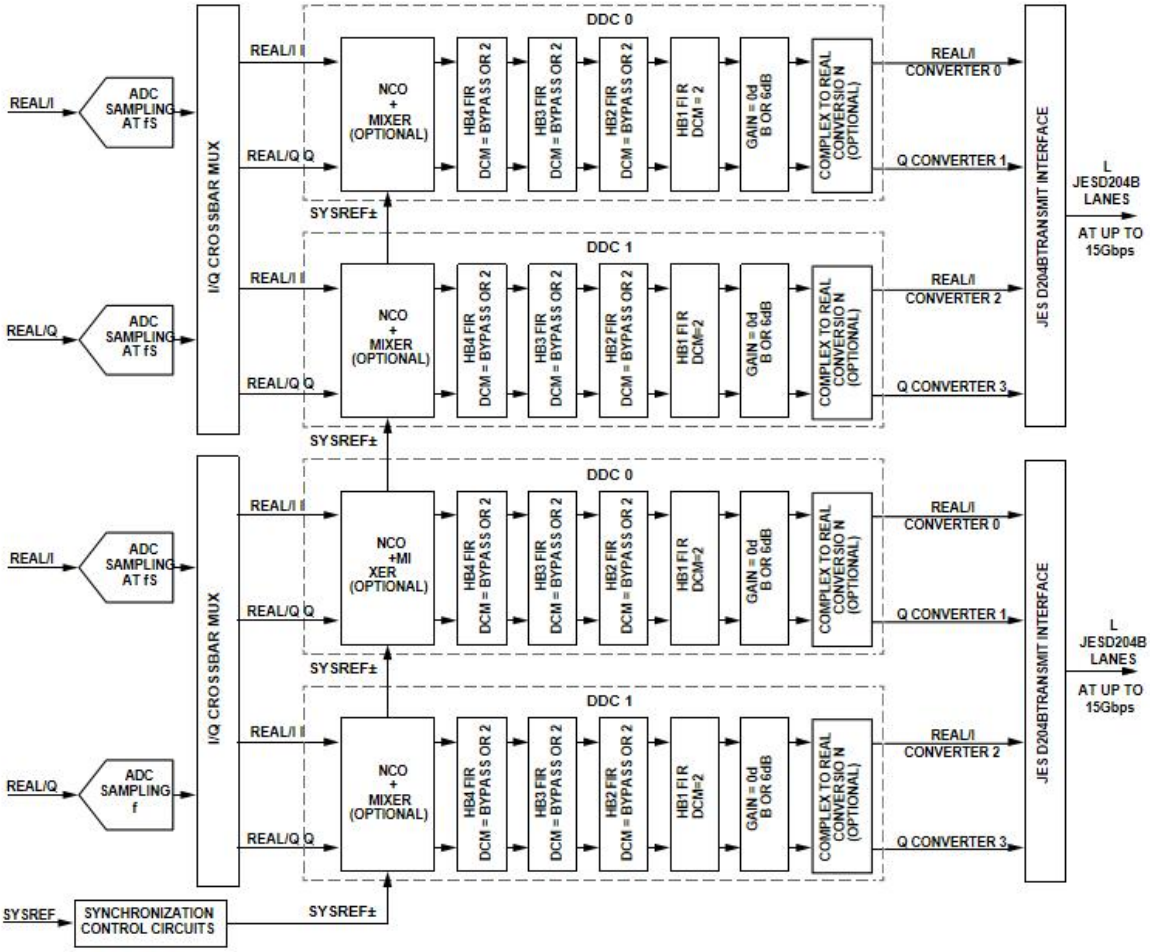

Figure 35 Two ADC + Two DDC Mode (L = 1, M = 4, F = 8, S = 1)

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15.0 Delay Characteristics

15.1 Total End-to-End Delay

The total delay in the CW9694 depends on the chip application mode and the JESD204B configuration. For any given combination of these parameters, the delay is deterministic, however, the value of this deterministic delay must be calculated as described in the Example Delay Calculation section.

Table 25 shows the combined latency through the ADC and DSP for the different chip application modes supported by the CW9694. Table 26 shows the latency through the JESD204B block for each application mode based on the M/L ratio. For Table 25 and Table 26, the latency is typical and is in units of encode clock. The latency through the JESD204B block does not depend on the output data type (real or complex). Therefore, the data type is not included in Table 26.

To determine the total latency, select the appropriate ADC+DSP latency from Table 25 and add it to Table 26 for the latency calculation examples:

Example 1:

In this example, the ADC application mode is full bandwidth with the following conditions:

Real output

- L=4, M=2, F=1, S=1 (JESD204 mode)
- M/L = 0.5
- Latency = 31+25 = 56 encode clocks

Example 2:

In this example, the ADC application mode is 4x decimate, DCM4 with the following conditions:

- Complex output
- L=4, M=2, F=1, S=1 (JESD204 mode)
- M/L = 0.5

Latency = 162 + 88 = 250 encode clocks

15.2 LMFC Reference Latency

FPGA vendors may require the end user to know the LMFC reference latency in order to make appropriate deterministic latency adjustments. If these parameters are required, the delay values in Table 25 and Table 26 can be used to simulate the input to LMFC delay values and the LMFC to data output delay values.

Table 25 Delay through ADC+DSP block (unit: number of sampling clocks)

Chip application mode [1]	Enable filter	ADC and DSP delay
Full bandwidth	Not applicable	31
DCM1 (real) DCM2 (complex)	HB1	94
DCM2 (real) DCM4 (complex)	HB2 +HB1	162
DCM4 (real) DCM8 (complex)	HB3 +HB2 +HB1	292
DCM8 (real) DCM16 (complex)	HB4+ HB3+ HB2 +HB1	548

[1] DCM_X represents the decimation ratio

Table 26 Delay through JESD204B block (unit: number of sampling clocks)

Chip application mode	M/L ratio [2]				
	0.5	1	2	4	8
Full bandwidth	25	14	7	4	3
DCM1	25	14	7	N/A	N/A
DCM2	46	27	14	7	N/A
DCM4	88	50	27	14	7
DCM8	172	96	50	27	14
DCM16	339	188	96	50	27

The [2] M/L ratio is the number of converters divided by the number of lanes used for configuration.

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15.3 Deterministic Latency

Both ends of a JESD204B link contain various clock domains distributed throughout each system. Data traversal from one clock domain to another results in ambiguous delays in a JESD204B link. These ambiguities result in non-repeatable delays on the link from one power cycle or link reset to the next. Section 6 of the JESD204B specification discusses deterministic latency for mechanisms defined as Subclass 1 and Subclass 2. The CW9694 supports JESD204B Subclass 0 and Subclass 1 operation. Register 0x0590, Bits[7:5] sets the subclass mode for the CW9694, which defaults to Subclass 1 mode of operation (Register 0x590, Bits[7:5] = 001). If deterministic latency is not a system requirement, it is recommended to use Subclass 0 operation, which does not require the system to provide a SYSREF± signal. Even in Subclass 0 mode, a SYSREF± signal may be required in applications where multiple CW9694 devices need to be synchronized (see the Timestamp Mode section for more information).

15.3.1 Subclass 0 Operation

If multichip synchronization is not required when operating in Subclass 0 mode (Register 0x590, Bits [7:5] = 000), the SYSREF± input can be left disconnected. In this mode, the relationship of the JESD204B clocks between the JESD204B transmitter and receiver is arbitrary but does not affect the receiver's ability to capture and align lanes in the link.

15.3.2 Subclass 1 Operation

The JESD204B protocol organizes data samples into octets, frames, and composite frames as described in the Transport Layer section. The LMFC is synchronous to the start of these composite frames. In subclass 1 operation, the SYSREF± signal is used to synchronize the LMFC of each device in a link or multiple links (in CW9694, SYSREF± also synchronizes the internal sample distributor), see Figure 36. The JESD204B receiver uses composite frame boundaries and buffering to achieve consistent latency across lanes (even across multiple devices) and to achieve fixed latency between power cycle and link reset conditions.

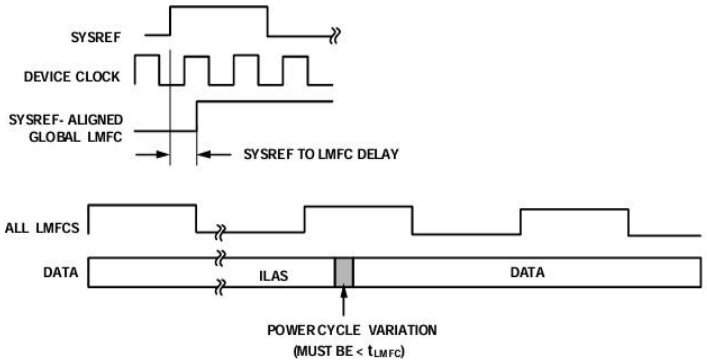

Figure 36 SYSREF and LMFC

15.3.3 Deterministic delay

Implementing deterministic latency in JESD204B subclass 1 system requires several key factors to be identified.

- The deviation of the SYSREF± signal distribution within the system must be less than the uncertainty required by the system.
- Each device in the system must meet the SYSREF± setup and hold time requirements.
- Total delay variations for all channels, links and devices must be ≤1 LMFC (tLMFC) cycle (see Figure 36).

This total delay includes variable delays and changes in the system from channel to channel, link to link and device to device.

15.3.4 Setting the deterministic delay register

JESD204B in the logical device receives buffer buffers data starting from the LMFC boundary. If the total link delay in the system is close to an integer multiple of the LMFC cycle, the data arrival time at the reception buffer may overlap with the LMFC boundary from one power cycle to the next. To ensure the determination delay in this case, phase adjustment of the LMFC must be performed at the transmitter or receiver

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all. Typically, the receiver's LMFC is adjusted to fit the receiver buffer. In the CW9694, the JTX LMFC offset register (Register 0x0578, bit [4:0]) can be adjusted. This register delays LMFC in frame clock increments, depending on the F parameter (number of octets per channel per frame). For F=1, every four settings (0, 4, 8,…) produce a frame clock offset. For F=2, a frame clock offset will be generated for every other setting (0, 2, 4,…). For F's

All other values, each setting will cause a frame clock offset. Figure 37 shows that when the link delay is close to the LMFC boundary, the local LMFC of the CW9694 can be delayed to delay the time when the data arrives at the receiver. Figure 38 shows how the receiver's LMFC is delayed to accommodate the receive buffer timing. For more information on making this adjustment, see the applicable JESD204B Receiver User Guide.

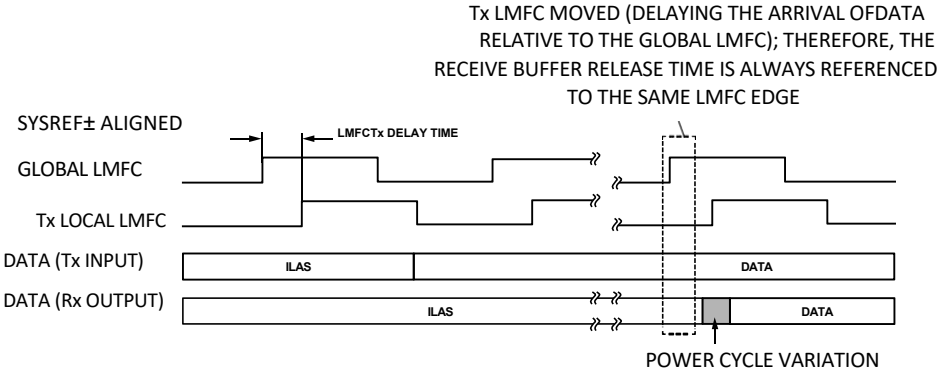

Figure 37 Adjusting JESD204B Tx LMFC in CW9694

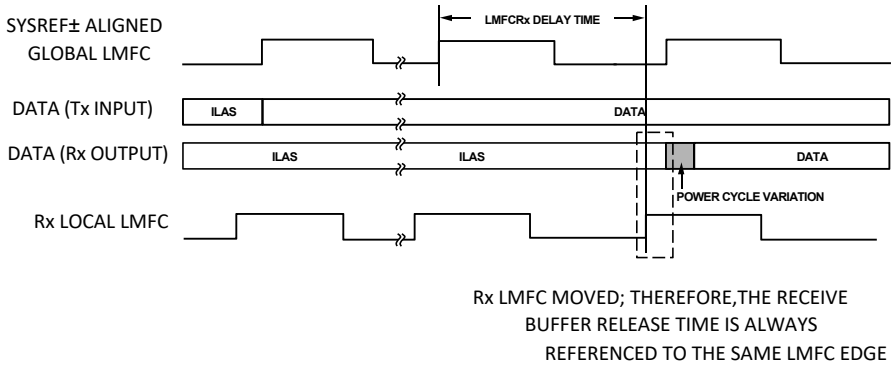

Figure 38 Adjusting JESD204B Rx LMFC in CW9694

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16.0 Multi-chip synchronization

The flowchart shown in Figure 39 describes the internal mechanism of multi-chip synchronization in the CW9694. There are two ways to achieve multi-chip synchronization, which is determined by the chip synchronization mode bit (register 0x1FF, bit 0). Each method involves different applications of SYSREF± signal.

16.1 Normal mode

The default value of the chip synchronization mode bit is 0, indicating that CW9694 is in normal operation.

Mode of chip synchronization.

The JESD204B standard specifies the use of SYSREF± to provide deterministic delays in a single link. With the same concept, multi-chip synchronization can also be provided when applied to systems with multiple converters and logic devices. In Figure 39, this synchronization mode is called the normal mode. Follow the process shown in the flowchart to ensure CW9694 is configured correctly. Please consult the Logic Device User Intellectual Property (IP) Guide to ensure that the JESD204B receiver configuration is correct.

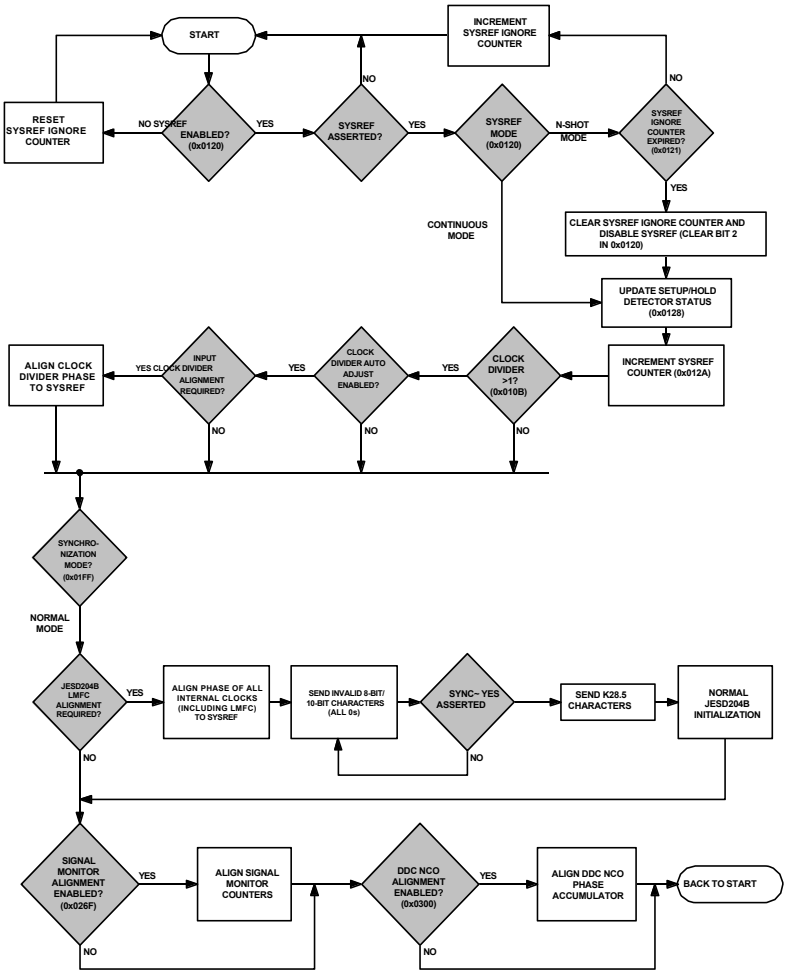

Figure 39 SYSREF± Capture Scenario and Multi-Chip Synchronization

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16.2 Timestamp mode

For CW9694 In full bandwidth operation mode, the SYSREF± input can also be used to timestamp the sample. Timestamps are another way that multiple channels and multiple devices can achieve synchronization. The timestamp mode is suitable when multiple devices are synchronized with one or more logical devices. Logical devices simply buffer data streams, identify timestamp samples, and align them.

When the Synchronization Mode bit (Register 0x01FF, bit 0) is set to 0x1, the timestamp mode is used for synchronization of multiple channels and/or devices. In this mode, SYSREF±Reset the sample allocator and JESD204B clock. When Sync Mode is set to 0x1, the clock does not reset; instead, the overlapping samples will be timestamped using the JESD204B control bit of that sample. To run in timestamp mode, the following additional settings are required:

- Continuous or N-shot SYSREF ±enabled (Register 0x0120, bits [2:1]
  The value is 1 or 2)
- At least one control bit must be enabled (register 0x58F, bit [7:6] has a value of 1, 2, or 3)
- Set the function of one of the control bits to SYSREF ± as shown below:

a) If control bit 0 is used, register 0x0559 bits [2:0] = 5
b) If control bit 1 is used, register 0x0559 bits [6:4] = 5
c) If control bit 2 is used, register 0x055A bit [2:0] = 5

Figure 40 shows how the input sample consistent with SYSREF± is performed interstamp and finally output from the ADC. In this example, there are two control bits, control bit 0 indicates which sample is consistent with SYSREF± rising edge. The channel delay is the same for each channel, and if desired, the SYSREF± timestamp delay register (Register 0x0123) can be used to adjust the time of the timestamped samples. No timestamp is supported in any operation mode that uses extraction.

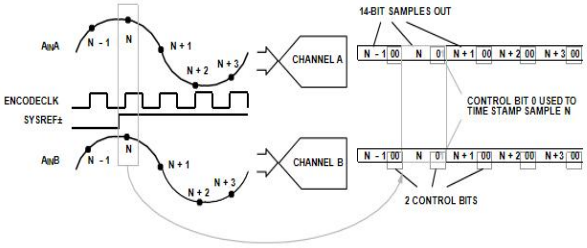

Figure 40 Time stamp CS=2 (Register 0x058F, bit [7:6]=2), control bit 0
is SYSREF±(Register 0x0559, bits [2:0]=5)

16.3 SYSREF±Input

The SYSREF± input signal is used as a high-precision system reference for deterministic delay and multi-chip synchronization.

CW9694 accepts single or periodic input signals. SYSREF±Mode Select bits (Register 0x0120, bits[2:1]) select the input signal type and when setting Activate the SYSREF± state machine. If in single pulse or N pulse mode (Register 0x0120, Bits[2:1] = 2), the SYSREF± mode selection bit is automatically cleared after the corresponding SYSREF± conversion is detected. The minimum pulse width must be two CLK±period widths. If clock divider (register 0x010B, Bits[2:0]) Set to a value other than 1 times the frequency division, multiply the minimum pulse width requirement by the frequency division

(For example, if you set the 8 frequency division, the minimum pulse width is 16 CLK±cycle). When using continuous SYSREF± signal (Register 0x0120, Bits[2:1] When = 1), the period of the SYSREF± signal must be an integer multiple of the LMFC. LMFC is derived using the following formula:

$$LMFC = ADC\ Clock/S \times K$$

in:

S is the JESD204B parameter, indicating the number of samples for each converter.

K is a JESD204B parameter, indicating the number of frames per multi-frame. In normal synchronization mode (register 0x01FF, Bits[1:0] = 0), the input clock divider, DDC, signal monitor module and JESD204B link are all used

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Synchronization is performed with the SYSREF± input, which can also be used to timestamp ADC samples, which can provide a synchronization mechanism to synchronize multiple CW9694 devices in the system. For the highest timing accuracy, SYSREF± must meet the establishment and hold requirements relative to the CLK± input. There are several features in the CW9694 that ensure that these requirements are met (see the SYSREF±Control Features section).

16.3.1 SYSREF± control characteristics

SYSREF± is used with the input clock (CLK±) as part of the source synchronization timing interface and requires a set-up and hold timing requirements relative to the input clock to be -44.8ps and 64.4ps, respectively (see Figure 41). The CW9694 has a variety of features to meet these requirements. First, the SYSREF± sampling event can be defined as a synchronous low to high conversion or a synchronous high to low conversion. Second, the CW9694 allows the SYSREF± signal to be sampled using the rising or falling edge of the input clock. Figure 41, Figure 42, Figure 43, and Figure 44 show all four possible combinations. The third available SYSREF± correlation feature is the ability to ignore a programmable number (up to 16) SYSREF± event.

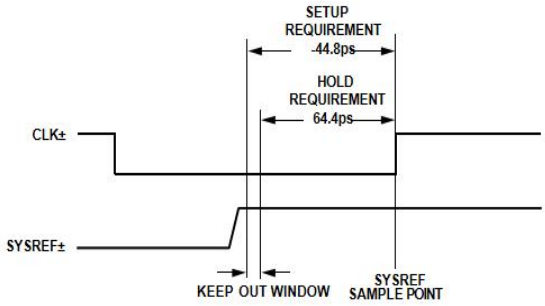

Figure 41 SYSREF±Setting and Hold Time Requirements;
SYSREF±Low to High Conversion
Uses Rising Edge Clock (Default)

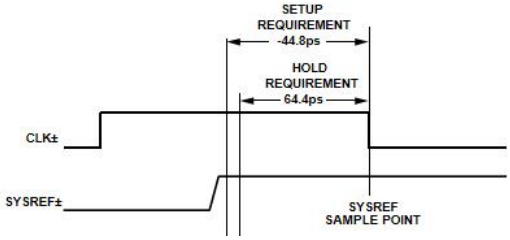

Figure 42 Low to high conversion of SYSREF± using clock falling edge capture
(0x0120, Bit 4=1'b0 and 0x0120, Bit 3=1'b1)

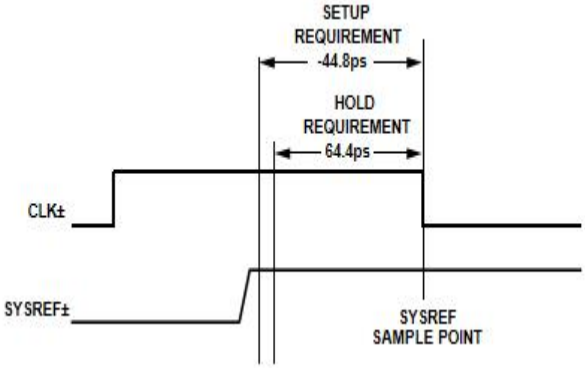

Figure 43 High to low conversion of SYSREF± is captured using rising edge of clock
(0x0120, Bit 4 = 1'b1 and 0x0120, Bit 3 = 1'b0)

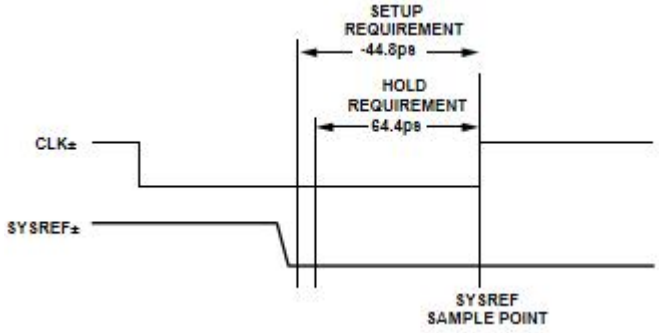

Figure 44 SYSREF±'s high to low conversion is captured using clock falling edge
(0x0120, Bit 4=1'b1 and 0x0120, Bit 3=1'b1)

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The SYSREF±ignore feature is enabled by setting the SYSREF± mode register (Register 0x0120, Bits[2:1]) to 2'b10, which is called N-shot mode. The CW9694 is able to ignore N SYSREF± events, which is very useful for processing periodic SYSREF± signals that require time to be established after startup. neglect SYSREF±, inaccurate SYSREF± triggering can be avoided until the clock in the system stabilizes. Figure 45 shows an example of the SYSREF±ignoring feature when three SYSREF± events are ignored.

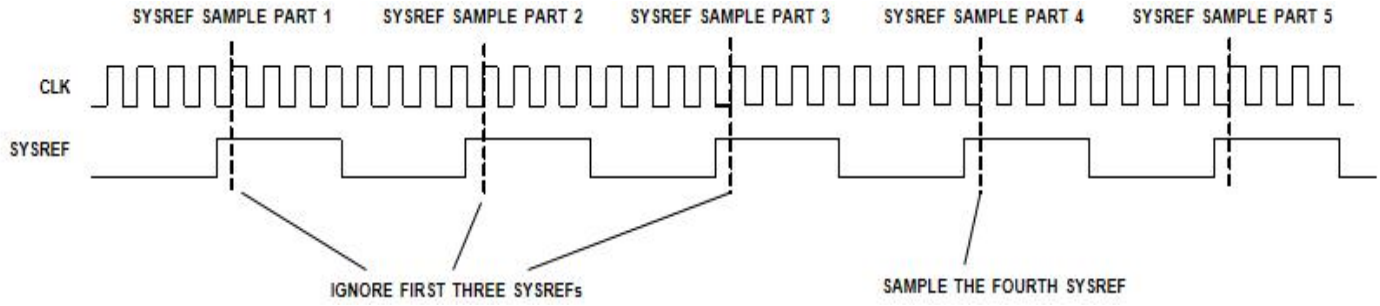

Figure 45 SYSREF±ignore example; SYSREF±ignore Count Bits (Register 0x0121Bits[3:0])=3

16.4 SYSREF±Create/Keep Window Monitor

To ensure effective SYSREF± signal capture, the CW9694 has a SYSREF± build/hold window monitor. This feature allows system designers to read the settling/hold margin on the interface through memory maps, thereby determining the location of the SYSREF± signal relative to the CLK± signal. Figure 46 and Figure 47 show the establishment and hold state values for different stages of SYSREF±. Create detector return

In the SYSREF± signal state before the CLK± edge, keep the detector returning the state of the SYSREF signal after the CLK± edge. Register 0x0128 stores the status of SYSREF± and lets the user know whether the SYSREF± signal is captured by the ADC. Table 27 describes the contents of register 0x0128 and the corresponding description.

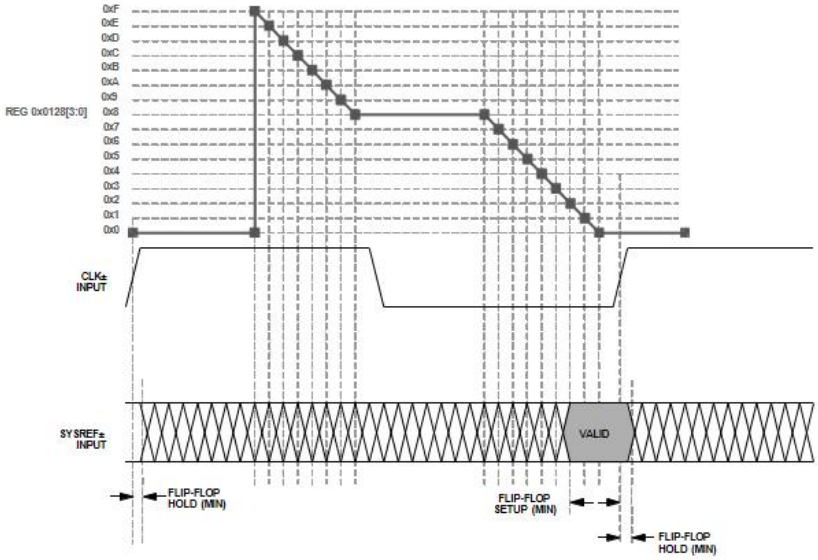

Figure 46 SYSREF±Create Detector

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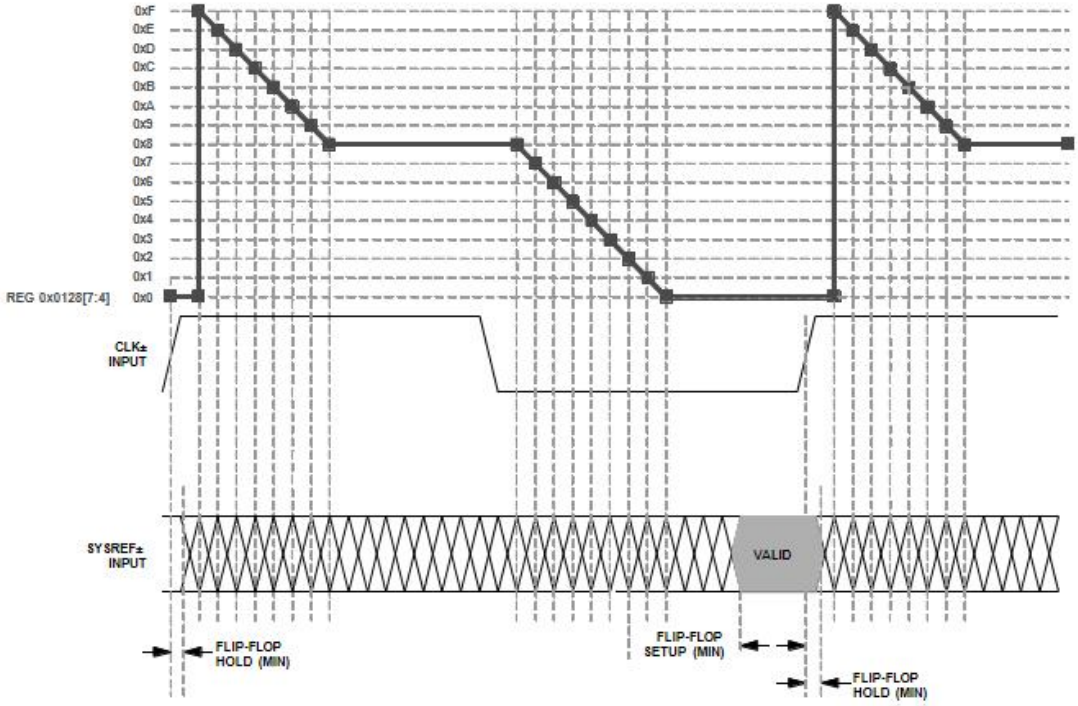

Figure 47 SYSREF±hold detector

Table 27 SYSREF±Settings/Hold Monitor, Register 0x0128

Register 0x0128, Bits[7:4] **Hold Status**	**Register 0x0128, Bits[3:0]** **Setup Status**	**Description**
0x0	0x0 to 0x7	Possible setup error. The smaller this number, the smaller the setup margin.
0x0 to 0x8	0x8	No setup or hold error (best hold margin).
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin).
0x8	0x0	No setup or hold error (best setup margin).
0x9 to 0xF	0x0	Possible hold error. The larger this number, the smaller the hold margin.
0x0	0x0	Possible setup or hold error.

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17.0 Test mode

17.1 ADC Test Mode

The CW9694 has a variety of testing options that facilitate system-level application. The CW9694 has ADC test mode and can be set in register 0x0550. Table 28 describes these test patterns. When output test mode is enabled, the analog portion of the ADC is disconnected from the digital backend block and the test mode runs through the output format module. Some test modes are affected by the output format, while others are not affected. The pseudo-random number (PN) generator in the PN sequence test can be reset by setting bit 4 or bit 5 of register 0x0550. These tests can be with or without Perform in case of analog signals (if present, the analog signal is ignored); however, these tests require an encoded clock.

If the application mode is set to select DDC operating mode, test mode must be enabled for each enabled DDC. Test mode can be enabled via bit 2 and bit 0 of registers 0x0327, 0x0347, and 0x0367, depending on the selected DDC. Channel I is used for the test mode selected by channel A, and channel Q is used for the test mode selected by channel B. For DDC3 only, the I channel is used for the test mode from channel A and the Q channel does not output the test mode. The 0 bit of register 0x0387 selects the channel A test mode for I data.

Table 28 ADC Test Mode 1

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	N/A	N/A	N/A
0001	Midscale short	0000 0000 0000	N/A	N/A
0010	Positive full-scale short	01 1111 1111 1111	N/A	N/A
0011	Negative full-scale short	10 0000 0000 0000	N/A	N/A
0100	Checkerboard	10 1010 1010 1010	N/A	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	x23 + x18 + 1	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	x9 + x5 + 1	0x0092	0x125B, 0x3C9A, 0x2660, 0x0C65, 0x0697
0111	One-/zero-word toggle	11 1111 1111 1111	N/A	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x0551 to Register 0x0558	N/A	User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2] … for repeat mode. User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000 … for single mode.
1111	Ramp output	(x)% 214	N/A	(x) % 2^{14}, (x +1) % 2^{14}, (x +2) % 2^{14}, (x +3) % 2^{14}

[1] N/A means not applicable.

17.2 JESD204B Block Test Mode

In addition to the ADC pipeline test mode, the CW9694 also has flexible test modes in the JESD204B module. These test modes are programmable in Register 0x0573 and Register 0x0574. These test patterns can be injected at different locations in the output data path. Table 29 describes the various test modes available in the JESD204B block. For CW9694, slave test mode (register 0x0573≠0x00) Transition to normal mode (register 0x0573=0x00) requires an SPI soft reset, which can be performed by writing 0x81 to register 0x0000 (self-clearing).

17.2.1 Transport layer sample test mode

CW9694 implements JEDEC JESD204B specification section 5.1.6.3 on-chip Transport layer test mode defined in Section 1. The test is controlled by register 0x571[5]. The test sequence is equivalent to the original sampling points from the ADC.

17.2.2 Interface test mode

The interface test mode is defined in register 0x0573, Bits[3:0]. Table 29 also describes these test modes. Interface tests can be injected at different points in the data. For more information on test injection points, refer to Register 0x0573, Bits[5:4] show the injection locations for these test sequences.

Table 30, Table 31, and Table 32 show some examples of test patterns when the JESD204B sample input, physical layer (PHY) 10-bit input, and scrambler 8-bit input are injected. The UPx in Table 30 to Table 32 represents the user-defined test sequence from the register map.

17.2.3 Data link layer test mode

The CW9694 data link layer test mode is implemented based on the definition in Section 5.3.3.8.2 of the JEDEC JESD204B specification. These tests are defined in Register 0x0574, Bits[2:0]. Inserted test patterns are useful for verifying the functionality of the data link layer. When the data link layer test mode is enabled, turn off SYNCINB± by writing 0xC0 to register 0x0572.

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1000	Ramp output	(x) % 216	Ramp size depends on test injection point
1110	Continuous/repeat user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x0551 to Register 0x0558	User Pattern 1 to User Pattern 4, then zeros

Table 30 Input M=2, S=2, N'=16 (register 0x0573, Bits[5:4] = 'b00)

Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0	0	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	0	1	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	0	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	1	0x5555	0x0000	(x) % 2^{16}	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
1	0	0	0xAAAA	0xFFFF	(x +1) %2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	0	1	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	0	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	1	0xAAAA	0xFFFF	(x +1) % 2^{16}	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
2	0	0	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	0	1	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	0	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	1	0x5555	0x0000	(x +2) % 2^{16}	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
3	0	0	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	0	1	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	0	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	1	0xAAAA	0xFFFF	(x +3) % 2^{16}	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
4	0	0	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	0	1	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	0	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	1	0x5555	0x0000	(x +4) % 2^{16}	0x5FD1	0x9B26	UP1[15:0]	0x0000

Table 31 Physical layer 10-bit input (register 0x0573, Bits[5:4] = 'b01)

10-Bit Symbol Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x155	0x000	(x) % 2^{10}	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	(x + 1) % 2^{10}	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	(x + 2) % 2^{10}	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	(x + 3) % 2^{10}	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	(x + 4) % 2^{10}	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	(x + 5) % 2^{10}	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	(x + 6) % 2^{10}	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	(x + 7) % 2^{10}	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	(x + 8) % 2^{10}	0x18E	0x10F	UP1[15:6]	0x000
9	0x2AA	0x3FF	(x + 9) %2^{10}	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	(x + 10) % 2^{10}	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	(x + 11) % 2^{10}	0x3DD	0x008	UP4[15:6]	0x000

Table 32 Scrambler 8-bit Input (Register 0x0573, Bits[5:4] = 'b10)

8-Bit Octet Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x55	0x00	(x) % 2^{8}	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	(x + 1) % 2^{8}	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	(x + 2) % 2^{8}	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	(x + 3) % 2^{8}	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	(x + 4) % 2^{8}	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	(x + 5) %2^{8}	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	(x + 6) % 2^{8}	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	(x + 7) % 2^{8}	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	(x + 8) % 2^{8}	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	(x + 9) % 2^{8}	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	(x + 10) % 2^{8}	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	(x + 11) % 2^{8}	0xAC	0xFF	UP4[15:9]	0x00

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18.0 Serial Interface (SPI)

The SPI interface of the CW9694 allows users to configure the converter through the structured register space provided internally by the ADC to meet specific functions or operations. SPI is flexible and can be customized according to the specific application. Through the serial port, the address space can be accessed and read and write to the address space. The register space is in bytes and can be further divided into multiple regions. For descriptions of each area, see the Register Map section.

18.1 Configuring with SPI

The SPI of the CW9694 ADC consists of three pins: the SCLK pin, the SDIO pin, and the CSB pin (see Table 33). The SCLK (Serial Clock) pin is used to synchronize data read from the ADC and data written to the ADC. The SDIO (Serial Data Input/Output) pin is a dual-function pin through which data can be sent to or read from the ADC internal register. The CSB (Chip Select Signal) pin is active low, which enables or disables the read and write cycles.

Table 33 Serial port interface pins

Pin	Function description
SCLK	Serial clock. Serial shift clock input for synchronous serial connection
SDIO	Read and write operations of the port. Serial data input/output. Dual function pins, usually used as inputs or output, depending on the sent instruction and relative position in the timing frame.
CSB	Chip selection signal. Active low level, used to gate read and write cycles.

The falling edge of CSB together with the rising edge of SCLK determines the start of the frame. Figure 6

This is an example of a serial timing diagram, and the corresponding definitions are shown in Table 6.

The CSB pin can operate in multiple modes. CSB can be maintained at low power flat state so that the device is always in the enable state; it can also stay at high level between bytes, which allows other external timing; when the CSB pin is pulled

When high, the SPI function is in high impedance mode, in which SPI can be turned on The second function of the pin.

All data consists of 8-bit words. The first bit of each byte of serial data indicates the issued read command or write command, so that the data transmission direction of the SDIO pin can be changed from input to output.

In addition to word length, the instruction cycle also determines whether the serial frame is read or write, so that the chip can be written through the serial port and the on-chip registers are read data. If the instruction is a readback operation, the read operation is performed while the SDIO pin changes from input to output at the appropriate position of the serial frame.

Data can be sent using MSB-first or LSB-first. Power-on is powered on by default and can be matched through SPI.
Set registers to change the data transmission method.

18.2 Hardware Interface

The pins described in Table 33 include the physical interface between the user-programmed device and the CW9694 serial interface. When using the SPI interface, the SCLK pin and the CSB pin are used as inputs. The SDIO pin is bidirectional, as an input pin in the write phase and as an output pin in the readback phase.

The SPI interface is very flexible and can be controlled by an FPGA or a microcontroller. The SPI interface should be disabled when the converter needs to fully utilize its full dynamic performance. Since SCLK, CSB, and SDIO signals are usually asynchronous to the ADC clock, This noise from these signals can reduce the performance of the converter. If the onboard SPI bus is used for other devices, it is recommended to add a buffer between that bus and the CW9694 to prevent these signals from changing at the converter input during the critical sampling period.

18.3 SPI access features

Table 34 briefly describes the functional features accessible through SPI. For details on the CW9694 specific device characteristics, please refer to the "Register Mapping" section.

Table 34 Features that can be accessed through SPI

Functional Features	describe
Working mode	Allows the user to set power down mode or standby mode.
clock	Allows users to access the clock divider via
DDC	SPI. Allows users to set up decimation filters
Test	for different applications.
input/output	Allows the user to set the test mode to obtain known data on the output
output mode	bit. Allows the user to set the output.
SERDES Output Settings	Allows the user to change the SERDES settings.

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19.0 Register Mapping

19.1 Read register map

Each row in the register map table has 8 bits. Register mapping is divided into the following parts:

- Analog Devices SPI Register (Register 0x0000 to Register 0x000D, register 0x18A6 to register 0x1A4D);
- ADC function registers (register 0x003F to register 0x027A, register 0x0701 and register 0x073B)
- DDC function register (register 0x0300 to register 0x0347)
- Digital Output and Test Mode Registers (Register 0x0550 to Register 0x1262)

Table 35 (see the Register Map section) documents the default hexadecimal value for each hexadecimal address shown. Bit 7 (MSB) is the starting bit for the default hexadecimal value. For example, the hexadecimal default value for address 0x0561 (output sampling mode register) is 0x01, which means bit 0 = 1 and the remaining bits are 0. This setting is the default output format (two's complement). See Table 35 for more information on this and other features.

19.2 Disabled and Reserved

All addresses and bits not included in Table 35 are not currently supported by the CW9694. Unused bits of valid address locations should be written to 0 unless the default setting is otherwise.

Address locations need to be written only if a portion of them is unassigned (for example, address 0x0561). If the entire address is disabled (for example, address 0x0013), then the address should not be written.

19.3 Default Values

After CW9694 is reset, the key registers will be loaded with default values. Table 35 (register map table) lists the default values of each register.

19.4 Logic Levels

The following is an explanation of the logic level terms:

"Set" means "set a bit to logic 1" or "write logic 1 to a bit".

- "Clear a bit" means "set a bit to logic 0" or "write logic 0 to a bit".
- X indicates a don't care bit.

19.5 SPI Soft Reset

When performing a soft reset by writing 0x81 to register 0x0000, CW9694 requires 5ms to recover. Therefore, when setting the CW9694 for the application, ensure that sufficient delay time is written into the program firmware after setting the soft reset and before starting the device setting.

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19.6 Register Map Table

The detailed register configuration list of the chip is shown in the table below

Table 35 Register Mapping Table

Register Address	Register Name	Bit	Bit Name	Description	Default	Value Access
Type	0x0000 SPI Configuration A	7	(Global Map)	Soft Reset Mirror (Self Clearing) After soft reset, user must wait 5ms before writing other registers. 1'b0: No operation. 1'b1: Reset SPI and registers (self clearing).	0x0	R/W
		6	LSB First Mirror	1'b1: For all SPI operations, LSB is shifted first. 1'b0: For all SPI operations, MSB is shifted first.	0x0	R/W
		5	Address Self-Increment Mirror	1'b0: Address automatically decreases for multi-byte SPI operations. 1'b1: Address automatically increases for multi-byte SPI operations.	0x0	R/W
		[4:3]	Reserved	Reserved.	0x0	R
		2	Address auto-increment	1'b0: Address auto-decrement for multi-byte SPI operation. 1'b1: Address auto-increment for multi-byte SPI operation.	0x0	R/W
		1	LSB first	1'b1: LSB is shifted first for all SPI operations. 1'b0: MSB is shifted first for all SPI operations.	0x0	R/W
		0	Soft reset (self-clearing)	After soft reset, user must wait 5ms before writing to other registers. 1'b0: No operation. 1'b1: Reset SPI and registers (self-clearing).	0x0	WC
0x0001	SPI Configuration B	7	Single instruction	1'b0: SPI stream enabled 1'b1: (multi-byte read/write) disabled. Only one read or write operation is performed regardless of the state of the CSB line	0x0	R/W
		[6:2]	Reserved	Reserved.	0x0	R
		1	Datapath soft reset (self-clearing)	1'b0: Normal operation. 1'b1: Datapath soft reset (self-clearing).	0x0	R/W
		0	Reserved	Reserved.	0x0	R
0x0002	Chip configuration	[7:2]	Reserved	Reserved.	0x0	R
		[1:0]	Channel power mode	Channel power mode: 2'b00: Normal mode (power-on). 2'b10: Standby mode, digital circuit datapath clock disabled; JESD204B interface enabled, normal output. 2'b11: Power-down mode, digital circuit datapath clock disabled, datapath held in reset state, JESD204B interface turned off, output turned off.	0x0	R/W
0x0003	Chip type	[7:0]	Chip type	Chip type: High-speed analog-to-digital converter.	0x3	R

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Register address	Register name	Bit	Bit name	describe	default value	Access Type
0x0004	Chip ID (LSB)	[7:0]	Chip ID[7:0]	Chip ID Low byte.	0xDE	R
0x0005	Chip ID (MSB)	[7:0]	Chip ID [15:8]	Chip ID High byte.	0x00	R
0x0006	Chip grade	[7:4]	Chip speed level	Chip speed level: 4x0101: 500MSPS.	0x0	R
		[3:0]	reserve	reserve.	0x0	R
0x0008	Chip channel index	[7:2]	reserve	reserve.	0x0	R
		1	B/D Channel	1'b0: Channel B/D does not accept the next SPI command. 1'b1: Channel B/D accepts the next SPI command.	0x1	R/W
		0	A/C channel	1'b0: Channel A/C does not accept the next SPI command. 1'b1: Channel A/C accepts the next SPI command.	0x1	R/W
0x0009	Channel-to-index	[7:2]	reserve	reserve	0x0	R
		1	C/D Channel	1'b0: Channel C/D does not accept the next SPI command. 1'b1: Channel C/D accepts the next SPI command.	0x1	R/W
		0	A/B Channel	1'b0: Channel A/B does not accept the next SPI command. 1'b1: Channel A/B accepts the next SPI command.	0x1	R/W
0x000C	Manufacturer ID (LSB)	[7:0]	Manufacturer ID [7:0]	Manufacturer ID Low byte.	0x56	R
0x000D	Manufacturer ID (MSB)	[7:0]	Manufacturer ID [15:8]	Manufacturer ID High byte.	0x04	R
0x003F	Chip power-off pin	7	PDWN/STBY Disabled	This register is used with register 0x0040. 1'b0: The power off pin (PDWN/STBY) is enabled. Global pin control selection is enabled (default); 1'b1: Power-off pin (PDWN/STBY) is disabled/ignored. Global pin control selection has been ignored;	0x0	R/W
		[6:0]	reserve	reserve	0x0	R
0x0040	Chip pin control	[7:6]	PDWN/STBY function	2'b0: Power off pin, power down/standby pin is used as chip full Power down in the game; 2'b01: Standby pin, external power is turned off, the chip enters standby mode; 2'b10: Disable pins. Ignore the pin status;	0x0	R/W
		[5:3]	Quick detection B/D (FD_B/D)	3'b0: Quick detection of B/D output; 3'b001: JESD204B LMFC output; 3'b010: JESD204B internal SYNC output; 3'b111: Disabled (configured with weak pull-down resistor)	0x7	R/W
		[2:0]	Fast Detect A/C (FD_A/C)	3'b0: Fast Detect A/C Output; 3'b001: JESD204B LMFC Output; 3'b010: JESD204B Internal SYNC Output; 3'b111: Disable (Configured with Weak Pull-Down Resistor)	0x7	R/W
0x0108	Clock Divider Control	[7:3]	Reserved	Reserved	0x0	R
		[2:0]	Clock Divider	3'b0: Divide by 1; 3'b001: Divide by 2; 3'b010: Divide by 4; 3'b111: Divide by 8;	0x1	R/W

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0x0109	Clock Divider Phase	[7:4]	Reserved	Reserved	0x0	R
		[3:0]	Clock Divider Phase Offset	4'b0: 0 Input Clock Cycle Delay; 4'b0001: 0.5 Input clock cycle delay (inverted clock); 4'b0010: 1 input clock cycle delay; 4'b0011: 1.5 input clock cycle delay; 4'b0100: 2 input clock cycle delay; 4'b0101: 2.5 input clock cycle delay; 4'b0110: 3 input clock cycle delay; 4'b0111: 3.5 input clock cycle delay; 4'b1000: 4 input clock cycle delay; 4'b1001: 4.5 input clock cycle delay; 4'b1010: 5 input clock cycle delay; 4'b1011: 5.5 input clock cycle delay; 4'b1100: 6 input clock cycle delay; 4'b1101: 6.5 input clock cycle delay; 4'b1110: 7 input clock cycle delay; 4'b1111: 7.5 Input clock cycle delay;	0x0	R/W
0x1B84	Clock delay fine adjustment	[7:0]		Clock delay fine adjustment, stepping in 0.15ps: 0x00~0x7F (0 to 127 delay steps adjustable)	0x0	R/W
0x1B85	Clock delay coarse adjustment	[7:0]		Clock delay rough adjustment, stepping at 10ps: 0x00~0x1E (0 to 30 delay steps adjustable)	0xC0	R/W
0x011F	Clock DCS control word (duty cycle stabilizer)	[7:0]	Clock DCS enabled	0x84: DCS Bypass 0x81: DCS enabled	0x84	R/W
0x0120	SYSREF Control 1	7	reserve	reserve	0x0	R
		6	SYSREF± flag reset	1'b0: Normal flag operation. 1'b1: SYSREF± flag holds when reset (establish/hold error flag clears)	0x0	R/W
		5	reserve	reserve	0x0	R
		4	SYSREF±Conversion Selection	1'b0: SYSREF± is valid on the rising edge of the selected CLK±. Change this setting When SYSREF± mode selection must be set to disabled. 1'b1: SYSREF± is valid on the selected falling edge of CLK. Even Change this setting When SYSREF± mode selection must be set to disabled.	0x0	R/W
		3	CLK±Edge Selection	1'b0: Snap on the rising edge of CLK±. 1'b1: Snap on the falling edge of CLK±.	0x0	R/W
		[2:1]	SYSREF Mode selection	2'b0: Disabled 2'b01: Continuous mode 2'b10: N shot mode	0x0	R/W
		0	reserve	reserve	0x0	R
0x0121	SYSREF Control 2	[7:4]	reserve	reserve	0x0	R
		[3:0]	SYSREF N times ignore counter selection	4'b0: Not ignored 4'b0001: Ignore the first 1 SYSREF±; 4'b0010: Ignore the first 2 SYSREF±;; 4'b0011: Ignore the first 3 SYSREF±; 4'b0100: Ignore the first 4 SYSREF±; 4'b0101: Ignore the first 5 SYSREF±; 4'b0110: Ignore the first 6 SYSREF±; 4'b0111: Ignore the first 7 SYSREF±; 4'b1000: Ignore the first 8 SYSREF±; 4'b1001: Ignore the first 9 SYSREF±; 4'b1010: Ignore the first 10 SYSREF±; 4'b1011: Ignore the first 11 SYSREF±; 4'b1100: Ignore the first 12 SYSREF±; 4'b1101: Ignore the first 13 SYSREF±; 4'b1110: Ignore the first 14 SYSREF±; 4'b1111: Ignore the first 15 SYSREF±;	0x0	R/W

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Register address	Register name	Bit	Bit name	describe	default value	Access Type
0x0123	SYSREF Control 4	7	reserve	reserve	0x0	R
		[6:0]	SYSREF± timestamp delay, Bits[6:0]	SYSREF± timestamp delay (within the converter sampling clock cycle) 0:0 sampling clock cycle delay 1:1 sampling clock cycle delay …… 127:127 Sampling clock cycle delay	0x40	R/W
0x0128	SYSREF Status 1	[7:4]		SYSREF±Retain	0x0	R
		[3:0]		SYSREF±estest status	0x0	R
0x0129	SYSREF Status 2	[7:4]	reserve	reserve	0x0	R
		[3:0]	When SYSREF± Clock frequency-dividing phase when captured	4'b0: Align 4'b0001: SYSREF± delay clock 0.5 cycles; 4'b0010: SYSREF± delay clock 1 cycle; 4'b0011: SYSREF± delay clock 1.5 cycles±; … 4'b1101: SYSREF± delay clock 6.5 cycles; 4'b1110: SYSREF± delay clock 7 cycles; 4'b1111: SYSREF± delay clock by 7.5 cycles;	0x0	R
0x012A	SYSREF Status 3	[7:0]	SYSREF counter, capture SYSREF± Bits[7:0] increment	Whenever SYSREF± is captured, the run counter is incremented. Can be reset via Bit6 in register 0x0120. 255 is counted to return. These bits are read only when register 0x0120, bits [2:1] are disabled	0x0	R
0x01FF	Chip synchronization	[7:1]	reserve	reserve	0x0	R
		0	Synchronous mode	1'b0: Sampling synchronization mode. SYSREF± signal reset all internal sample points Orchestration. Use this mode when synchronizing multiple chips as specified in the JESD204B standard. If the phase of any divider If you need to change the JESD204B link, it will be disconnected. 1'b1: Partial Synchronization/Timestamp Mode. SYSREF± signal is no longer bit sample internal allocator. In this mode, the JESD204B link, signal monitor, and parallel interface clock are not affected by the SYSREF± signal. The SYSREF± signal simply timestamps the sample as it passes through the ADC.	0x0	R/W
0x0200	Chip mode	[7:6]	reserve	reserve	0x0	R
		5	Chip Q is ignored	1'b0: Select real number (I) and complex number (Q) 1'b1: Only real numbers (I) are selected, complex numbers (Q) are ignored		
		4	reserve	reserve	0x0	R
		[3:0]	Chip application mode	4'b0: Full bandwidth mode (default); 4'b0001: A DDC mode (DDC0 only) 4'b0010: Two DDC modes (DDC0 and 1 only)	0x0	R/W

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Register address	Register name	Bit	Bit name	describe	default value	Access Type
0x0201	Chip extraction rate	[7:3]	reserve	reserve	0x0	R
		[2:0]	Chip extraction rate selection	3'b0: 1x decimation, full sampling rate mode (default); 3'b001: 2 times draw 3'b010: 4 times draw 3'b011: 8 times draw 3'b100: 16 times draw	0x0	R/W
0x0228	Custom channel offset	[7:0]	LSB offset adjustment from +127 to -128	Digital data path offset. Two complement offset adjustments aligned with the least effective converter resolution bits	0x0	R/W
0x0245	Fast Detect Control	[7:4]	Reserved	Reserved	0x0	R
		3	Force Enable FD_A/FD_B/FD_C /FD_D pins.	1'b0: Normal mode, fast detection output pin works normally 1'b1: Fast detection output pin is forced to assign a value	0x0	R/W
		2	Force FD_A/FD_B/FD_C /FD_D pin value (If the forced pin is true, this value is output on the FDx pin)	When the output is forced, the fast detection output pin of this channel is set to this value	0x0	R
		1	Reserved	Reserved	0x0	R
		0	Enable fast detection output	1'b0: Fast detection output function disabled 1'b1: Fast detection output function enabled	0x0	R/W
0x0247	Fast detection upper threshold low	[7:0]		Programmable 13-bits, fast detection upper threshold low eight bits [7:0]	0x0	R/W
0x0248	Fast detection upper threshold high	[7:5]	Reserved	Reserved	0x0	R
		[4:0]		Programmable 13-bits, fast detection upper threshold high five bits [12:8]	0x0	R/W
0x0249	fast detection lower threshold low bit	[7:0]		Programmable 13-bits, fast detection lower threshold low eight bits [7:0]	0x0	R/W
0x024A	fast detection upper threshold high bit	[7:5]	Reserved	Reserved	0x0	R
		[4:0]		Programmable 13-bits, fast detection lower limit threshold is high five digits [12:8]	0x0	R/W
0x024B	Quick detection of low dwell time	[7:0]	Rapid detection of dwell time low [7:0]	Quickly detect LSBs of the dwell time counter target, which is a 16-bit meter The load value of the counter to determine how long the ADC data must remain below the lower threshold before the FD x pin reset to 0	0x0	R/W
0x024C	Quick detection of dwell time high	[7:0]	Rapid detection of residence time high [15:8]	Quickly detect LSBs of the dwell time counter target, which is a 16-bit meter The load value of the counter to determine how long the ADC data must remain below the lower threshold before the FD x pin reset to 0	0x0	R/W
0x026F	Signal monitoring synchronization control	[7:2]	reserve	reserve	0x0	R
		1	reserve	reserve	0x0	R/W
		0	Signal monitoring synchronization mode	1'b0: Synchronous disabled 1'b1: Only on the next valid edge of the SYSREF± pin Synchronous signal monitoring. The edge of the SYSREF± pin will be ignored. When the next SYSREF± is received, this bit will be cleared. The SYSREF± input pin must be enabled to synchronize the signal monitoring module.	0x0	R/W
		[7:2]	reserve	reserve	0x0	R

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0x0270	Signal monitoring and control	1	Peak detector	1'b0: Disable the peak detector 1'b1: Enable peak detector	0x0	R/W
		0	reserve	reserve	0x0	R
0x0271	Signal Monitor Period 1	[7:0]	Signal monitor cycle [7:0]	This 24-bit value is used to set the number of output clock cycles for which the signal monitor performs its operation. Bit0 is ignored	0x0	R/W
0x0272	Signal Monitor Period 2	[7:0]	Signal monitor cycle [15:8]	This 24-bit value is used to set the number of output clock cycles for which the signal monitor performs its operation. Bit0 is ignored		
0x0273	Signal Monitor Period 3	[7:0]	Signal monitor cycle [23:16]	This 24-bit value is used to set the number of output clock cycles for which the signal monitor performs its operation. Bit0 is ignored		
0x0274	Signal monitor status control	[7:5]	reserve	reserve	0x0	R
		4	Result update	1'b1: Status update based on bit[2:0] (self-clearing)	0x0	R/W
		3	reserve	reserve	0x0	R
Register address	Register name	Bit	Bit name	describe	default value	Access Type
		[2:0]	Results selection	3'b001: Peak monitor reads the signal back	0x1	R/W
0x0275	Signal Monitor Status 0	[7:0]	Signal monitoring result bit [7:0]	Signal monitor status results. This 20-bit value contains the status results calculated by the signal monitor block. Content depends on register 0x0274, setting of bit [2:0].	0x0	R
0x0276	Signal Monitor Status 1	[7:0]	Signal monitoring result bit [15:8]	Signal monitor status results. This 20-bit value contains the status results calculated by the signal monitor block. The content depends on the setting of register 0x0274, bit [2:0].	0x0	R
0x0277	Signal Monitor Status 2	[7:4]	reserve	reserve	0x0	R
		[3:0]	Signal monitoring result bit [19:16]	Signal monitor status results. This 20-bit value contains the signal monitored The status result of the calculation of the machine block. Content depends on register 0x0274, setting of bit [2:0].	0x0	R
0x0278	Signal Monitor Status Frame Counter	[7:0]	Period count result bit [7:0]	Signal Monitor Frame Counter Status bit. Whenever the period counter expires, the frame counter is incremented.	0x0	R
0x0279	Signal monitor serial frame control	[7:2]	reserve	reserve	0x0	R
		1	reserve	reserve	0x0	R/W
		0	Based on JESD204B Ability signal monitor results	1'b0: Disabled 1'b1: Enable	0x0	R

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0x0300	DDC synchronization control	7	reserve	reserve	0x0	R/W
		6	reserve	reserve	0x0	R/W
		5	reserve	reserve	0x0	R
		4	DDC NCO soft reset	This bit can be used to synchronize all NCOs within the DDC 1'b0: Working normally 1'b1: DDC remains reset	0x0	R/W
		[3:2]	reserve	reserve	0x0	R
		1	DDC synchronizes next time	The SYSREF± pin must be an integer multiple of the period of the NCO frequency for this function to operate correctly in continuous mode. 1'b0: Continuous Mode 1'b1: Next on the SYSREF± pin in the DDC module Valid edge. Subsequently SYSREF± is ignored. The DDC Sync Enable bit is cleared when the next SYSREF± valid edge is received.	0x0	R/W
		0	DDC synchronization mode	The SYSREF± input pin must be enabled to synchronize DDCs. 1'b0: Disable synchronization 1'b1: If DDC next sync==1, only SYSREF± The next active edge of the pin is used to synchronize the NCO. The subsequent edge of the SYSREF± pin is ignored. This bit is cleared when the next SYSREF± edge is received	0x0	R/W
0x0310	DDC 0 control	7	DDC 0 Mixer Selection	1'b0: Real mixer (I and Q inputs must come from the same real channel) 1'b1: Complex mixer (I and Q must come from the ADC receiving channel of the real and imaginary inputs)	0x0	R/W
		6	DDC 0 Gain Selection	Gain can be used to compensate and downconvert the input signal and filter 6dB loss associated with negative frequency 1'b0: 0dB Gain 1'b1: 6dB gain (multiply by 2)	0x0	R/W
		[5:4]	DDC 0 IF mode	2'b0: Variable IF mode 2'b01: Zero IF mode 2'b10: fS/4 mid-frequency mode 2'b11: Test mode	0x0	R/W
		3	DDC 0 complex to real number enable	1'b0: The complex (I and Q) output contains valid data 1'b1: Only (I-channel) output, complex to real number is valid, converted from additional fS/4 mixing to real number.	0x0	R/W
		2	reserve	reserve	0x0	R
		[1:0]	DDC 0 Draw rate selection	Selection of decimation filter 2'b11: HB1: 1x decimation (real output (complic to real conversion function is enabled)) or 2x decimation (complic to real conversion (complic to real conversion is disabled)) 2'b0: HB2 + HB1: 2x decimation (real output) or 4x decimation (complex output) 2'b01: HB3 + HB2 + HB1: 4x decimation (real output) or 8x decimation (complex output) 2'b10: HB4 + HB3 + HB2 + HB1: 8 times decimation (real output) or 16 times (complex output)	0x0	R/W

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Register address	Register name	Bit	Bit name	describe	default value	access type
0x0550	Test mode control	7	User mode selection	1'b0: Continuous repeating pattern 1'b1: Single shot mode	0x0	R/W
		6	reserve	reserve	0x0	R
		5	Reset long PN sequence generator	1'b0: Enable long PN sequence 1'b1: keep reset	0x0	R/W
		4	Reset short PN sequence generator	1'b0: Enable short PN sequence 1'b1: keep reset	0x0	R/W
		[3:0]	Test mode selection	4'b0: Turn off test mode 4'b0001: Half-scale output 4'b0010: Positive full scale 4'b0011: Negative full scale 4'b0100: Alternate board 4'b0101: long PN sequence 4'b0110: short PN sequence 4'b0111: 0/1 word switching 4'b1000: User-defined test mode (used with registers) 4'b1111: ramp output	0x0	R/W
0x0559	Output control mode 0	7	reserve	reserve	0x0	R
		[6:4]	Converter control bit bit1 selection	3'b0: Pull low (1'b0); 3'b001: over-range bit 3'b010: signal detector bit 3'b011: Fast detection (FD) bit 3'b100: reserved 3'b101：SYSREF± 3'b110: Reserved 3'b111: Reserved	0x0	R/W
		3	Reserved	Reserved	0x0	R
		[2:0]	Converter control bit bit0 selection	3'b0: pull low (1'b0); 3'b001: over range bit 3'b010: signal detector bit 3'b011: fast detect (FD) bit 3'b100: SYSREF± 3'b101: Reserved 3'b110: Reserved 3'b111: Reserved	0x0	R/W
0x055A	Output control mode 1	[7:3]	Reserved	Reserved	0x0	R
		[2:0]	Converter control bit bit0 selection	3'b0: pull low (1'b0); 3'b001: over range bit 3'b010: signal detector bit 3'b011: fast detect (FD) bit Bit 3'b100: Reserved 3'b101: SYSREF± 3'b110: Reserved 3'b111: Reserved	0x01	R/W
0x0561	Output sampling mode	[7:3]	Reserved	Reserved	0x0	R
		2	Sampling data flip	1'b0: ADC sampling data not flipped 1'b1: ADC sampling data flipped	0x0	R/W
		[1:0]	Data output format selection	2'b0: Offset binary code 2'b01: Two's complement code	0x1	R/W

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Register Address	Register Name	Bit	Bit Name	Description	Default Value	Access Type
0x0564	Output lane selection	[7:2]	Reserved	Reserved	0x0	R
		1	Reserved	Reserved	0x0	R/W
		0	Converter lane swap control	1'b0: Normal lane order 1'b1: Enable lane swap function	0x0	R/W
0x056E	JESD204B mapping PLL control	[7:4]	JESD204B lane transfer Transmission rate	4'b0: Lane rate = 8 Gbps to 13.1 Gbps 4'b0001: Lane rate = 4 Gbps to 6.75 Gbps 4'b0101: Lane rate = 2 Gbps to 3.375 Gbps 4'b1000: Lane rate = 6.75 Gbps to 8 Gbps 4'b1001: Lane rate = 3.375 Gbps to 4 Gbps 4'b1101: Lane rate = 1.6875 Gbps to 2 Gbps 4'b0011: reserved	0x0	R/W
		[3:0]	Reserved	Reserved	0x0	R
0x056F	JESD204B Mapping PLL Status	7	PLL Lock Status	1'b0: Unlocked 1'b1: Locked	0x0	R
		[6:4]	Reserved	Reserved	0x0	R
		3	Reserved	Reserved	0x0	R
		[2:0]	Reserved	Reserved	0x0	R
0x0570	JESD204B Mapping JTX Fast Configuration	[7:6]	Fast Configuration L Value	Number of Lanes L 1'b0: L=1 1'b1: L=2	0x1	R/W
		[5:3]	Fast Configuration M Value	Number of Converters M 3'b0: M=1 3'b001: M=2 3'b010: M=4	0x1	R/W
		[2:0]	Fast Configuration F Value	Number of Octet Frames F 3'b0: F=1 3'b001: F=2 3'b010: F=4 3'b011: F=8	0x1	R/W

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0x0571	JESD204B Mapping JTX Link Control 1	7	STBY Mode	1'b0: Standby mode forces all converter samples to 0 1'b1: Standby mode forces code group synchronization (/K28.5 characters)	0x0	R/W
		6	Tail bit (t) pseudo-random sequence	1'b0: Disable 1'b1: Enable	0x0	R/W
		5	Long transport layer test	1'b0: Disable JESD204B test sampling 1'b1: Enable JESD204B test sampling Long transport layer test sampling sequence sent on all link lanes	0x0	R/W
		4	Lane synchronization	1'b0: Disable FACI using /K28.7/ 1'b1: Enable FACI using /K28.7/ and /K28.3/	0x1	R/W
		[3:2]	ILAS sequence test	2'b0: Disable initialization lane alignment sequence--(JESD204B 5.3.3.5) 2'b01: Enable initialization lane alignment sequence--(JESD204B 5.3.3.5) 2'b11: Initialization lane alignment sequence is always in test mode- -JESD204B Data link layer test mode, in which the channel alignment sequence is repeatedly sent on all channels	0x1	R/W
		1	Frame-aligned character insertion (FACI)	1'b0: Enable frame alignment character insertion 1'b1: Disable frame alignment character insertion--debug only	0x0	R/W
		0	Link layer control	1'b0: Enable JESD204B serial transmission link. Used for code group Step /K28.5/ Character transmission is controlled by the SYNCINB±x pin 1'b1: JESD204B serial link powered off (keep reset and clock strobe)	0x0	R/W
0x0572	JESD204B mapping JTX Link Control 2	[7:6]	SYNCINB±x pin control	2'b0: Normal mode 2'b01: Ignore SYNCINB±x (force CGS) 2'b11: Ignore SYNCINB±x (force LAS/user data)	0x0	R/W
		5	SYNCINB±x pin Flip	1'b0: SYNCINB±x pin does not flip 1'b1: SYNCINB±x pin flip	0x0	R/W
		4	SYNCINB±x pin type	1'b0: LVDS Differential SYNC Input 1'b1: CMOS single-ended SYNC input	0x0	R/W
		3	reserve	reserve	0x0	R
		2	8-bit/10-bit bypass enable	1'b0: Enable 8-bit/10-bit 1'b1: Bypass 8-bit/10-bit	0x0	R/W
		1	8-bit/10-bit flip	1'b0: Normal 1'b1: Flip abcdefghij symbol	0x0	R/W
		0	reserve	reserve	0x0	R
0x0573	JESD204B mapping JTX Link Control 3	[7:6]	Checksum mode	2'b0: Checksum is for all 8-bit registers in the link configuration table sum 2'b01: Checksum is the sum of all single link configuration fields (LSB aligned) 2'b10: Disable checksum (set to zero). For testing purposes only 2'b11: Not used	0x0	R/W
		[5:4]	Test injection points	2'b0:N' sampling input 2'b01: 10-bit data output from 8-bit/10-bit (for PHY test) 2'b10: 8-bit data input from the scrambler	0x0	R/W

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Register address	Register name	Bit	Bit name	describe	default value	Access Type
		[3:0]	JESD204B Test Model Style	4'b0: Working normally (test mode is disabled) 4'b0001: Alternate board mode 4'b0010: 1/0 word switch 4'b0011:31-bit PN sequence: x31+ x28+1 4'b0100: 23-bit PN sequence: x23+ x18+1 4'b0101: 15-bit PN sequence: x15+ x14+1 4'b0110: 9-bit PN sequence: x9+ x5+1 4'b0111: 7-bit PN sequence: x7+ x6+1 4'b1000: Ramp output 4'b1110: Continuous user testing 4'b1111: Single user test	0x0	R/W
0x0574	JESD204B mapping JTX Link Control 4	[7:4]	ILAS delay	4'b0: Transfer initial channel alignment sequence on the 1st local multi-frame clock after SYNCINB±x is invalid 4'b0001: Transfer initial channel alignment sequence on the 2nd local multi-frame clock after SYNCINB±x is invalid 4'b0010: Transfer initial channel alignment sequence on the 3rd local multi-frame clock after SYNCINB±x is invalid 4'b0011: Transfer initial channel alignment sequence on the 4th local multi-frame clock after SYNCINB±x is invalid 4'b0100: Transfer initial channel alignment sequence on the 5th local multi-frame clock after SYNCINB±x is invalid 4'b0101: Transfer initial channel alignment sequence on 6th local multi-frame clock after SYNCINB±x is invalid 4'b0110: Transfer initial channel alignment sequence on 7th local multi-frame clock after SYNCINB±x is invalid 4'b0111: Transfer initial channel alignment sequence on the 8th local multi-frame clock after SYNCINB±x is invalid 4'b1000: Transfer initial channel alignment sequence on the 9th local multi-frame clock after SYNCINB±x is invalid 4'b1001: After SYNCINB±x is invalid, in the 10th book Transmission of initial channel alignment sequence on ground multi-frame clock 4'b1010: Transmission of initial channel alignment sequence on the 11th local multi-frame clock after SYNCINB±x is invalid 4'b1011: Transmission of initial channel alignment sequence on the 12th local multi-frame clock after SYNCINB±x is invalid 4'b1100: Transmission of initial channel alignment sequence on the 13th local multi-frame clock after SYNCINB±x is invalid 4'b1101: Transmission of initial channel alignment sequence on the 14th local multi-frame clock after SYNCINB±x is invalid 4'b1110: Transmission of initial channel alignment sequence on the 14th local multi-frame clock after SYNCINB±x is invalid 4'b1110: Transmission of initial channel alignment sequence on the 14th local multi-frame clock after SYNCINB±x is invalid 4'b1110: Transmission of initial channel alignment sequence on the 13th local multi-frame clock after SYNCINB±x is invalid 4'b1110: Transmission of initial channel alignment sequence on the 14th local multi-frame clock after SYNCINB±x is invalid 4'b1110: Transmission of initial channel alignment sequence on the 12th local multi-frame clock after SYNCINB±x is invalid 4'b1110: Transmission of initial channel alignment sequence on the 13th local multi-frame clock after SYNCINB±x is invalid 4'b1110: Transmission of initial channel alignment sequence on the 13th local multi-frame clock after SYNCINB±x is invalid Transmission of initial channel alignment sequence on each local multi-frame clock 4'b1111: Transmission of initial channel alignment sequence on the 16th local multi-frame clock after SYNCINB±x is invalid	0x0	R/W
		3	reserve	reserve	0x0	R
		[2:0]	Link layer test mode	3'b0: Works normally (disable link layer test mode) 3'b001: Continuous /D21.5/character sequence 3'b010: Reserved 3'b011: Reserved 3'b100: Adjusted RPAT test sequence 3'b101: JSPAT test sequence 3'b110: JTSPAT test sequence 3'b111: Reserved	0x0	R/W

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Register address	Register name	Bit	Bit name	describe	default value	Access Type
0x0578	JESD204 B mapping JTX LMFC offset	[7:5]	reserve	reserve	0x0	R
0x0578	JESD204 B mapping JTX LMFC offset	[7:5]	reserve	reserve	0x0	R
		[4:0]	LMFC phase offset value	Local multi-frame clock (LMFC) phase offset value, reset of LMFC phase counter when SYSREF± is valid. For deterministic delay applications	0x0	R/W
0x058B	JESD204B mapping SCR/L configuration	7	JESD204B Scramble	1'b0: Disable JESD204x scrambler (SCR = 0) 1'b1: Enable the JESD204x scrambler (SCR = 1)	0x1	R/W
		[6:5]	reserve	reserve	0x0	R
		[4:0]	JESD204B Channel	1'b0: One channel per link (L = 1) 1'b1: One channel per link (L = 2)	0x1	R/W
0x058C	JESD204B mapping F configuration	[7:0]	Number of octets per frame (F)	Number of octets in each frame, F=Register 0x058C Bits[7:0]+1	0x1	R

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Register address	Register name	Bit	Bit name	describe	default value	Access Type
0x058D	JESD204B mapping K configuration	[7:5]	reserve	reserve	0x0	R
		[4:0]	Number of frames in each multi-frame (K)	JESD204B Number of frames per multi-frame (K = register 0x058D, bit [4:0]+1), can only be used that can be divisible by 4 F×K value. 5'b00011: K = 4 5'b00111: K = 8 5'b01100: K = 12 5'b01111: K = 16 5'b10011: K = 20 5'b10111: K = 24 5'b11011: K = 28 5'b11111: K = 32	0x1F	R/W
0x058E	JESD204B mapping M configuration	[7:0]	Number of converters on each link	8'b0: A virtual converter (M = 1) 8'b01: A virtual converter (M = 2) 8'b11: A virtual converter (M = 4)	0x1	R
0x058F	JESD204B mapping CS/N configuration	[7:6]	Number of control bits per sample (CS)	2'b0: No control bit (CS = 0) 2'b01: 1 control bits (CS = 1), only control bit 2; 2'b10: 2 control bits (CS = 2), control bits 2 and bits 1; 2'b11: 3 control bits (CS = 3)		
		5	Reserved	Reserved	0x0	R
		[4:0]	ADC converter resolution (N)	5'b00110: N = 7 5'b00111: N = 8 5'b01000: N = 9 5'b01001: N = 10 5'b01010: N = 11 5'b01011: N = 12 5'b01100: N = 13 5'b01101: N = 14 5'b01110: N = 15 5'b01111: N = 16	0xF	R/W
0x0590	JESD204B Mapping Subclass Version and N' Configuration	[7:5]	Subclass Support	3'b000: Subclass 0 3'b001: Subclass 1	0x1	R/W
		[4:0]	ADC bits per sample (N')	5'b00111: N' = 8 5'b01111: N' = 16	0xF	R/W
0x0591	JESD204B mapping S configuration	[7:5]	Reserved	Reserved	0x1	R
		[4:0]	Number of samples per converter frame period (S)	Number of samples per converter frame period (S = register 0x0591, Bits[4:0] + 1)	0x0	R
0x0592	JESD204B mapping Transmission interface high density and link CF configuration	7	HD (High density) value	1'b0: disable high density format 1'b1: enable high density format	0x0	R
		[6:5]	reserve	reserve	0x0	R
		[4:0]	Each link at each frame Control word for clock cycle (CF)	Control word for each frame clock cycle per link (CF=Register 0x0592, Bits[4:0])	0x0	R
0x05A0	JESD204B transmission interface checksum 0 configuration	[7:0]	SERDOUTx0±Calibration and 0's check value	The serial checksum value of channel 0. Automatically calculate for each channel. Sum (all link configuration parameters for channel 0) %256	0xC3	R

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Register Address	Register Name	Bits	Bit Name	Description	Default Value	Access Type
0x05A1	JESD204B transmission interface checksum 1Configuration	[7:0]	SERDOUTx1±Calibration and 0's check value	The serial checksum value of channel 1. Automatically calculate for each channel. Sum (all link configuration parameters for channel 1) %256	0xC4	R
0x05B0	SERDOUTx0±/SERDOUTx 1±Channel power-off configuration	[7:3]	reserve	reserve	0x1	R/W
		2	SERDOUTx1±Lane 1 Power off	Lane1 Forced power outage	0x0	R/W
		1	reserve	reserve	0x1	R/W
		0	SERDOUTx0±Lane 0 Power off	Lane0 Forced power outage	0x0	R/W
0x05B2	JESD204B mapping Transmission interface channel allocation 1	[7:3]	reserve	reserve	0x1	R
		[2:0]	SERDOUTx0± lane assignment	3'b000: Logic Lane 0 (default) 3'b001: Logic Lane 1 3'b010: Logic Lane 2 3'b011: Logic Lane 3	0x0	R/W
0x05B2	JESD204B mapping Transmission interface channel assignment 2	[7:3]	Reserved	Reserved	0x1	R
		[2:0]	SERDOUTx1± lane assignment	3'b000: Logic Lane 0 3'b001: Logic Lane 1 (default) 3'b010: Logic Lane 2 3'b011: Logic Lane 3	0x1	R/W
0x05C0	JESD204B Serial Driver Adjustment	[7:3]	Reserved	Reserved	0x1	R
		[2:0]	SERDOUTx0± Voltage Swing	3'b000: 326mVp-p 3'b001: 405mVp-p 3'b010: 483mVp-p 3'b011: 560mVp-p 3'b100: 634mVp-p 3'b101: 704mVp-p 3'b110: 768mVp-p 3'b111: Reserved	0x1	R/W
0x05C1	JESD204B Serial Driver Adjustment	[7:3]	Reserved	Reserved	0x1	R
		[2:0]	SERDOUTx1± voltage Swing	3'b000: 326mVp-p 3'b001: 405mVp-p 3'b010: 483mVp-p 3'b011: 560mVp-p 3'b100: 634mVp-p 3'b101: 704mVp-p 3'b110: 768mVp-p 3'b111: Reserved	0x1	R/W

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Register Address	Register Name	Bits	Bit Name	Description	Default Value	Access Type
0x05C4	JESD204B serial logic channel 0 pre-emphasis selection register	7	Post tap enable	1'b0: disable 1'b1: enable	0x0	R/W
		[6:4]	Post tap level	3'b000: 0dB (when voltage swing is set to 0, insertion loss 0dB to 4dB, recommended) 3'b001: 3dB (recommended when the voltage swing is set to 0 and the insertion loss is 4dB to 9dB) 3'b010: 6dB (recommended when the voltage swing is set to 0 and the insertion loss is 9dB to 14dB) 3'b011: 9 dB (recommended when the voltage swing is set to 0 and the insertion loss is >14dB) 3'b100: 12 dB	0x0	R/W
		[3:0]	Reserved	Reserved	0x0	R
0x05C6	JESD204B Serial Logic Lane 1 Pre-emphasis Select Register	7	Post tap enable		0x0	R/W
		[6:4]	Post tap level	3'b000: 0dB (recommended when the voltage swing is set to 0 and the insertion loss is 0dB to 4dB) 3'b001: 3dB (recommended when the voltage swing is set to 0 and the insertion loss is 4dB to 9dB) 3'b010: 6dB (recommended when the voltage swing is set to 0 and the insertion loss is 9dB to 14dB) 3'b011: 9 dB (recommended when the voltage swing is set to 0 and the insertion loss is >14dB) 3'b100: 12 dB	0x0	R/W
		[3:0]	Reserved	Reserved	0x0	R
0x1222	PLL calibration	7	Reserved	Reserved	0x0	R
		[6:1]	pll_vco_ctrim	vco band code	0x0	R
		0	pll_afc_fine enable	PLL fine tuning mode indication 1'b0: coarse adjustment 1'b1: fine adjustment	0x0	R
0x1908	Analog input control	[7:3]	Reserved	Reserved	0x0	R
		2	Analog input DC coupling control	1'b0: AC coupling 1'b1: DC coupling	0x1	R/W
		[1:0]	Reserved	Reserved	0x0	R
0x1910	Input full scale range	[7:4]	Reserved	Reserved	0x0	R
		[3:0]	Input full scale control	4'b0: 2.16Vp-p 4'b1010: 1.44Vp-p 4'b1011: 1.56Vp-p 4'b1100: 1.68Vp-p 4'b1101: 1.80Vp-p 4'b1 110: 1.92Vp-p 4'b1111: 2.04Vp-p	0xD	R/W
0x1A4C	Buffer control 1	[7:6]	Reserved	Reserved	0x0	R
		[5:0]	Buffer control 1	6'b000110: 120uA 6'b001000: 160uA 6'b001010: 200uA 6'b001100: 240uA	0xC	R/W

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Register address	Register name	Bit	Bit name	describe	default value	Access Type
				6'b001110:280uA 6'b010000:320uA 6'b010010:360uA 6'b010100:400uA 6'b010110:440uA		
0x1A4D	Buffer Control 2	[7:6]	reserve	reserve	0x0	R
		[5:0]	Buffer Control 2	6'b000110:120uA 6'b001000:160uA 6'b001010:200uA 6'b001100:240uA 6'b001110:280uA 6'b010000:320uA 6'b010010:360uA 6'b010100:400uA 6'b010110:440uA	0xC	R/W

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19.7 Application Information

19.7.1 Power Supply Recommendations

The CW9694 needs to be powered by the following seven power supplies:

- AVDD1 = AVDD1_SR = 0.975 V
- AVDD2 = 1.8 V
- AVDD3 = 2.5 V
- DVDD = 0.975 V
- DRVDD1 = 0.975V
- DRVDD2 = 1.8 V
- SPIVDD = 1.8 V

If only one 0.975 V power supply is available, connect to AVDD1 first,

Then tap it and use ferrite beads or filter choke Isolate it with a decoupling capacitor AVDD1, DVDD and DRVDD1, sorted in order. Several different decoupling capacitors can be used by users to cover high and low frequencies. These capacitors must be close to the entry point of the PCB board and close to the device, with minimal trace length.

19.7.2 Suggestions for heat dissipation of exposed pads

For optimal electrical and thermal performance, the bare bottom of the ADC must be

The exposed pad is connected to AGND. The exposed continuous copper layer on the PCB should be connected to the exposed pad (pin 0) of the CW9694. There must be multiple vias on the copper layer to obtain the lowest possible thermal resistance path for heat dissipation through the bottom of the PCB. It is recommended that these vias must be filled with solder.

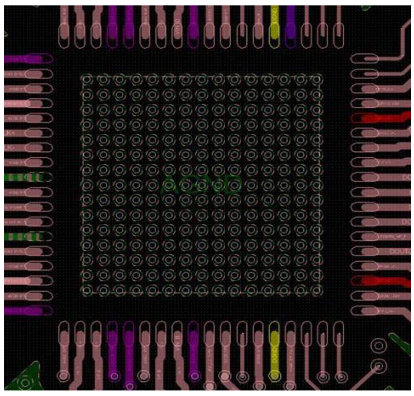

Figure 48 Recommended PCB layout for exposed pad of CW9694

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20.0 Package size

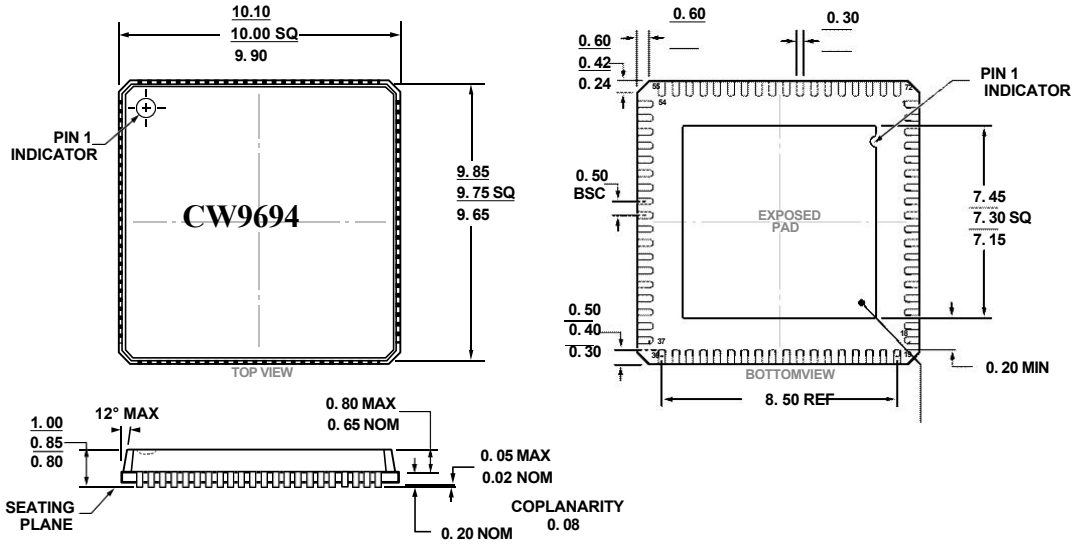

Figure 49 CW9694 QFN72 package outline

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