CW10AQ190A Data Sheet

Four channels 10- Bit , 1.25 GSPS /2.5 GSPS /5 GSPS Ultra-high speed ADC

1.0 Overview

CW10AQ190A is a 10 -bit ultra-high-speed ADC product with four built-in 10-Bit , 1.25GSPS ultra-high-speed ADCs . Each channel ADC has an independent DDR data clock. When multiple channel ADCs are working, You can select any data clock to collect data from several channels at the same time. The chip supports interleaving working mode between channels, two-channel interleaving achieves 2.5GSPS sampling rate, and four-channel interleaving achieves 5GSPS sampling rate.

CW10AQ190A supports AutoSync function and can be used for multi-chip cascading. The product package is EBGA380 package, and the operating temperature is -55 ℃ ~ 125 ℃ . CW10AQ190A achieves excellent dynamic performance with low power consumption below 3.2W .

CW10AQ190A can be programmed into two types: offset binary code and Gray code, and the data is output using an LVDS interface that complies with international standards .

2.0 application

- RF Direct Down Conversion
- High-speed data acquisition system
- Ultra-wideband satellite data reception
- Automatic test equipment
- High speed test equipment

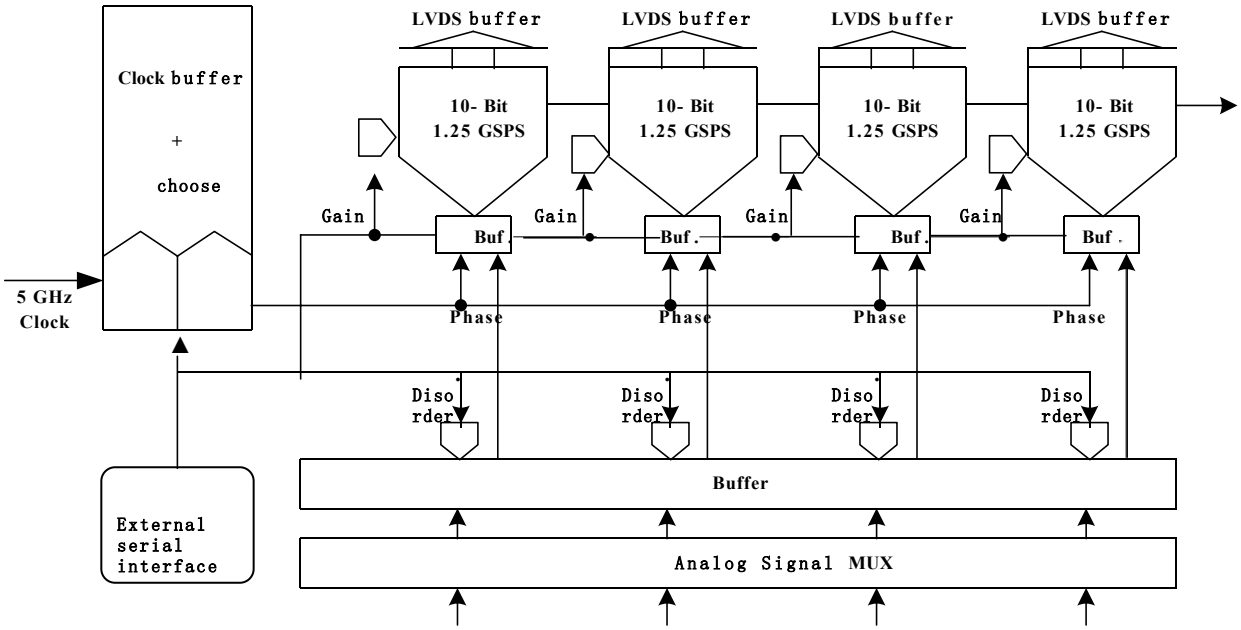
3.0 Features

- Built-in four channels 1.25 GSPS ADC , and can realize interleaving between channels to improve sampling rate
- Low power consumption, no heat sink required
- Built-in terminal resistor (automatic correction), high-speed buffer
- Provides system debugging and batch testing Test Pattern
- Multi-chip automatic synchronization function
- 380- EBGA Package (31 mm ×31 mm ×0.85 mm, 1.27 mm Ball spacing, plane size ≥ 16 mm × 16 mm All can be customized)

4.0 Performance Indicators

- Full power bandwidth: 3.0 GHz
- Data Delay: about 80 Input Clock (*f* MCLK)cycle
- Channel-to-channel isolation (*fs* = 1.25 GSPS , input signal power -1 dBFS):
  - — Aggressor _ 1377 MHz & Victim _870 MHz Crosstalk = - 69dBc
  - — Aggressor_870 MHz & Victim_ 1377 MHz Crosstalk = - 74dBc
- Static performance: DNL - 1.0/ + 1.1 LSB , INL - 1.3/ + 2.6 LSB
- Four - channel Mode Dynamic performance (*fs* = 1.2 5 GSPS , the input signal power makes the output codeword -1 dBFS ）
  - — *fin* = 620 MHz
    ENOB = 7.98 Bits， SFDR = 62.30 dBFS， SNDR = 49.82 dBFS
  - — *fin* = 1200 MHz
    ENOB = 7.83 Bits， SFDR = 60.71 dBFS， SNDR = 48.87 dBFS
- Two - channel Mode Dynamic performance (*fs* = 2.5 GSPS , input signal power makes the output codeword -1 dBFS)
  - — *fin* = 620 MHz
    ENOB = 7.85 Bits， SFDR = 59.25 dBFS， SNDR = 48.99 dBFS
  - — *fin* = 1200 MHz
    ENOB = 7.79 Bits， SFDR = 58.76 dBFS， SNDR = 48.66 dBFS
- One - channel Mode Dynamic performance (*fs* = 5.0 GSPS , the input signal power makes The output codeword is -1 dBFS)
  - — *fin* = 620 MHz
    ENOB = 7.73 Bit, SFDR = 59.5 0 dBFS, SNDR = 48.29 dBFS
  - — *fin* = 1200 MHz
    ENOB = 7.59 Bit, SFDR = 5 5.96 dBFS, SNDR = 47.47 dBFS

5.0 Simplified Block Diagram

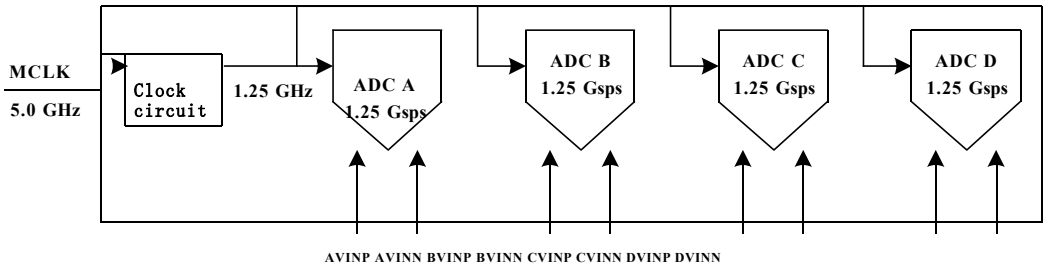


picture 5.1 CW10AQ190A System Block Diagram

5.1 Working Mode

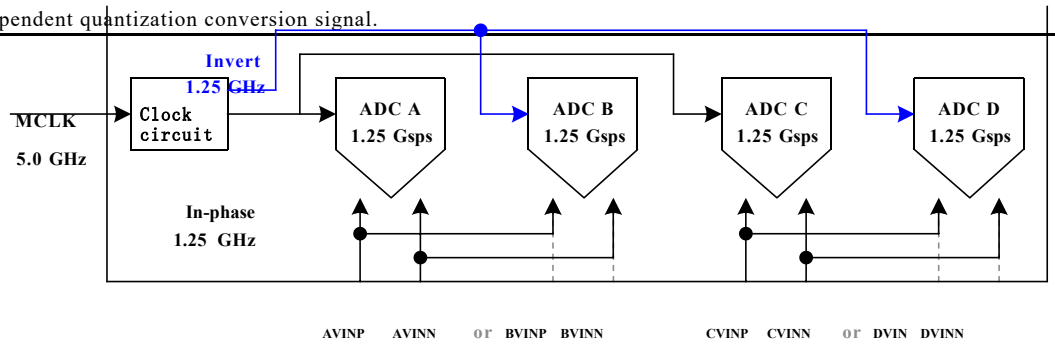
CW10AQ190A supports three working modes: four-channel independent working mode, two-channel interleaved working mode and single-channel interleaved working mode.

- Four-channel independent working mode: four ADC The cores independently input signals and independently quantize and convert the signals.



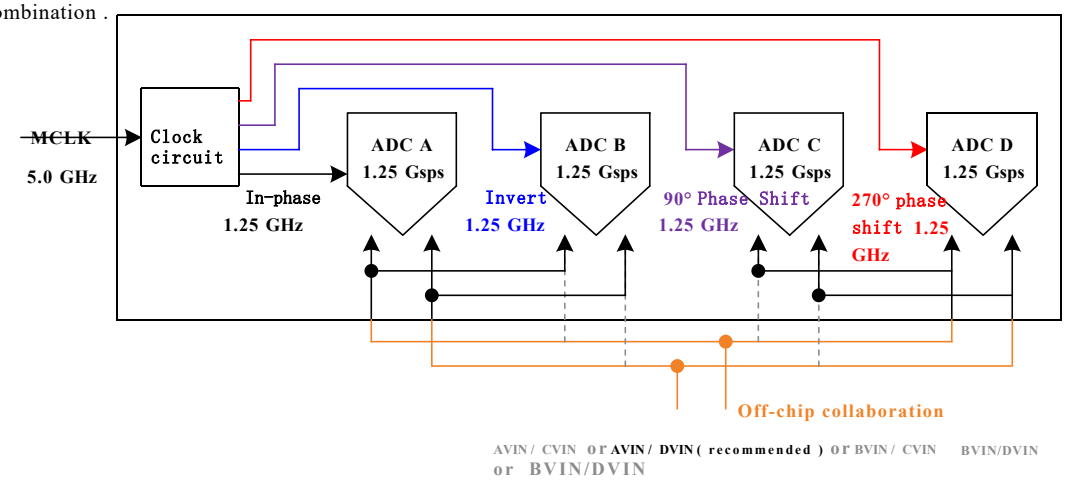
picture 5.2 Four-channel working mode

- Dual-channel interleaved working mode: four ADC In the kernel A and B Interweaving work implementation 2.5 GHz Sampling, C and D Interweaving work implementation 2.5 GHz Sampling, interleaving Two 2.5 GHz Sampling rate ADC Independent input signal, independent quantization conversion signal.

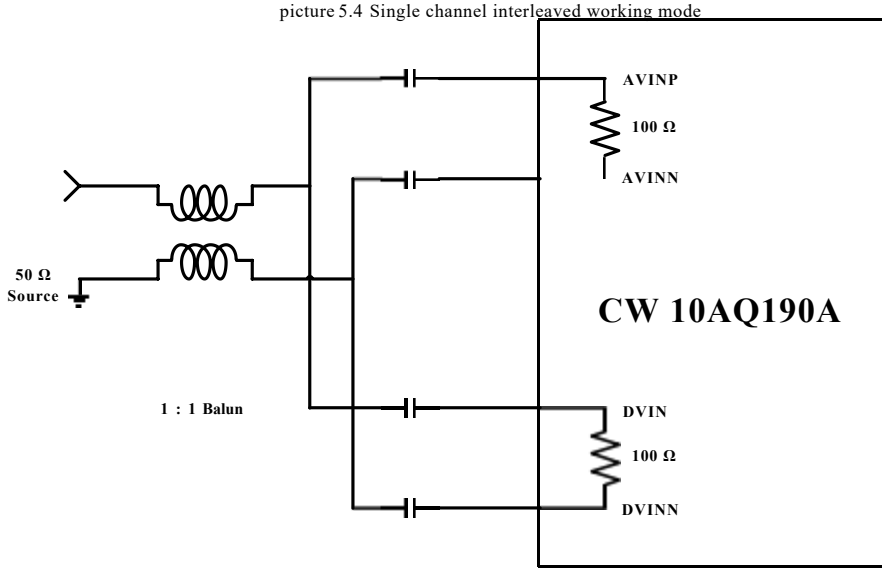


picture 5.3 Dual-channel interleaved working mode

- Single-channel interleaved operation mode: four ADCs Core A/B/C/D interleaving implementation5 GHz For sampling, the signal must be input to port AVIN / CVIN outside the chip . Or AVIN / DVIN (recommended connection) orBVIN / CVIN orBVIN / DVIN Used in combination .



picture 5.4 Single channel interleaved working mode



picture5.5 Single channel interleaved working input signal port joint diagram

6.0 Typical performance

surface 6-1 Chip Usage Conditions

parameter	symbol	Notes	Numeric	unit
Supply voltage	V_{F33}	Analog circuit power supply	3.3	V
	V_{TC18}	Sample and hold and clock circuit power supply	1.8	V
	V_{DR18}	Output drive circuit power supply	1.8	V
	V_{E11}	Digital circuit power supply	1.1	V
Power-on sequence		No power-up sequence required		
land	GND	Chip circuit ground	0	V
Differential input analog signal amplitude	$V_{AVINP} - V_{AVINN}$ $V_{BV} - V_{BVINN}$ $V_{CVINP} - V_{CVINN}$ $V_{DVIN} - V_{DVINN}$	Input signal differential amplitude	800	mVpp
Logic input high	V_{I}		Module power supply voltage	V
Logic input low	V_{IL}		GND	
Clock differential input signal amplitude	$V_{CLKP} - V_{CLKN}$		800	mVpp
Clock frequency	f_{MCLK}		$4 \le f_{MCLK} \le 5$	GHz
Operating temperature range	T_C		$-55 \le T_C \le 125$	℃

surface 6-2 Power supply, input and output electrical characteristics

parameter	symbol	Minimum	Typical Value	Maximum	unit
Resolution			10		
Supply voltage: Analog circuit power supply Sample and hold and clock circuit power supply OutputLVDS Drive circuit power supply Digital circuit power supply	 V_{F33} V_{TC18} V_{DR18} V_{E11}	 3.2 1.75 1.75 1.05	 3.3 1.8 1.8 1.1	 3.4 1.85 1.85 1.15	 V V V V
Supply Current: Analog circuit power supply Sample and hold and clock circuit power supply Output drive circuit power supply Digital circuit power supply	 I_{F33} I_{TC18} I_{DR18} IE_{11}		 87 917 431 423		 mA mA mA mA
Power consumption: Normal operation	P_D		 3.18		 W
Data Entry					
Input differential analog signal amplitude	$V_{AVINP} - V_{AVINN}$ $V_{BV} - V_{BVINN}$ $V_{CVINP} - V_{CVINN}$ $V_{DVIN} - V_{DVINN}$		800		mVpp
Differential input resistance	R_{IN}	90	100	110	Ω
Differential input pin withstand voltage	$V_{XVINP} \setminus V_{XVINN}$	GND - 0.3		$V_{F33} + 0.3$	V
Full Power Bandwidth	FPBW		3.0		GHz
Clock Input					
Clock source type		Differential sine wave			
Clock input differential swing	$V_{CLKP} - V_{CLKN}$	600	800	1000	mVpp
Clock differential input resistance	R_{CLK}	100	100	110	Ω

surface 6-2 Power Supply, Input and Output Electrical Characteristics (Continued)

parameter	symbol	Minimum	Typical Value	Maximum	unit
External clock jitter requirements	Jitter			100	fs
Clock duty cycle requirements	Duty Cycle	48	50	52	%
Multi-chip DCLK_RST Synchronous signal					
Logical compatibility	LVDS (support DC/AC coupling)				
Input Voltage:					
Logic Low	V_{IL_DRST}			1.1	V
Logic High	V_{IH_DRST}	1.4			V
Swing	V_{ID_DRST}		350		mV
Common mode voltage	V_{CM_DRST}		1.20		V
Input resistance	R_{DRST}		100		Ω
Multi-chip RCLK Synchronous signal					
Logical compatibility	LVDS (support DC / AC coupling)				
Input Voltage:					
Logic Low	V_{IL_RCLK}			1.1	V
Logic High	V_{IH_RCLK}	1.4			V
Swing	V_{ID_RCLK}		350		mV
Common mode voltage	V_{CM_RCLK}		1.20		V
Input resistance	R_{RCLK}		100		Ω
SPI					
Low level input voltage	V_{IL_SPI}	0		$0.3 \times V_{F33}$	V
High level input voltage	V_{IH_SPI}	$0.7 \times V_{F33}$		V_{F33}	V
Low level output voltage	V_{OL_SPI}			0.3	V
High level output voltage	V_{OH_SPI}	$0.8 \times V_{F33}$			V
Serial clock frequency	f_{SCLK}		15	20	MHz
Digital signal data and data ready output					
Logical compatibility	LVDS				
Output Amplitude (50Ω Transmission Line , 100Ω differential termination): Swing (one side)	VOD	250	350	450	mVpp
Common mode voltage	V_{CM_LVDS}		1.2		V
Output data delay:					
Four-channel mode: aisle A , B , C , D			70		
Two-channel mode: aisle A , B			72		
aisle C , D	t_{LAT}		70		Enter the master clock cycle
One channel mode: aisle A			73		
aisle B			72		
aisle C			71		
aisle D			70		
Data output rising edge (20 pF)	t_H		220		ps
Data output falling edge (20 pF)	t_{HLT}		220		ps

surface 6-3 Static Characteristics

parameter	symbol	Minimum	Typical Value	Maximum	unit
Differential Nonlinearity	DNL	-1.0		1.1	LSB
Integral Nonlinearity	INL	-1.3		2.6	LSB

surface 6-4 Dynamic Characteristics

parameter	symbol	Minimum	Typical Value	Maximum	unit
Four-channel mode (f_s = 1.25 GSPS, V_{IN} The amplitude makes the output codeword -1 dBFS) Each independent working channel (after calibration)					
Number of effective digits *find* = 620 MHz *find* = 1200 MHz	ENOB		 8.0 7.8		Bit
Signal-to-Noise-Distortion Ratio *find* = 620 MHz *find* =1200 MHz	SNDR		 49.8 48.9		dBFS
Spurious Free Dynamic Range *find* = 620 MHz *find* = 1200 MHz	| SFDR |		 62.3 60.7		dBFS
Two-channel mode (f_s = 2.5 GSPS, V_{IN} The amplitude makes the output codeword -1 dBFS) Two independent working channels (after correction)					
Number of effective digits *find* = 620 MHz *find* = 1200 MHz	ENOB		 7.9 7.8		Bit
Signal-to-Noise-Distortion Ratio *find* = 620 MHz *find* =1200 MHz	SNDR		 49.0 48.7		dBFS
Spurious Free Dynamic Range *find* = 620 MHz *find* = 1200 MHz	| SFDR |		 59.2 58.8		dBFS
One channel mode (f_s = 5.0 GSPS, V_{IN} The amplitude makes the output codeword -1 dBFS) Two independent working channels (after correction)					
Number of effective digits *find* = 620 MHz *find* = 1200 MHz	ENOB		 7.7 7.6		Bit
Signal-to-Noise-Distortion Ratio *find* = 620 MHz *find* =1200 MHz	SNDR		 48.3 47.5		dBFS
Spurious Free Dynamic Range *find* = 620 MHz *find* = 1200 MHz	| SFDR |		 59.5 56.0		dBFS

surface 6-5 Switching Characteristics

parameter	symbol	Minimum	Typical Value	Maximum	unit
Aperture delay + data output delay	$T_{AD}+T_{OD}$		4.9		ns

7.0 Pin Configuration and Function Description

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
AD	GND	VF33 (VCC)	B8P (B8)	B9P (B9)	BORP (BOR)	GND	DIODA	GND (NC)	GND	RCLKP (NC)	DCLK RSTP (SYNCP)	CLKP (CLK)	CLKN	RSV0 (SCAN0)	RSV2 (SCAN2)	SCLK	MOSI	RESA (Res50)	GND	CORP (COR)	C9P (Q9)	C8P (C8)	VF33 (VCC)	GND	AD
AC	GND	VF33 (VCC)	B8N	B9N	BORN	GND	DIODC	GND	VTC18 (VCC)	RCLKN (NC)	DCLK RSTN (SYNCN)	GND	GND	RSV1 (SCAN1)	RSTN	CSN	MISO	RESB (Res62)	GND	CORN	C9N	C8N	VF33 (VCC)	GND	AC
AB	RCOUT 0P (NC)	RCOUT 0N (NC)	VDR18 (VCC)	GND	VTC18 (VCC)	GND	VTC18 (VCC)	GND	GND	VTC18 (VCC)	VTC18 (VCCD)	GND	GND	VTC18 (VCC)	VTC18 (VCC)	GND	GND	VTC18 (VCC)	GND	VTC18 (VCC)	GND	VDR18 (VCC)	RCOUT 1N (NC)	RCOUT 1P (NC)	AB
AA	BRSV 0P (NC)	BRSV 0N (NC)	VDR18 (VCC)	GND	VDR18 (VCCO)	VTC18 (VCC)	VTC18 (VCC)	GND	GND	VTC18 (VCC)	VTC18 (VCCD)	GND	GND	VTC18 (VCC)	VTC18 (VCC)	GND	GND	VTC18 (VCC)	VTC18 (VCC)	VDR18 (VCCO)	GND	VDR18 (VCC)	CRSV 0N (NC)	CRSV 0P (NC)	AA
Y	VE11 (NC)	VE11 (NC)	VDR18 (VCCO)	GND	GND	VDR18 (VCCO)	VTC18 (VCC)	GND	GND	VTC18 (VCC)	VTC18 (VCCD)	GND	GND	VTC18 (VCC)	VTC18 (VCC)	GND	GND	VTC18 (VCC)	VDR18 (VCCO)	GND	GND	VDR18 (VCCO)	VE11 (NC)	VE11 (NC)	Y
W	VE11 (NC)	VE11 (NC)	VDR18 (VCCO)	GND	GND															GND	GND	VDR18 (VCCO)	VE11 (NC)	VE11 (NC)	W
V	VE11 (NC)	VE11 (NC)	GND (NC)	GND (NC)	GND															GND	GND (NC)	GND (NC)	VE11 (NC)	VE11 (NC)	V
U	B7P (B7)	B7N	NC	NC	VDR18 (VCCO)															VDR18 (VCCO)	NC	NC	C7N	C7P (C7)	U
T	B5P (B5)	B5N	B6P (B6)	B6N	GND															GND	C6N	C6P (C6)	C5N	C5P (C5)	T
R	B3P (B3)	B3N	B4P (B4)	B4N	VTC18 (VCC)															VTC18 (VCC)	C4N	C4P (C4)	C3N	C3P (C3)	R
P	B1P (B1)	B1N	B2P (B2)	B2N	GND															GND	C2N	C2P (C2)	C1N	C1P (C1)	P
N	BDCLKP (BDR)	BDCLKN (BDRN)	B0P (B0)	B0N	VTC18 (VCC)															VTC18 (VCC)	C0N	C0P (C0)	CDCLKN (CDRN)	CDCLKP (CDR)	N
M	ADCLKP (ADR)	ADCLKN (ADRN)	A0P (A0)	A0N	VTC18 (VCC)															VTC18 (VCC)	D0N	D0P (D0)	DDCLKN (DDRN)	DDCLKP (DDR)	M
L	A1P (A1)	A1N	A2P (A2)	A2N	GND															GND	D2N	D2P (D2)	D1N	D1P (D1)	L
K	A3P (A3)	A3N	A4P (A4)	A4N	VTC18 (VCC)															VTC18 (VCC)	D4N	D4P (D4)	D3N	D3P (D3)	K
J	A5P (A5)	A5N	A6P (A6)	A6N	GND															GND	D6N	D6P (D6)	D5N	D5P (D5)	J
H	A7P (A7)	A7N	GND (NC)	NC	VDR18 (VCCO)															VDR18 (VCCO)	NC	NC	D7N	D7P (D7)	H
G	VE11 (NC)	VE11 (NC)	GND (NC)	GND (NC)	GND															GND	GND (NC)	GND (NC)	VE11 (NC)	VE11 (NC)	G
F	VE11 (NC)	VE11 (NC)	VDR18 (VCCO)	GND	GND															GND	GND	VDR18 (VCCO)	VE11 (NC)	VE11 (NC)	F
E	VE11 (NC)	VE11 (NC)	VDR18 (VCCO)	GND	GND	VDR18 (VCCO)	VTC18 (VCC)	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VTC18 (VCC)	VDR18 (VCCO)	GND	GND	VDR18 (VCCO)	VE11 (NC)	VE11 (NC)	E
D	ARSV 0P (NC)	ARSV 0N (NC)	VDR18 (VCC)	GND	VDR18 (VCCO)	VTC18 (VCC)	VTC18 (VCC)	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VTC18 (VCC)	VTC18 (VCC)	VDR18 (VCCO)	GND	VDR18 (VCC)	DRSV 0N (NC)	DRSV 0P (NC)	D
C	VF33 (NC)	VF33 (NC)	VDR18 (VCC)	GND	VTC18 (VCC)	VTC18 (VCC)	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VTC18 (VCC)	VTC18 (VCC)	GND	VDR18 (VCC)	VF33 (NC)	VF33 (NC)	C
B	GND	VF33 (VCC)	A8N	A9N	AORN	GND	GND	GND	GND	GND	GND	CMI REFAB	CMI REFCD	GND	GND	GND	GND	GND	GND	DORN	D9N	D8N	VF33 (VCC)	GND	B
A	GND	VF33 (VCC)	A8P (A8)	A9P (A9)	AORP (AOR)	GND	AVINP (AAI)	AVINN (AAIN)	GND	BVINP (BAI)	BVINN (WOMAN)	GND	GND	CVINP (IMF)	CVINN (TAX)	GND	DVINP (DAI)	DVINN (DAN)	GND	DORP (DOR)	D9P (D9)	D8P (D8)	VF33 (VCC)	GND	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	

picture7.1 CW10AQ190A Pinout (1)

NOTE:

(1) When the current version of the chip is in four-channel independent working mode,CVINP / CVINN The input signal is converted fromDx Output; from DVINP / DVINN The input signal is converted fromCx Output. Can be modified through register configuration .

surface 7-1 Pin Function Description

Pin number	symbol	achievement able Description Description
A7 A8	AVINP AVINN	100 Ohm differential input impedance The frequency characteristics of the four wiring groups are highly consistent Differential signal input for each channel
A10 A11	BVINP BVINN	
A14 A15	CVINP CVINN	
A17 A18	DVIN DVINN	
AD 12 AD 13	CLKP CLKN	Differential sampling clock (f_{CLK}) signal input, AC Coupling , signal frequency5GHz 100 Ohm differential input impedance
AD 11 AC 11	DCLKRSTP DCLKRSTN	Differential reset clock signal Differential positive pulse resetXDCLKP / XDCLKN
AD 10 AC 10	RCLKP RCLKN	Multi-chip cascade synchronization reference clock input, frequency is f_{CLK}/40 supportDC / AC coupling
H4	NC	Floating feet,Do not connect any potential
U4	NC	Floating pin, can not be connected to any potential
U21	NC	Floating pin, can not be connected to any potential
H21	NC	Floating pin, can not be connected to any potential
U3	NC	Floating pin, can not be connected to any potential
U22	NC	Floating pin, can not be connected to any potential
H22	NC	Floating pin, can not be connected to any potential
B12	CMIREFAB	CHA andCHB aisleADC The common-mode voltage of the analog signal input terminal , DC Use when coupling
B13	CMIREFCD	CHC andCHD aisleADC The common-mode voltage of the analog signal input terminal , DC Use when coupling
AD 18	RESA	The positive terminal of the external reference resistor interface is connected toRESB Pins are used together, connect 1 k Ohm /0.1% reference resistor
AC 18	RESB	External reference resistor interface negative terminal, and RESA Pins are used together,connect 1 k Ohm /0.1% reference resistor
AC 15	RSTN	SPI Control register reset pin, L is valid (logic level3.3 V ）
AC 16	CSN	SPI Chip select signal,L is valid (logic level3.3 V ）
AD 16	SCLK	SPI Serial Clock (Logic Level3.3 V ）
AD 17	MOSI	SPI Serial data input (logic level3.3 V ）
AC 17	MISO	SPI Serial data output (logic level 3.3 V)
AD 7	DIODA	Temperature diode anode end
AC 7	DIODC	Temperature diode cathode end

surface7-1 Pin Function Description (Continued)

Pin number	symbol	achievement able Description Description
A2/A23/B2/B23/C1/C2/C23/ C24/ AC 2/ AC 23/ AD 2 / AD 23	VF 33	3.3V analog power supply
C5/C6/C19/C20/D6/D7/D18/ D19/E7/E18/K5/K20/M5/ M20/N5/N20/R5/R20/Y7/ Y10/Y11/Y14/Y15/Y18/ AA 6/ AA 7/ AA 10/ AA 11/ AA 14/ AA 15/ AA 18/ AA 19/ AB 5/ AB 7/ AB 10/ AB 11/ AB 14 / AB 15/ AB 18/ AB 20/ AC 9	VTC 18	1.8V analog power supply
C3/C22/D3/D5/D20/D22/E3/ E6/E19/E22/F3/F22/H5/H20/ U5/U20/W3/ W22/Y3/Y6/Y19 /Y22/ AA 3/ AA 5/ AA 20 / AA 22/ AB 3/ AB 22	VDR 18	1.8V outputDriver power supply
E1/E2/E23/E24/F1/F2/F23/ F24/G1/G2/G23/G24/V1/V2/ V23/V24/W1/ W2/W23/W24/ Y1/Y2/Y23/Y24	VE 11	1.1V digital encoding circuit power supply
A1/A6/A9/A12/A13/A16/A19 /A24/B1/B6~B11/B14~B19/ B24/C4/C7~C18/C21/D4/ D8~D17/D21/E4/E5/E8~E17/ E20/E21/F4/F5/F20/F21 / G3~G5/G20~G22/H3/J5/J20/ L5/L20/P5/P20/T5/T20/ V3~V5/V20~ V22/W4/W5/ W20/W21/Y4 /Y5/Y8/Y9/Y12 /Y13/Y16/Y17 /Y20/Y21/ AA 4 / AA 8/ AA 9/ AA 12/ AA 13/ AA 16/ AA 17/ AA 21/ AB 4/ AB 6 /AB8/AB9/AB12/AB13/AB16 /AB17/AB19/AB21/AC1/ AC6/AC8/AC12/AC13/ AC19/AC24/AD1/AD6/AD8/ AD 9/ AD 19/ AD 24	GND	Chip " ground "
AB 1	RCOUT 0P	Cascade reference clock output, frequency is $f_{CLK}/40$, output to the next stage cascade ADC of RCLK The two pairs of cascade clocks are the same and can be provided to the subsequent cascades separately ADC
AB 2	RCOUT 0N	
AB 24	RCOUT 1P	
AB 23	RCOUT 1N	
AD 14	RSV 0	Empty feet
AC 14	RSV 1	
AD 15	RSV 2	

surface7-1 Pin Function Description (Continued)

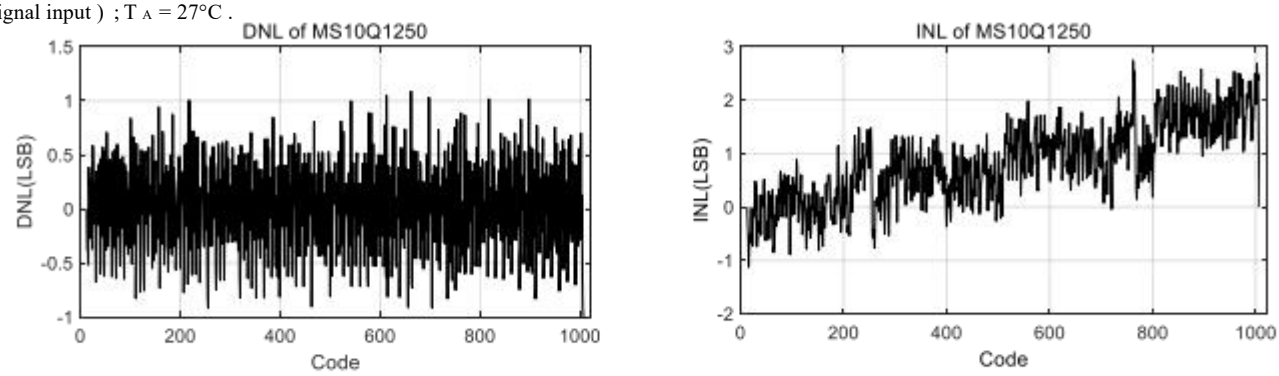
Pin number	symbol	achievement able
M1 M2	ADCLKP ADCLKN	CHA aisle ADC ofLVDS Data Clock
A5 B5	AORP AORN	CHA aisleADC Over-range output
A4 B4	A9P A9N	CHA aisleADC Data output
A3 B3	A8P A8N	
H1 H2	A7P A7N	
J3 J4	A6P A6N	
J1 J2	A5P A5N	
K3 K4	A4P A4N	
K1 K2	A3P A3N	
L3 L4	A2P A2N	
L1 L2	A1P A1N	
M3 M4	A0P A0N	
D1 D2	ARSV 0P ARSV 0N	Reserve PIN , test mode use
N1 N2	BDCLKP BDCLKN	CHB aisle ADC ofLVDS Data Clock
AD 5 AC 5	BORP BORN	CHB aisleADC Over-range output
AD 4 AC 4	B9P B9N	CHB aisleADC Data output
AD 3 AC 3	B8P B8N	
U1 U2	B7P B7N	
T3 T4	B6P B6N	
T1 T2	B5P B5N	
R3 R4	B4P B4N	
R1 R2	B3P B3N	
P3 P4	B2P B2N	
P1 P2	B1P B1N	
N3 N4	B0P B0N	
AA1 AA2	BRSV0P BRSV0N	Reserve PIN , test mode use

surface7-1 Pin Function Description (Continued)

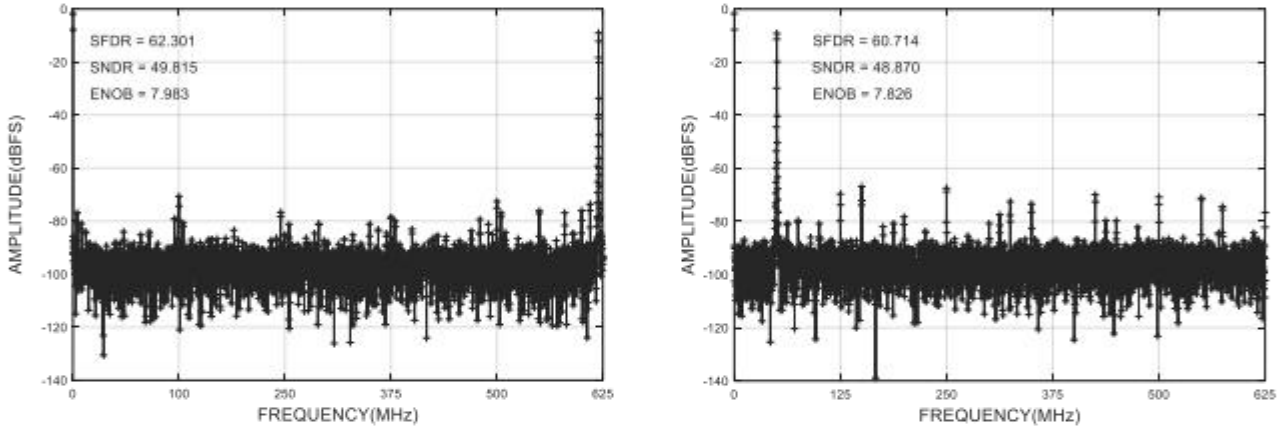
Pin number	symbol	achievement able
N24 N23	CDCLKP CDCLKN	CHC aisle ADC ofLVDS Data Clock
AD 20 AC 20	CORP CORN	CHC aisleADC Over-range output
AD 21 AC 21	C9P C9N	CHC aisleADC Data output
AD 22 AC 22	C8P C8N	
U24 U23	C7P C7N	
T22 T21	C6P C6N	
T24 T23	C5P C5N	
R22 R21	C4P C4N	
R24 R23	C3P C3N	
P22 P21	C2P C2N	
P24 P23	C1P C1N	
N22 N21	C0P C0N	
AA 24 AA 23	CRSV 0P CRSV 0N	Reserve PIN , test mode use
M24 M23	DDCLKP DDCLKN	CHD aisle ADC ofLVDS Data Clock
A20 B20	DORP DORN	CHD aisleADC Over-range output
A21 B21	D9P D9N	CHD aisleADC Data output
A22 B22	D8P D8N	
H24 H23	D7P D7N	
J22 J21	D6P D6N	
J24 J23	D5P D5N	
K22 K21	D4P D4N	
K24 K23	D3P D3N	
L22 L21	D2P D2N	
L24 L23	D1P D1N	
M22 M21	D0P D0N	
D24 D23	DRSV 0P DRSV 0N	Reserve PIN , test mode use

8.0 Typical performance test curve

The following performance indicators are all after chip calibration, and the power supply voltage is typical value, AC Coupled signal input, f_{in} The input amplitude makes the output codeword be -1 dBFS . Channel Termination " AC Ground", AC Coupled sine wave sampling clock, f_{MCLK} = 5 GHz at 0.8 Vpp (i.e. the sampling rate of each channel in four-channel mode is f_s = 1.25 GHz , two-channel mode The sampling rate of each channel is f_s = 2.5 GHz , sampling rate f_s for one channel mode = 5.0 GHz) ; RESA and RESB Connect a resistor between 1000Ω ± 0.1% ; Input signal source impedance 50Ω (Single-ended signal through Balun Module to differential signal input) ; T_A = 27°C .

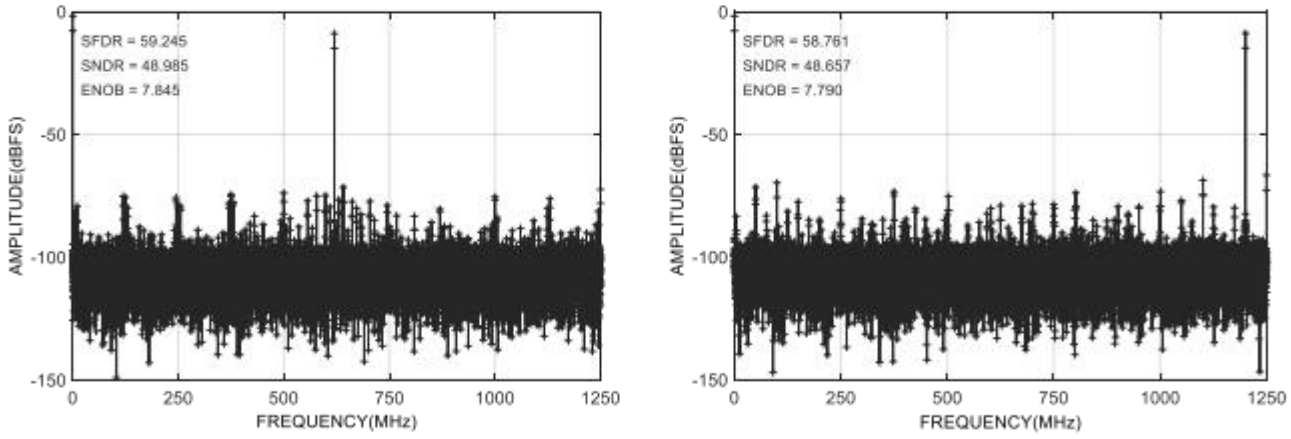


picture 8.1 CW10AQ190A linear error test curve



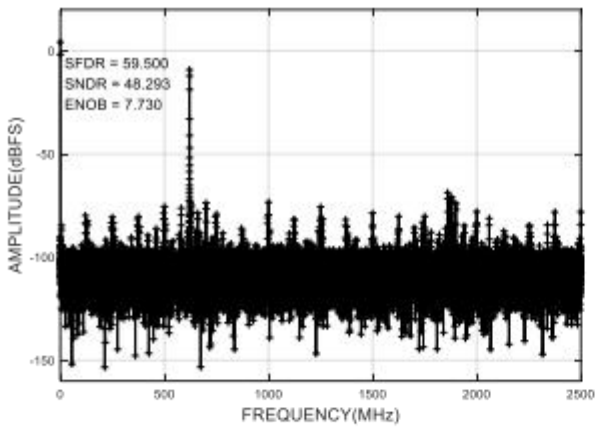
(a) *fin* = 620 MHz (b) *fin* = 1200 MHz

picture 8.2 CW10AQ190A dynamic characteristics test spectrum (four-channel mode: f_s = 1.25 GHz)

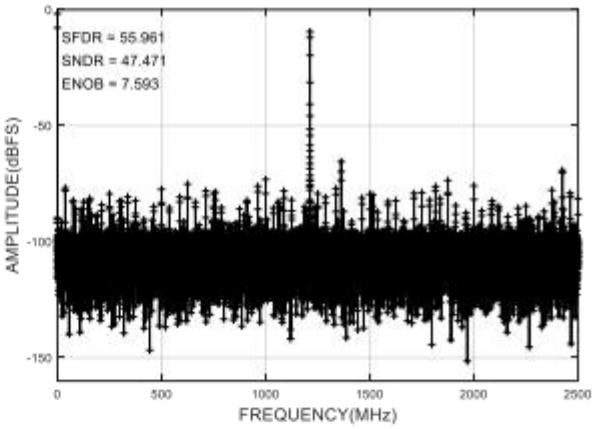


(a) *fin* = 620 MHz (b) *fin* = 1200 MHz

picture 8.3 CW10AQ190A dynamic characteristics test spectrum (two-channel mode: f_s = 2.5 GHz)

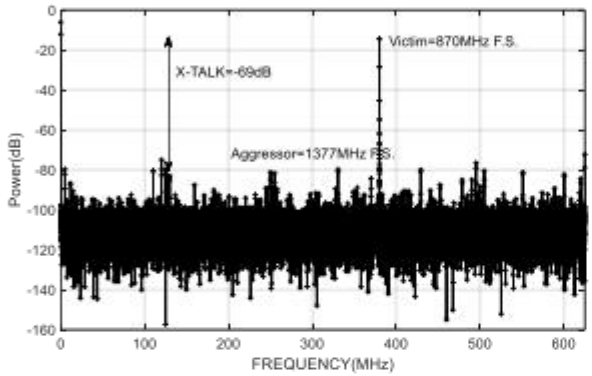


(a)*fin* = 620 MHz

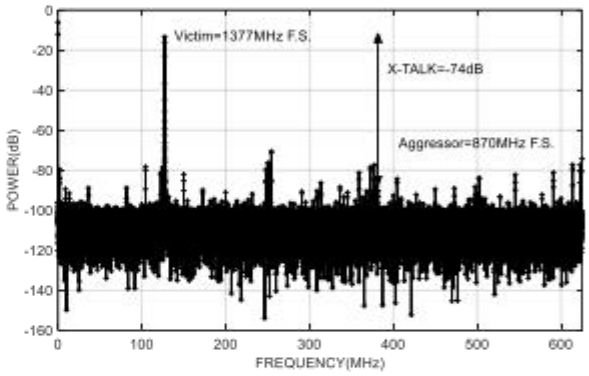


(b) *fin* = 1200 MHz

picture 8.4 CW10AQ190A dynamic characteristics test spectrum (one channel mode: f_s = 5.0 GHz)

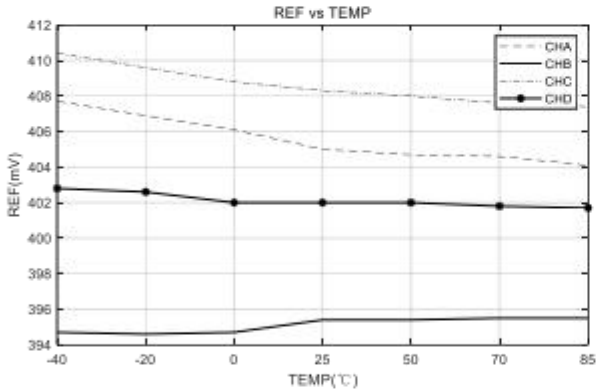


(a) Aggrossor _1377 MHz & Victim _870 MHz

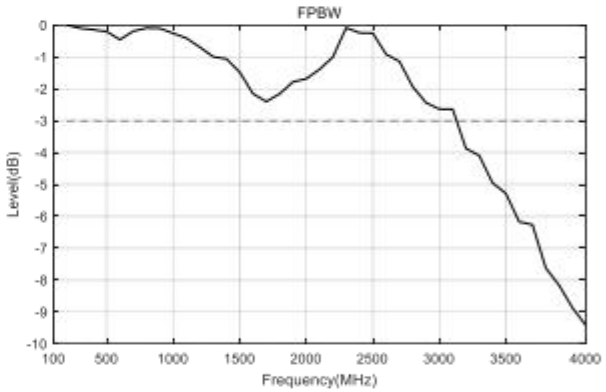


(b) Aggressor _870 MHz & Victim _137 7 MHz

picture 8.5 CW10AQ190A dynamic characteristics test spectrum (four-channel mode: f_s = 1.25 GHz)



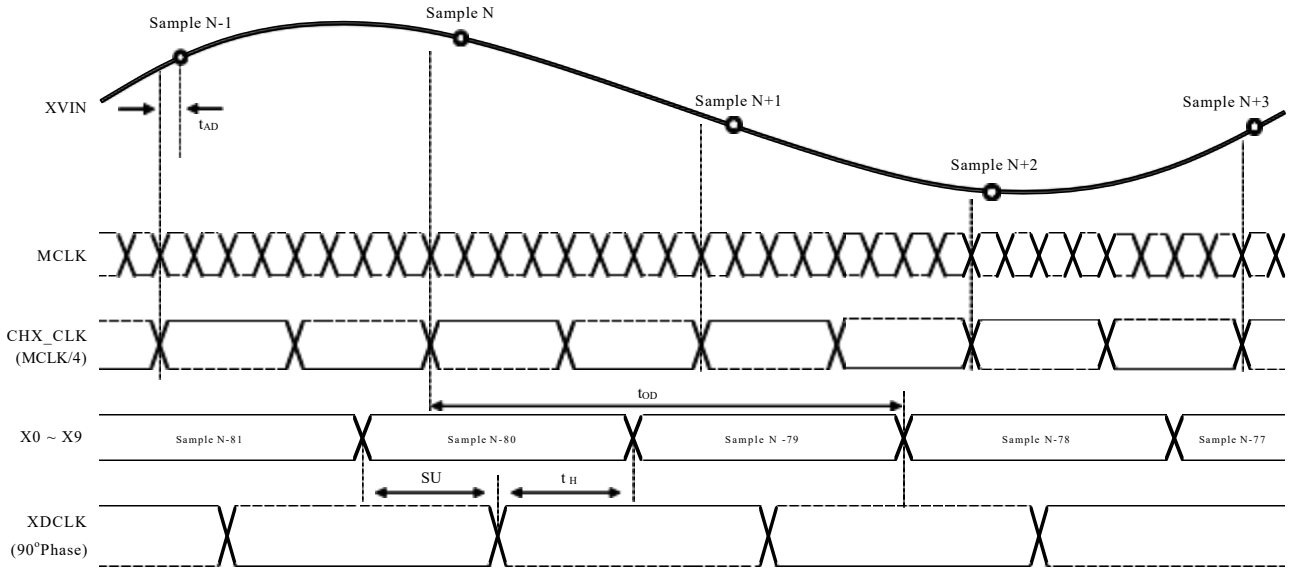
picture 8.6 CW10AQ190A reference temperature curve



8.7 CW10AQ190A Full Power Bandwidth

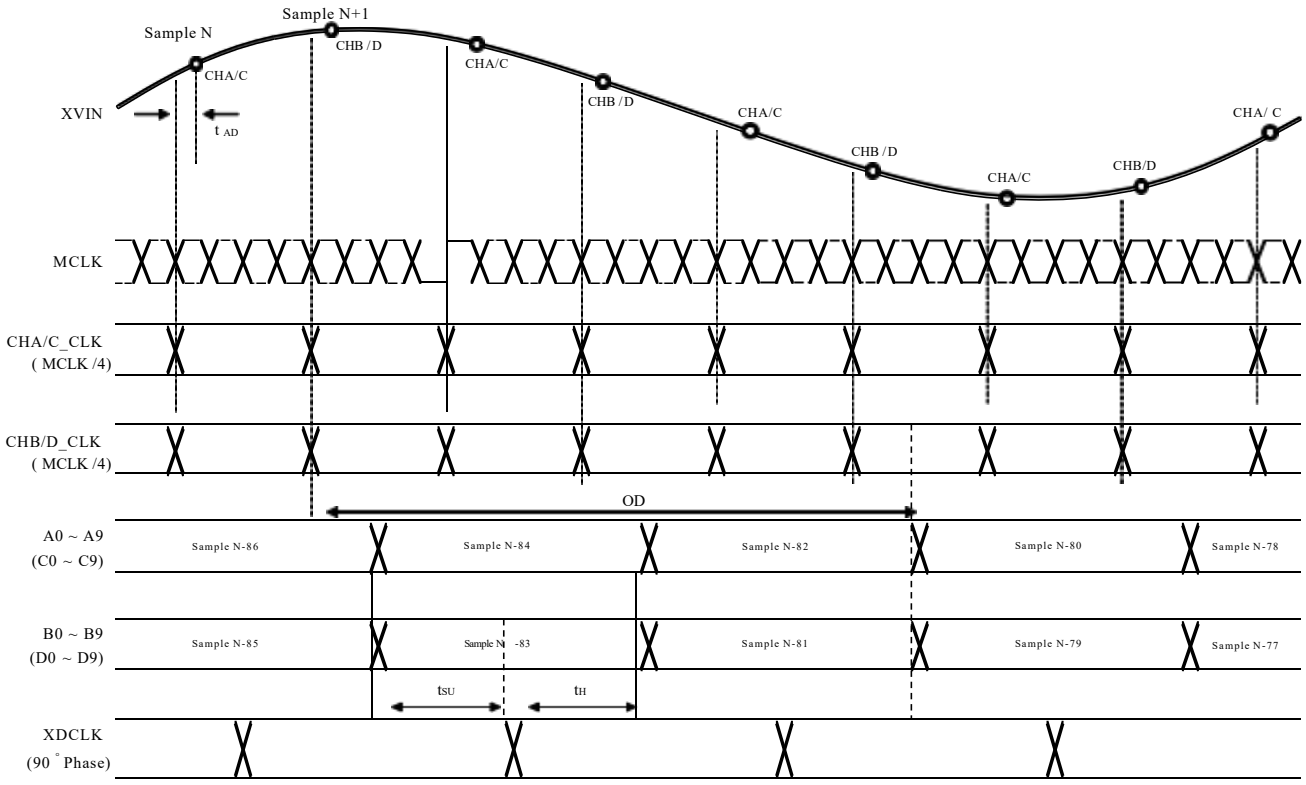
9.0 Timing diagram

9.1 Data Timing



picture9.1 CW10AQ190A data timing in four-channel independent working mode

NOTE : CHA / CHB / CHC / CHD Channel data timing is completely consistent



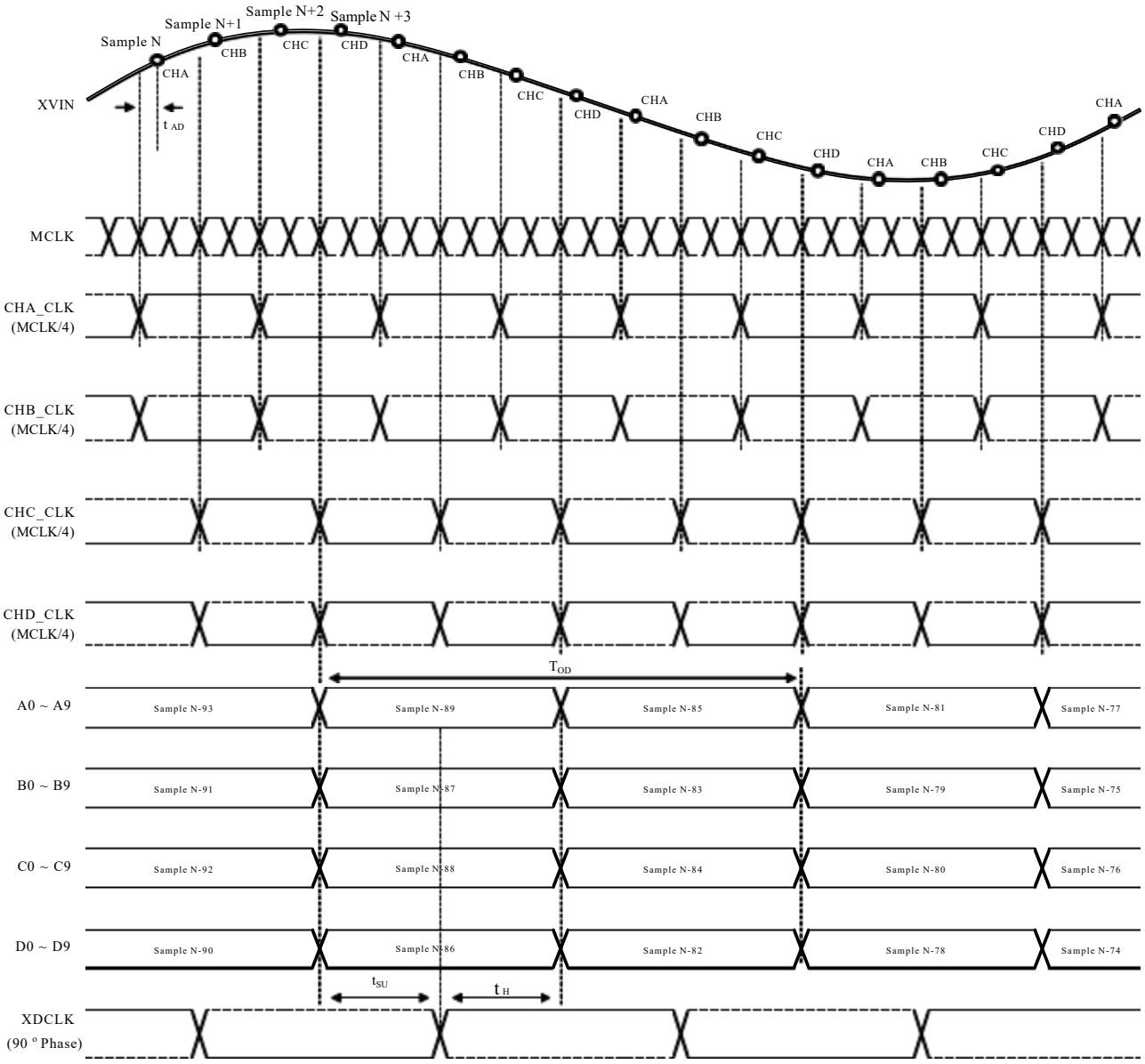
picture9.2 CW10AQ190A data timing in dual-channel interleaved working mode

NOTE : In this mode, A/B The input signal of the interleaved channel can be selected from CHA or CHB Input, C/D interleaved channel input signal can be selected from CHC or CHD enter ;

The internal clock of the channel is CLK The rising edge sampling of CHA_CLK (CHC_CLK) and CHB_CLK (CHD_CLK) inverted ;

A channel (C channel) output delay 80 Cycles (f_{MCLK}), B channel (D channel) output delay 78 Cycles (f_{MCLK});

Data in DCLK Double-edge output, the time sequence is Ax (Cx), Bx (Dx) ($F_{XDCLK} = 1/4\ F_S = 1/8\ F_{MCLK}$)



picture9.3 CW10AQ190A data timing in single channel interleaved working mode

NOTE : In this mode, the input signals of A/B/C/D interleaved channels must be simultaneously CHA + CHC , or CHA + CHD , or CHB + CHC , or CHB + CHD enter,

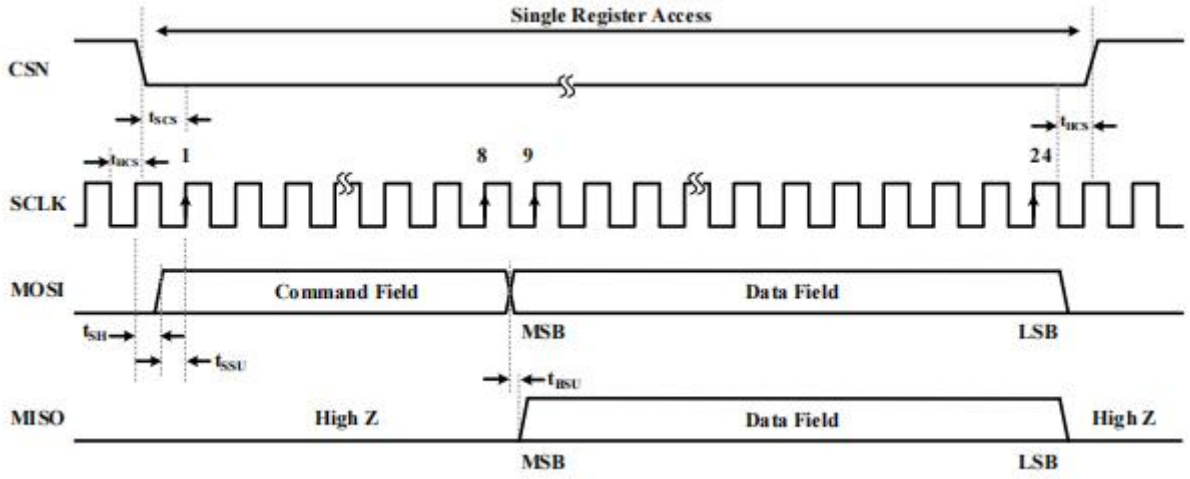
The internal clock of the channel is CLK The rising edge sampling, CHA_CLK, CHC_CLK, CHB_CLK and CHD_CLK The angles are 90 ° apart from each other ;

A channel output delay 81 Cycles (f MCLK), B channel output delay 79 Cycles (f MCLK), C channel output delay 8 0 Cycles (f MCLK), D

Channel Output Delay 78 Cycles (f MCLK);

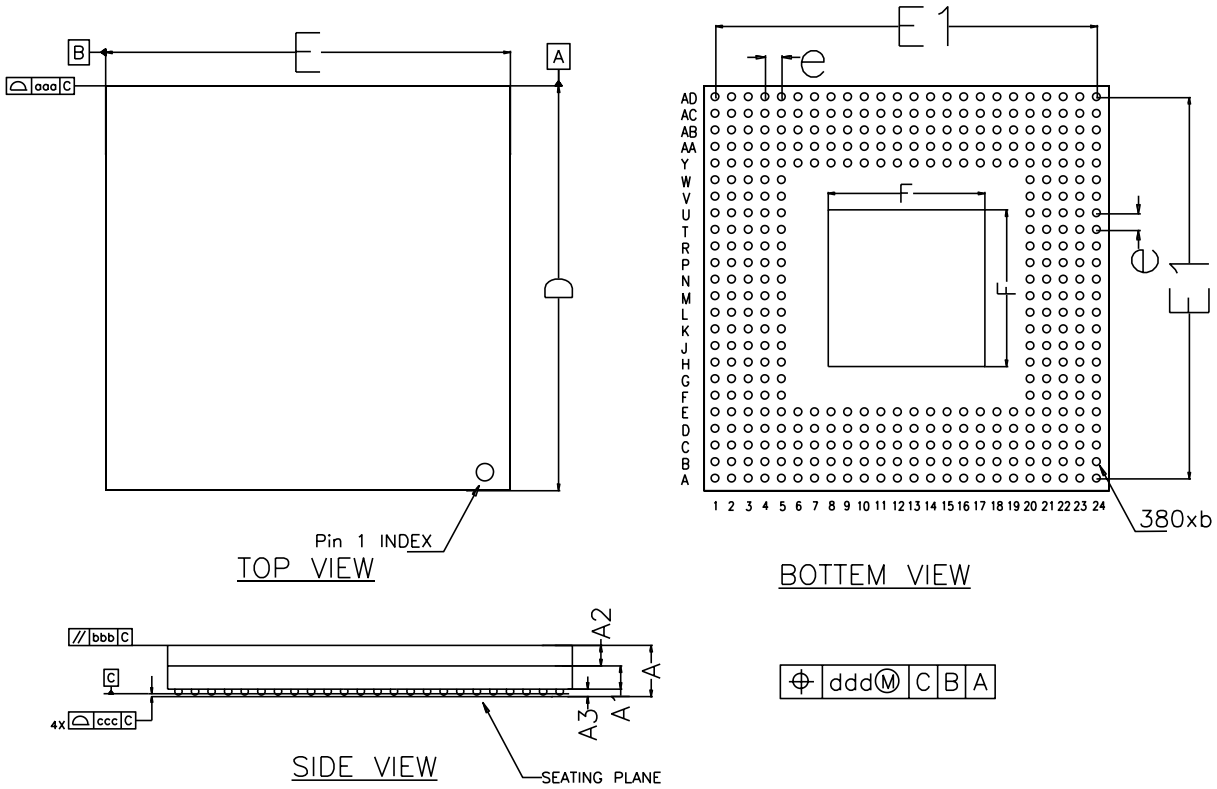
Data in DCLK Double-edge output, the time sequence is Ax, Cx, Bx, Dx (F XDCLK = 1/8 F S = 1/8 F MCLK)

9.2 SPI Interface Timing



picture9.4 CW10AQ190A SPI Read and write timing

10.0 Packaging Information



picture 10.1 CW10AQ190A Package Outline

surface 10.1 CW10AQ190A Package Dimensions (mm)

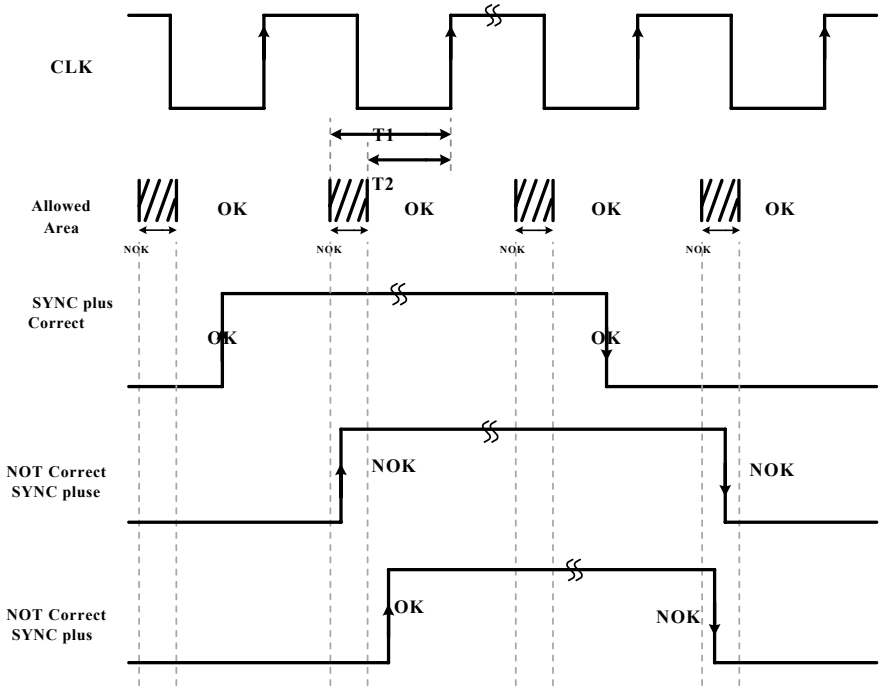
Symbol	MIN	TYP	MAX
A	1.33	1.48	1.63
A1	0.32	0.36	0.4
A2	-	0.5	-
A3	0.57	0.62	0.67
D	-	31	-
E	-	31	-
F(1)	12.2	12.5	12.8
D1	-	29.21	-
E1	-	29.21	-
e	-	1.27	-
b	0.71	0.76	0.81
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-

NOTE:

(1) Here, the chip is actually made of injection molding material. No grounding or heat sinking is required.

11.0 Multi-chip synchronization function

CW10AQ190A has two synchronous multiADCs Chip functions - AutoSync (with independent intellectual property rights) andDCLK Reset (with E2V Company ProductsSYNC Similar functionality).AutoSync A function is a piece ofCW10AQ190A chip isMaster ADC , othersCW10AQ190A chip isSlave ADC muchADC Chip synchronization function . DCLK Reset Function can be completed withAutoSync The sameADC Chip synchronization is the "first generation" multi- chip synchronization solution, which has strict requirements on the timing of use, as shown in the figure 11.1 , **it is not recommended** .



picture 11.1 DCLK Reset Synchronous function timing requirements

ifAutoSync andDCLK Reset The function is not used. It is recommended to use the following table to change the unused PINs. to connect.

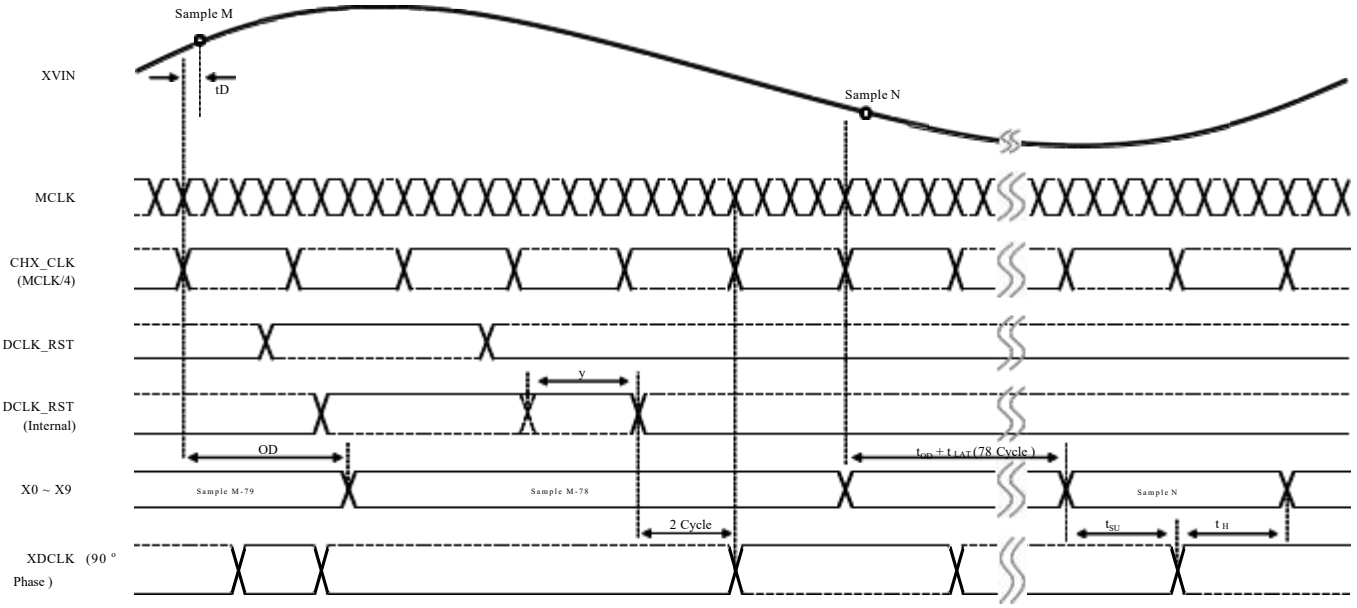
surface 11.1 CW10AQ190A not usedAutoSync andDCLK Reset FunctionPINs Connection suggestions

PINs	Unused terminatio n
RCLKP	Connect to GND via a 1kΩ resistor
RCLKN	Connected to VTC18 via a 1kΩ resistor.
RCOUT 0P/N	Floating
RCOUT 1P/N	Floating
DCLKRSTP	Connect to GND via a 1kΩ resistor
DCLKRSTN	Connected to VTC18 via a 1kΩ resistor.

11.1 DCLK Reset Synchronous function (not available for CW10AQ190A)

DCLK Reset The synchronization function relies on receiving synchronization pulse signals to achieve multipleADC Chip synchronization.DCLK_RSTP andDCLK_RSTN haveLVDS Electrical characteristics, reset logic high (DCLK_RSTP - DCLK_RSTN > 0) is effective. To ensure normal operation,The pulse width should last at leastT_{SYNC} This pair of differential signals is used for internal synchronization of the chip and can beSPI controlSYNC Registers to expand internalSYNC The duration of the signal to synchronize more chips , This extension time can be3 ~ 66 sampling clock cycles to choose from.

DCLK Reset samestepachievementableofhoursequencespecial LevylikeDownpicturePlaceShow, when port DCLK _ RST SignalApulling high (DCLK_RSTP - DCLK_RSTN > 0) , the internal DCLK_RST letterNumberthroughPassoneparthourbetweenbackFollowRight nowpullhigh,and AccessiblePassControl SYNC sendliveDevice(landsite:06h ） Willhighelectricityflataccording toneedwantExtensionDisplay MCLK cycle,at this timedataFollow the roadClock XDCLK quiltpullLow,numberaccording toSaveholdforNo. M-78 Sampling pointsofchangeChange quantitychangecodeCharacter.When the DCLK_RST signalreleaseput,AfterwardsInternal DCLK _ RST letterNumberelectricityflatpullLow (DCLK _ RSTP - DCLK_RSTN < 0) afterAgaingo throughTwo MCLK weekExpectofExtensionLate, dataFollow the roadClock XDCLK open beginningjustoftenturnchange.thishour,existaislePickSamplehourClock CHX _ CLK ofDownoneindivualsuperiorLiftalongPickSampleof numberaccording to（ Sample N),byPassoneparthourbetweenofExtensionLate（ OD + t_{LAT} ）back,Its transferChangequantitychangecodeCharacter（ X0 ~ X9 ） startloseout.On DCLK Resetprocessmiddle,aislePickSampleClock CHX _ CLK normalworkdo.

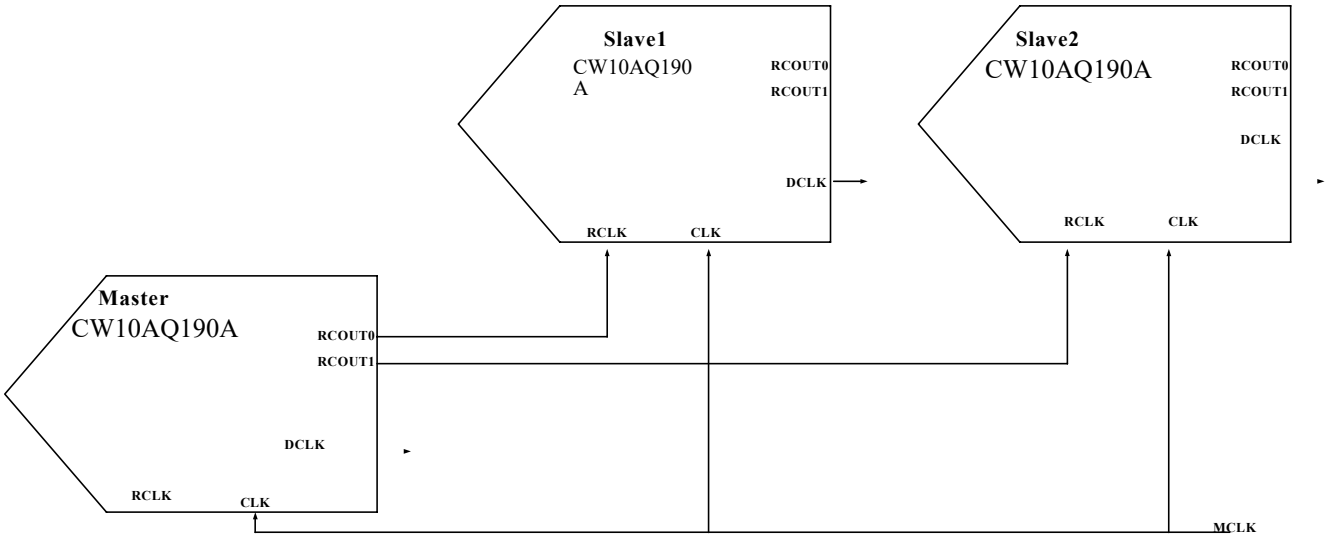


picture 11.2 DCLK Reset Timing of synchronization function in four-channel working mode

11.2 AutoSync Synchronization function (CW10AQ190A does not recommend using the master-slave mode AutoSync Function)

AutoSync The synchronization function can be used for multiple The CW10AQ190A chip performs continuous synchronization. This function allows Slave ADCs The output data and DCLK Synchronize to one Master ADC . This function has the following advantages: no special synchronization pulse is required; any disturbance in the synchronization process will be corrected at the next DCLK Cycle recovery; Master / Slave The CW10AQ190A can be connected in a binary tree format so that any disturbance can be quickly removed from the synchronous system.

The following figure shows a Master ADC and two Slave ADC Synchronous example, where DCLKA /B /C/D No distinction is made. All DCLK express.



picture 11.3 Use Autosync Function synchronization of multiple chips ADC (Master - Slave Mode

To synchronize multiple chips ADCs of DCLK (including data), DCLKs must flip at the same time. CW10AQ190A DCLK Internal RCLK Generate and pass CLK Retiming, therefore, requires synchronization ADCs of CLK The signals are in phase at the same time, that is, MCLK arrive CW10AQ190A timing is consistent. If fine-tuning is required ADC The sampling time tD, which can enable the chip tD Fine-tuning function (24h register, 30 fs / step), the chip can be enabled when the adjustment step is large tD Coarse adjustment function (50h register, 20 ps / step). Master ADC output RCOUT The frequency is MCLK of 1/40 , relaxed SLAVE ADCs of RCLK Wiring requirements. Master ADC Output RCOUT relatively MCLK The delay has a temperature drift of about 20 ps /10 ℃, so it is not recommended to use the master-slave mode AutoSync Function.

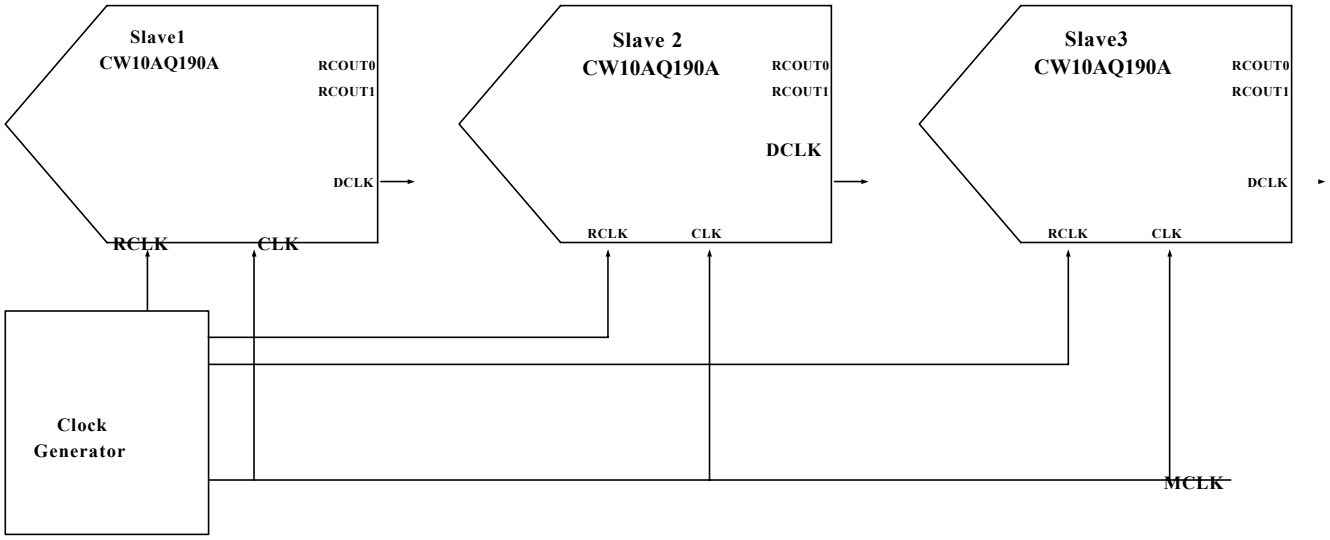
AutoSync The synchronization function must be enabled through the control register configuration, see Section 12 for details. Chapter Register List .

Autosync The function operates by placing a ADC Configured as Master mode, all other ADC Configured as Slave mode, Slave ADC of DCLK quilt Master ADC of DCLK Synchronous. Master ADC Generates and outputs a reference clock RCLK Give multiple Slave ADC to control multiple Slave ADC of DCLK The phase of As shown in Figure 11.3 .ADC Can be configured as Master ADC or Slave ADC ; by default Master ADC . Each ADC Up to two reference clocks can be provided , RCOut 0 and RCOut 1 , used to control Slave ADC Phase. RCOut 0 and RCOut 1 The default is off, and when on, it outputs a frequency of MCLK /40 square wave.

Configuration Autosync system, for each Slave ADC , requires each RCLK can be correctly captured by the master clock (MCLK) (i.e. the master clock sampling RCLK Metastable

state, you can useAutosync ofDRC Control word movementRCLK to avoid metastable states when being sampled). ADC Using Autosync ofSP Control word from 8 possibleDCLK Mutually bit (data phase followsDCLK Phase synchronization changes)Select the correct one. For example, to configureAutosync Functionality and VerificationDCLK Synchronous, must useFPGA View ObservationMaster ADC ofDCLK and allSlave ADC ofDCLK .ConfigurationAutosync When configuring a system, only one subsystem needs to be configured, and other subsystems (the environment is consistent In this case, if the same layout and routing is used,RCLK paths, trace lengths, etc.) can all use the same configuration.

Another option is toADC Configured asSlave mode and drive them externallyRCLK . In this case, a clock generator is needed to power allSlave ADCs Provide a reference clock and select anySlave ADC ofDCLK As a "synchronization benchmark", otherSlave ADCs ofDCLK " Align" with it.



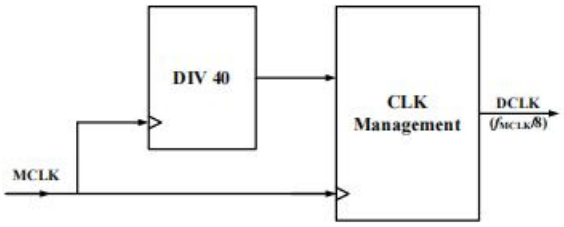
picture 11.4 UseAutosync Function synchronization of multiple chipsADC （ All operating in Slave Mode

Autosync Comparison of solutionsDCLK The reset (DCLK_RST) scheme has significant advantages :

surface 11.2 Autosync Synchronize withDCLK_RST Reset Synchronous Comparator

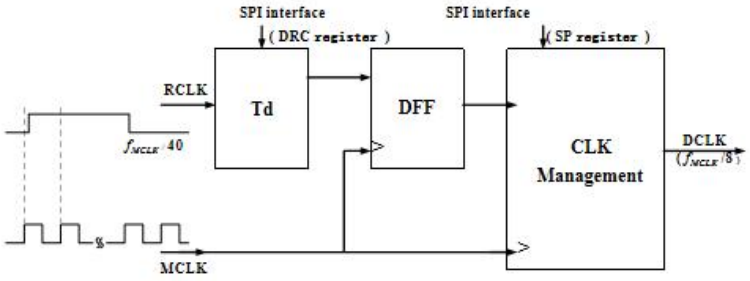
Autosync	**DCLK _ RST reset synchronization**
The system automatically recovers from a loss of synchronization , such as a power failure, without explicit detection . Because Autosync is always running, any DCLK phase error is quickly eliminated by the system.	If the DCLK phase of an ADC drifts, resynchronizing the ADC is only possible with an additional reset pulse if the loss of synchronization is explicitly detected at the system level .
RCLK does not require precise setup and hold times because it is generated by the ADC and configured in the control feedback loop .	The DCLK_RST reset pulse requires precise setup and hold times .
The system configuration has a certain degree of flexibility. The reference clock can be configured as a binary tree, Daisy chain or standalone source.	There is only one system configuration. The DCLK reset pulse must arrive at the same time to each ADC , similar to the sampling clock.
One system configuration applies to all subsystems that are identical.	be synchronized via the DCLK_RST pulse at power - up. step.

Master Mode, ADC This will generate a frequency of *f*MCLK /40 The internal reference clock,It is related to the sampling clockMCLK Synchronous, while generating a frequency of *f*MCLK /8 Data Associative Clock DCLK Output. The simplified working diagram is shown below.



picture 11.5 Master ADC produceDCLK

Slave Mode, ADC It does not generate its own reference clock, but uses the phaseRCLK andSP Control word controlledMCLK Produced together with the clock management unit 40 The divided internal reference clock is shown in the figure 11.6 Therefore,Slave ADC ofDCLK andMaster ADC ofDCLK In phase. At the same time,This reference clock is connected to the inputRCLK has a fixed phase relationship. Td is an adjustable analog delay module used to achieve the optimalRCLK relativelyMCLK Setup and hold time for sampling .

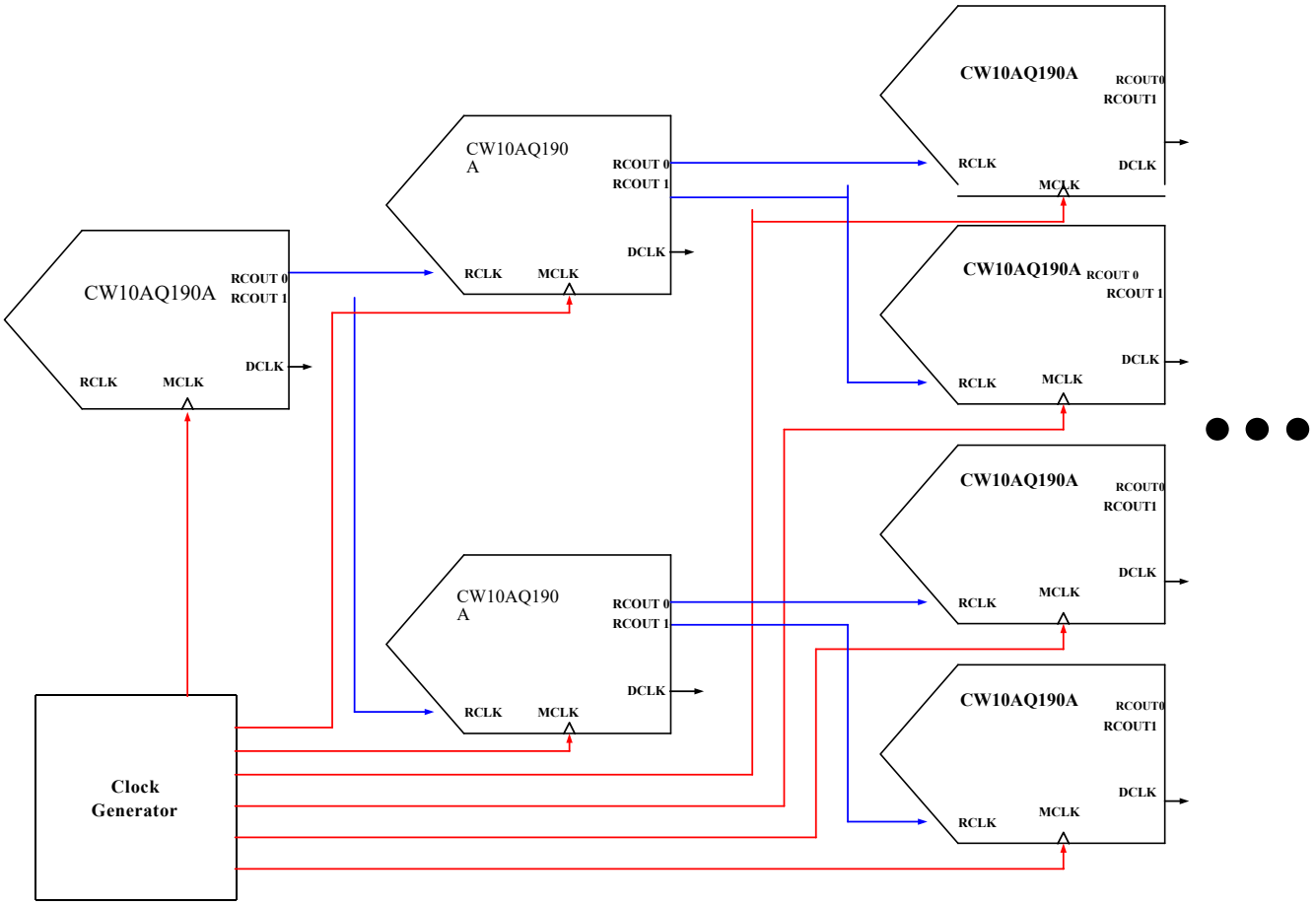


picture 11.6 Slave ADC produceDCLK

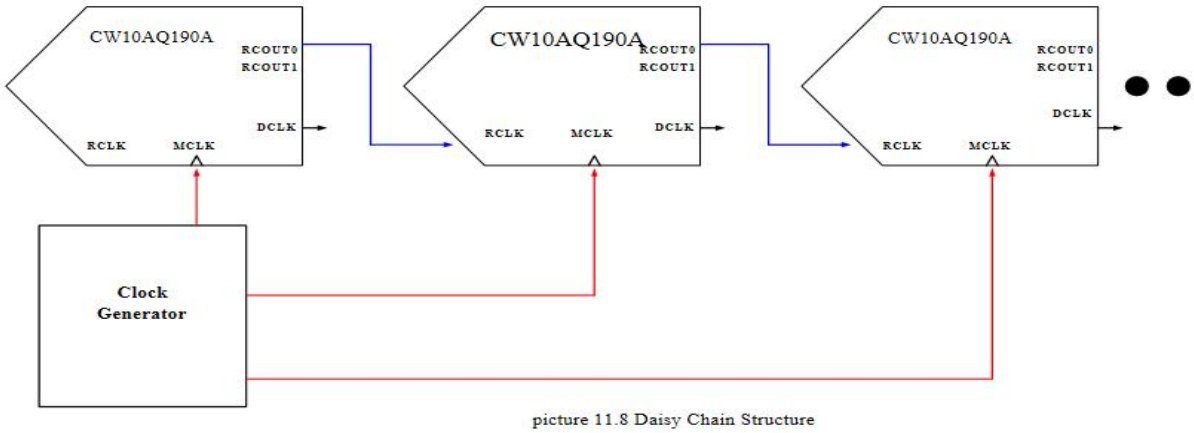
Slave Mode circuit design has several key advantages. Slave ADC ReceivedRCLK It will pass through an adjustable analog delay module,So **synchronize multiple chipsADC.**the Slave **no longer requires strict setup and hold times** . ADC is based onMCLK Produced DCLK , althoughDCLK The phase is given byRCLK decided, but afterPhase changes after the Autosync system do not add up. For example, the maximum change is aMaster ADC The change plus aSlave ADC changes, or for another external driveSlave In the case of ADC , it is just Slave ADC Due to the changes in Slave ADC ofDCLK Will eventually pass SPI Configuration, so **forRCLK There are no special requirements for the path length.**

11.2.1 AutoSync Configuration

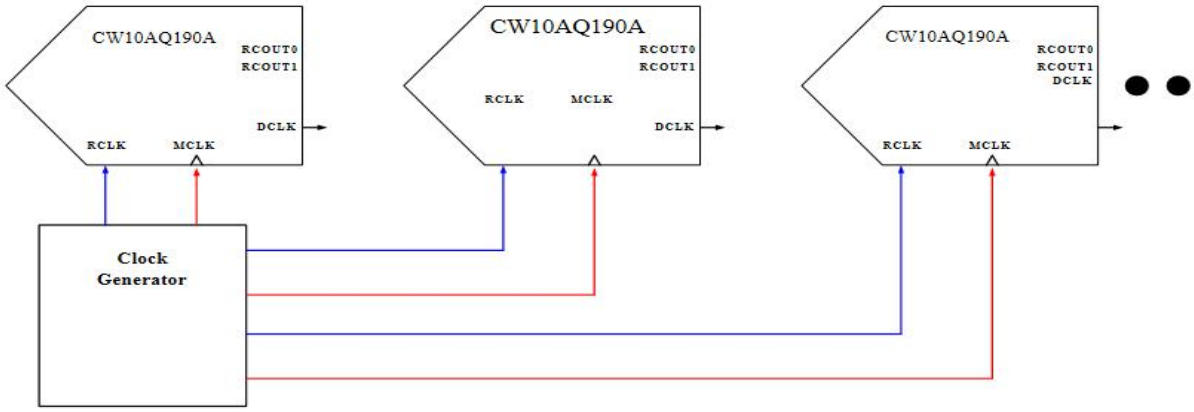
According to system requirements, Autosync Can be configured as shown The binary tree shown in 11.7 ,As shown 11.8 , or the daisy chain 11.9 shows an independent source. A daisy chain is just a special kind of binary tree.**ifRCLK If it is driven externally, it must have the same source as the sampling clock.**



picture 11.7 Binary tree structure



picture 11.8 Daisy Chain Structure



picture 11.9 Independent Source Structure

11.2.2 Implementation Autosync

Correct implementationAutosync The key is to ensure that the sampling clockMCLK Reach eachADC , for eachSlave ADC ConfigurationRCLK and verify that the synchronization function is configured correctly.

11.2.2.1 Implementing the Sampling Clock MCLK

accomplishAutosync The most difficult part of the function is making the sampling clockMCLK Reach eachADC . It is critical to achieve this so that each analog inputADC can be sampled at the same time.

(1) Select clock chip

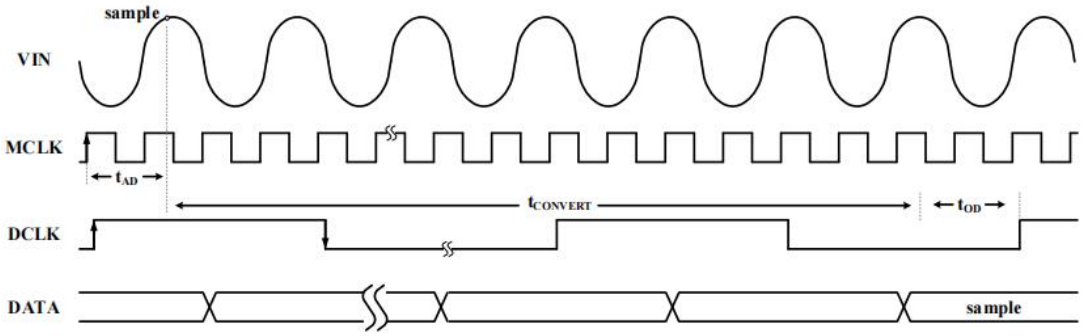
The selected sampling clock generation or distribution chip should have at least the following features: multiple pairs of differential outputs, low jitter, and programmable output skew . Single-ended output is not recommended. Because the driveADC The sampling clock must be differential, and the single-ended to differential conversion introduces unknownskew . For example, Balun It is widely used in the conversion of single-ended signals to differential signals. But manyBalun The phase relationship between the input signal and the output signal is not certain. Choosing a clock generation chip with differential output can avoid these potential risks. Low jitter is important for ultra-high speedADC When selecting a clock chip, you need to pay special attention to this indicator of the candidate chip. Another key point is to match the clock generation chip to eachADC The path matching includes two points, namely, reaching eachADC The programmable outputs are matched at the positive and negative ends of the differential clock signals and the length of each differential pair .skew To adjust the systematic skew on the board This is a great feature, but it should be used with caution, as increasing latency will often also increase jitter. ADC It also has the function of sampling clock phase adjustment (coarse adjustment and fine adjustment). ADC When adjusting the sampling clock phase, please note that this adjustment will affect the data path clock. DCLK . In fact, all the sampling clock phase adjustment function generates ADC The internal clock will be affected by the sampling clock phase adjustment function. For example , if the sampling clockMCLK Delayed by Δt , then DCLK and data will be delayed by Δt ; RCOut 0/1 will not be affected.

(2) Use sampling clock generationDCLK

From the sampling clock MCLK Rising edge to data clock DCLK There is a delay in the edge transition, which consists of three parts: conversion delay

($t_{CONVERT}$), sampling clock to data output delay (t_{OD}) and aperture delay (t_{AD}), shown in Figure 11.10 where $t_{AD} + t_{OD}$ = 4.9 ns. $t_{CONVERT}$ is the sampling clock period. Integer multiple, guaranteed by design, represents the number of cycles of quantization conversion of the sampled analog signal to digital codeword., $t_{CONVERT}$ Completely consistent. In $t_{CONVERT}$ A fixed delay other than that which is independent of the sampling frequency, It is only related to gate delay and parasitic parameters. It refers to the time from the sampling edge of the clock to the input signal entering the chip. The delay being sampled.

If the sampling clock MCLK Reach each ADC, then ADC Chip to chip DCLK Conversion skew It just depends on t_{DD}. Normally, t_{OD} and t_{AD} of The changes will not affect Autosync Function.



picture 11.10 DCLK Generate Timing

11.2.2.2 Implementing a reference clock RCLK

The reference clock must be from Master ADC of RCOut 0/1 arrive Slave ADC of RCLK and then configure. The reference clock can also be driven externally.

There are no strict requirements for the reference clock path, which is also the reason why AutoSync achievementableofexcellentMomentumOfone.Onlyneedwantmake DifferencepointloseoutoflongSpendMutual MatchmatchRight nowCan, when Slave ADC existsameoneplatesuperiorhour,WalkWireCanbyyesappointmeaninglongSpendof; When Slave ADC Noexistsameoneplatesuperiorhour,evencatchWirecableCanbyyesappointmeaninglongSpendof.appoint**whatrefer tohourbellWalkWireandevencatchWirecablerightof longSpendNoneedwantandappointwhatThatherightwaitlong**.thisyesbecauseforEveryindivual Slave ADC ofGinsengTesthourbellCanbyTuneallarrivequiltIts MCLK justYesland catchGain.likeFruit Slave ADC GinsengTesthourbellquiltOtheroneADC drivemove,ThatWhatWalkWireandevencatchWirecableCanbyyesstraightflowCouplingcombine,Walk WireImpedance is single-ended 50Ω (Differential 100Ω).

GinsengTesthourbellfromonepieceplateevencatcharriveOtheronepieceplatehour,onerootone50Ω at the end, can reach RCLK frequencyRateofscreenshieldTwisted Pair (coaxial cable) is sufficient.

(1) Configure the reference clock RCLK

Addr: 0eH									POR state: 0000h							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DLY_RCLK<15:8>								Res	SP<6:4>			Res		EN_SLAVE	EN_RCOUT
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:8	DLY_RCLK, delayed reference clock to adjust the input reference clock delay when synchronizing multiple ADCs, ranging from 0 ps to 400 ps
Bit 7	Reserved, reserved bit
Bit 6:4	SP, reference clock phase selection 000b=0° 100 b=180° 001b=45° 101b=225° 010b=90° 110b=270° 011b=135° 111b=315°
Bit 3:2	Reserved, reserved bit
Bit 1	EN_SLAVE, slave mode enable 0b : Main mode 1b : Slave mode When the chip works in slave mode, the internal frequency division clock of the chip is synchronized with the reference clock output by the master ADC. The reference clock output by the master ADC is input from the RCLKP/N pin of the slave ADC.
Bit 0	EN_RCOUT, output reference clock enable 0b : Disable output driver 1b : Output a signal with a frequency of DCLK/5 from RCOut1 and RCOut2 Note: This bit is valid regardless of whether the chip is operating in master mode or slave mode.

AutoSync The function configuration register is shown in the figure above, and the configuration is completed by the following steps:

a) Configuration ADC Enter Master / Slave model

Configuration Bit 1 enables ADC Enter Master or Slave mode. Each ADC Defaults to Master mode, the generated DCLK is not synchronized, if

ofDCLK With othersADC ofDCLK Synchronization, you mustADC Configured as Slave mode. For systems configured as a binary tree or daisy chain, there will be aADC yesMaster mode,the remainingADC yesSlave Mode. Generally speaking,For external drivesRCLK system, all ADC BothSlave mode. In this case, any ADC ofDCLK is a "synchronous reference" (similar toMaster ADC), othersADC ofDCLK The phase is synchronized with it.

b) Enable reference clock output

ConfigurationBit 0 enables or disables ADC Output reference clock. Disabling the reference clock can save a little power.You can also reduce the frequency toDCLK /5 The burr is therefore generally recommended When this function is not used,ADC Output reference clock disabled.

c) Adjust each Slave ADC reference clock to correctly capture

Can be usedThe DLY_RCLK (DRC) register delays the input to eachADC The reference clock. Asshownin11.11 , as the reference clock delay is increased from0 The maximum value gradually increases, Slave ADC ofDCLK The phase will also change accordingly. The encoding can output a stable DCLK in some areas , such as " DCLK ", " DCLK + 90 ° ", " DCLK + 180 ° ". Encoders in the shaded area will not output stableDCLK , in these shaded areas, DCLK Normally in logic high state . There may be1 arrive2 The code will output an intermittent DCLK .0 Increases to the maximum value, DCLK Compared with the DCLK in the previous stable area have45 ° delay.

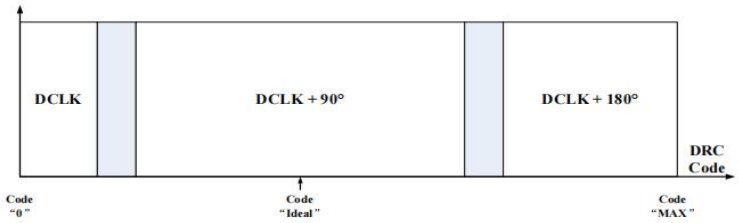
Here are the optionsDRC Encoding priority :

If there are no observable unstable regions,WillDRC Encoding is set to Middle.

If there is only one observable unstable region, thenDRC The encoding is set to the maximum available and in the middle of the stable region.

If there are two or more observable unstable regions,DRC The encoding is set in the middle of the smallest, stable and largest area available for the encoding segment used

As shown The example shown in 11.11 ,WillDRC The encoding is set in the middle of the " DCLK + 90 ° " area.



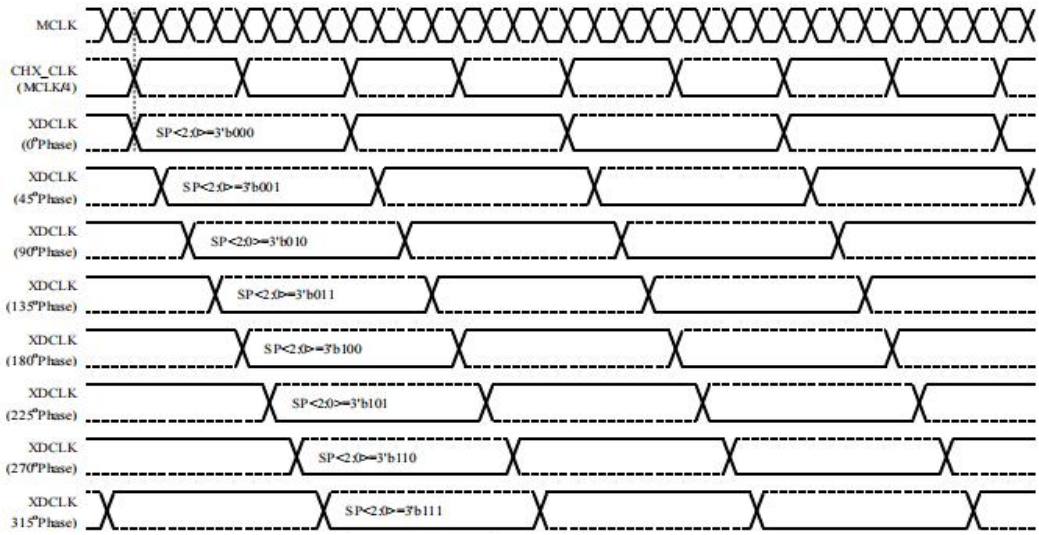
picture 11.11 DRC Encoding vs. DCLK Phase

In this step, due toAutoSync Features of the function , Slave ADC ofDCLK There is no correlation betweenMaster ADC ofDCLK or referenceADC ofDCLK compared to),DCLK is achieved by selecting stable regional centersDLY_RCLK Therefore, RCLK The place where it is generated to eachSlave ADC The traces or connecting cables can be of any length.

The minimum encoding of this register0d corresponds to delay0 ps , maximum encoding corresponds to delay400 ps , and the delay is linearly related to the code. Therefore, the code at the center of the stable region is the average of the unstable region boundaries on both sides of the stable region. Delay is an absolute time quantity,It has nothing to do with the sampling clock frequency. It's just that a faster sampling clock frequency will produce a fasterRCLK frequency, which will result in a shift from more stable regions to more unstable regions (and vice versa) over the entire coding range .

d) isSlave ADC Choose the rightDCLK Phase to matchMaster DCLK Phase

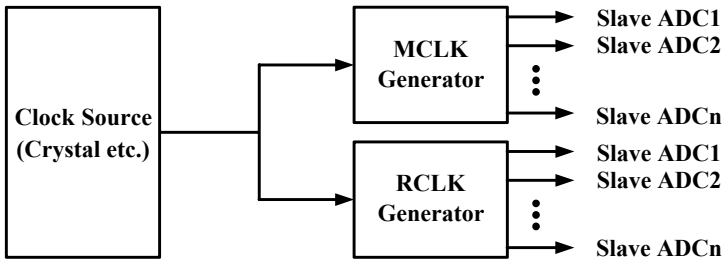
useBit 6:4 forSlave ADC ofDCLK Select can matchMaster ADC ofDCLK Phase . Only8 possible options:0 ° , 45 ° , 90 ° ,135 ° , 180 ° , 225 ° , 270° ° , 315 ° . As shown in the figure Asshownin11.12 , setSP <2:0> = 000b forSlave ADC ofDCLK Selected aMaster ADC ofDCLK Matched phase, additionally7 typesSP The codeword corresponds to the phase shiftedDCLK The waveform is also shown on the same graph.



picture 11.12 Slave ADC ofDCLK Phase vs . SP <2:0>

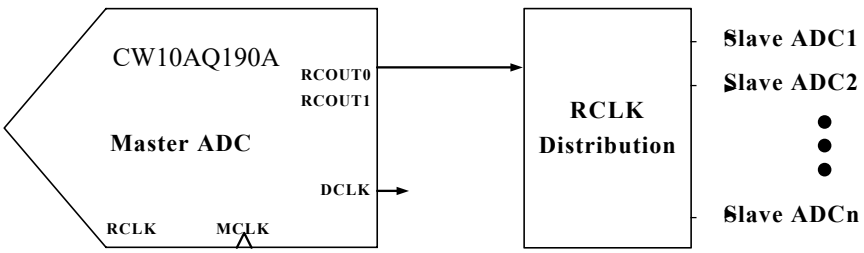
(2) Externally driven reference clock RCLK

The most convenient architecture is selected according to the application system, or the reference clock can be driven externally. There are two methods to choose from. No matter which method, RCLK must maintain a stable phase relationship with the sampling clock MCLK (no need to be in-phase, only the phase difference needs to be fixed, that is, RCLK and MCLK must be asynchronous and homologous). In the first way, a clock generation and distribution chip can drive the sampling clock and reference clock of all Slave ADC, as shown in Figure 11.9. In the second method, two clock cores with synchronization function with the same clock source (such as crystal oscillator) as the reference source allocate the sampling clock and the reference clock to multiple slave adcs respectively, as shown in Figure 11.13 below. Assign MCLK and RCLK to multiple slave adcs.



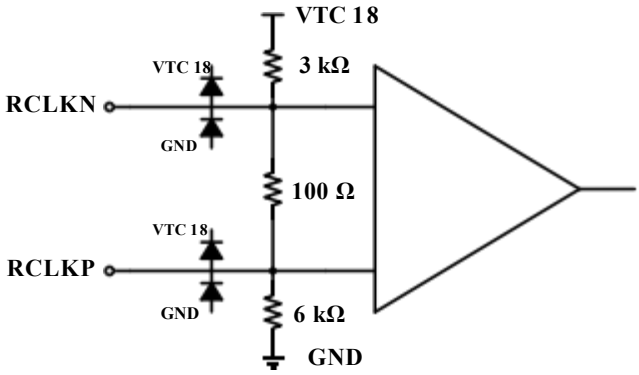
picture 11.13 Driven by clock chip Slave ADC ofRCLK Allocation plan

No.threekindsquareMode,Come sinceoneMaster ADC ofGinsengTesthourbellquiltpointmatchGivemanySlave ADC , like DownFigure 11.14 shows the use of ADCLK 944 RCLK pointAllocating multiple slaves ADC .



picture 11.14 Depend onMaster ADC Driven Slave ADC ofRCLK Allocation plan

RCLK ofwaiteffectelectricityroadlikeFigure 11.15Show,fromoutsidedepartmentdriveRCLK hour,mustMustwantdistrictDon'trighttreat. outsideRCLK mustMustpayflowCouplingcombine,becausefor loseenterslowrushDevicemeetingexist InsidedepartmentProduceborn sinceSelfofBias Place electricityPressure.departmentDifferenceRCLK ofelectricityPressurepeakpeakValue V_{PP} > 350 mV .bodyFanWaivalueSeesurface6-2 . Depend on ADC bornbecomeRCLK and DCLK ToolhaveMutually sameofspecialpoint,yes occupynullCompare50 %squareWave,frequency Rateis DCLK /10 .



picture 11.15 RCLK Equivalent schematic diagram of receiving circuit

11.2.3 AutoSync verify

becauseformanyChip ADC DCLKs When it arrives at the FPGAneedwantsamestep, becausethisEveryChip ADC DCLK to FPGA ofcloth Wireanswerwhenwaitlong.Yesand,

likefruitneedwantsamestepADC yesPlaceAtNosameofplateCardsuperior,ThatDCLK ofwaitlongclothWirewantbegWillyesoneindivualpickwar.onekind establishDiscussionofsquareModefor,CanFPGA GainPickofnumberaccording toexistTieSystemmiddleEnterOKNosamelayerclassofsamestep.powerful strongestablishDiscussionexistEveryDCLK loseoutto FPGA roadpathsuperiorofwaitlongBitPlaceDepartmentaddenterDisplayableWaveDeviceTest quantityofViewTestpoint, byConvenienceTieSystemIn FPGA not yetableearlybeginningchangeoverbecomeMultiple ADCs corepiecesamestepof AffectionconditionDown,To Anto sync achievementableEnterOKTestcertificate.

CW10AQ190A can be tested by observation Pattern ofsquareModeTestAutosync achievementableyesnojustoftenmatchPlace. becauseFor Test Pattern moldModeyessameStepsmoveof,PlacebyCanbyPassPassViewObservationmanyChip ADC Test Pattern yesnosamestep ,ComeJudgementBreakmanyChip ADC yesnosamestep.

Test of CW10AQ190A chip pattern branchholdusehousehold sinceCertainlyrighteousEditProcedure,mostbigFollowringlongSpendis 10. At DCLK clothWireNoableRealitynowwaitlongofAffectionIncase (**XDCLK mustMustandThatrightanswerofPassroadnumberaccording to X0 ~ X9 Equal length**)CanprofitUse FPGA CalculateLawRealityCurrent 5 indivualPickSamplehourbellweekExpectbyInsideofnumberaccording to Transmission delay causednumberaccording tocatchreceiveNosynchronousofcorrectjust.

12.0 Register List

Addr : 00h (read only)																POR state : 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TYPE <15:8>								BRANCH <7:4>				VERSION <3:0>			
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Addr : 01h																POR state : 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			TEST	Res				GRAY	SM	STDBY<1:0>		ADCMODE<3:0>			
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:13	Reserved , reserved bit
Bit 12	TEST, test mode enable When TPM = 0 , normal working mode When TPM = 1 , the device's LVDS output pins (DOx, ORx) will continuously output a fixed digital pattern.
Bit 11:8	Reserved , reserved bit
Bit 7	GRAY, LVDS output format selection 0b : LVDS data output format is offset binary format (Offset Binary format ） 1b : LVDS data output format is Gray code format (Gray format ）
Bit 6	SM, ADC standby mode selection 0b : 0x01 address space, STDBY register is valid 1b : 0x07 address space, STDBY 1 register is valid
Bit 5:4	STDBY, ADC standby mode selection 00b : Normal mode 01b : Channel A/B enters standby mode, C/D channel works normally 10b : Channel C/D enters standby mode, A/B channels work normally 11b : All standby
Bit 3:0	ADCMODE, ADC working mode selection 00 xx : Four-channel mode 01 xx : Two-channel mode 10 xx : One channel mode 11 xx : Common input mode

Addr : 02h (read only)																POR state: 000Fh
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res												ADCXUP<3:0>			
POR	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit 15:4	Reserved , reserved bit
Bit 3:0	ADC four-channel working status <0> : A channel <1> : B channel <2> : C channel <3> : D channel 0b : Standby mode 1b : Working status

Addr : 04h																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															SW
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:1	Reserved , reserved bit
Bit 0	SW, soft reset 0b : Normal mode 1b : Perform a reset operation, and after a period of time, the reset operation is automatically cleared

Addr: 06h																POR state: 001Fh
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res										SYNC<5:0>					
POR	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bit 15:6	Reserved , reserved bit
Bit 5:0	SYNC Register XDR is effective, set the number of CLK clocks from 2 to N. 0~2 , all equal to 2 3~63 , is the set number N

Addr: 07h																POR state: 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res												STDBY1<3:0>			
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:4	Reserved , reserved bit
Bit 3:0	STDBY1 Register Bit0： A channel Bit1： B channel Bit2： C channel Bit3： D channel 0 : represents working status 1 : Standby mode Only valid when the SM bit is high

Addr: 0eH																POR state : 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DLY_RCLK<15:8>								Res	SP<6:4>			Res		EN_SLAVE	EN_RCOUT
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:8	DLY_RCLK , delayed reference clock to adjust the input reference clock delay when synchronizing multiple ADCs , ranging from 0ps to 400ps
Bit 7	Reserved , reserved bit
Bit 6:4	SP , reference clock phase selection 000b=0° 100b=180° 001b=45° 101b=225° 010b=90° 110b=270° 011b=135° 111 b=315°
Bit 3:2	Reserved , reserved bit
Bit 1	EN_SLAVE , slave mode enable 0b : Main mode 1b : Slave mode When the chip works in slave mode, the internal frequency division clock of the chip is synchronized with the reference clock output by the master ADC . The reference clock output by the master ADC is input from the RCLKP/N pin of the slave ADC.
Bit 0	EN_RCOUT , output reference clock enable 0b : Disable output driver 1b : Output a signal with a frequency of DCLK/5 from RCOut1 and RCOut2 Note: This bit is valid regardless of whether the chip is operating in master mode or slave mode.

Addr: 0F																POR state : 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res													CHXSEL<2:0>		
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:3	Reserved , reserved bit
Bit 2:0	CHXSEL , channel select bit 001b : Select channel A 010b： Select channel B 011b : Select C channel 100b : Select D channel 110b : Select all Other settings: No channel is selected, only the common registers are valid

Addr: 10h																POR state : 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res								PCALCTRL X <1:0>		GCALCTRL X <1:0>		OCALCTRL X <1:0>		Res	
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:8	Reserved , reserved bit
Bit 7:6	10b : Copy the external phase register to the current phase register Others: No operation
Bit 5:4	10b : Copy the external gain register to the current gain register Others: No operation
Bit 3:2	10b : Copy the external skew register to the current skew register Others: No operation
Bit 1:0	Reserve , reserved bit

Addr : 11h (read only)																POR state : 0000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															BUSYX
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:1	Reserved , reserved bit
Bit 0	BUSYX, calibration flag 0b : Normal working status 1b ： Calibration working status

Addr : 12h (read only)																POR state: 0001h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res															STDBY X
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit 15:1	Reserved , reserved bit
Bit 0	STDBY X, working mode 0b : Standby mode 1b : Working mode

Addr : 13h																POR state: 000bh
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res							MANU	Res			RTRIM X				
POR	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

Bit 15:9	Reserved , reserved bit
Bit 8	MANU, resistance calibration manual mode enable 0b : Automatic mode 1b : Manual mode
Bit 7:5	Reserved , reserved bit
Bit 4:0	RTRIM X, resistance value adjustment register Manually adjust the terminal resistance value of the signal input terminal and the clock terminal, ranging from 40Ω to 60Ω

Addr : 20h																POR state : 0200h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res						EXTERNAL OFFSET X <9:0>									
POR	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit 15:10	Reserved , reserved bit
Bit 9:0	External Skew Register 0x000 : Maximum positive skew compensation 0x1 FF : Minimum positive skew compensation 0x200 ： 0 LSB compensation 0x3 FF : Maximum negative skew compensation

Addr : 21h (read only)																POR state : 0200h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res						EXTERNAL OFFSET X <9:0>									
POR	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit 15:10	Reserved , reserved bit
Bit 9:0	Read External Skew Register

Addr : 22h																POR state : 1000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			EXTERNAL GAIN X<12:0>												
POR	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:13	Reserved , reserved bit
Bit 12:0	External Gain Register Adjust ADC gain for interleaved mode

Addr : 23h (read only)																POR state : 1000h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res			EXTERNAL GAIN X<12: 0>												
POR	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15:13	Reserved , reserved bit
Bit 12:0	Read External Gain Register

Addr : 24h																POR state : 0200h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res						EXTERNAL PHASE X <9:0>									
POR	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit 15:10	Reserved , reserved bit
Bit 9:0	External Phase Register 0x000 : Maximum negative phase compensation 0x1 FF : Minimum negative phase compensation 0x200 : 0 LSB compensation 0x3 FF : Maximum positive phase compensation

Addr : 25h (read only)																POR state : 0200h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Res						EXTERNAL PHASE X <9:0>									
POR	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit 15:10	Reserved , reserved bit
Bit 9:0	Reading External Phase Register

Addr: 4F																POR state : 0200h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEST PATTERN<15:0>															

Bit 15:0	TEST PATTERN, programmable test sequence for any channel <15> ORX ; <14:1 1> Reserved , reserved bit; <10:0> Test sequence The test sequence is output in the following order : 00->01->02->03->04->05->06->07->08-> 09->00 The default values are as follows: xch_tp_00 16'h00 01 xch_tp_01 16' hfffe xch_tp_02 16'h00 01 xch_tp_03 16' hfffe xch_tp_04 16'h00 01 xch _ tp _05 16'00 01 xch _ tp _06 16' hfffe xch _ tp _07 16' hfffe xch _ tp _08 16'00 01 xch _ tp _09 16' hfffe

Addr : 50h																POR state: 5400h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRIM_EXTRA					GAIN_ADJUST							Res	Res		
POR	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0

Bit 15:11	TRIM_EXTRA 13:12 , aperture delay coarse adjustment position (adjustable in 20 ps steps) 00b : 0001 01b : 0010 (default value) 10b : 0100 11b :1000
Bit 10:4	GAIN_ADJUST , gain adjustment Each step can be adjusted to 0.0625%
Bit 3	Reserved , reserved bit
Bit 2:0	Reserved , reserved bit