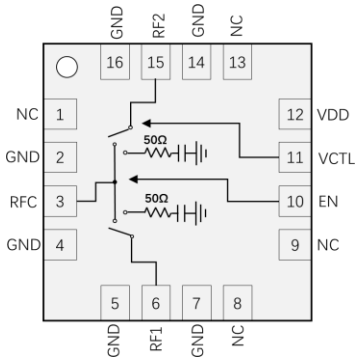
Performance Features

- Operating frequency band: 0.1~6GHz
- Low insertion loss: 0.65dB~1dB typical
- High isolation: 60dB@0.1~2GHz
  50dB@2GHz~4GHz
  45dB@4GHz~6GHz
- Package size: 16-pin QFN, 3mmx3mm

Typical Applications

- Base station communication
- Wireless Infrastructure
- Automotive Electronics
- Instrumentation

Functional Block Diagram



Overview

The CWS084SP3 is a highly isolated, low insertion loss, and highly linear single-blade double-throw switch.
The CWS084SP3 switch is available in a 16-pin 3mmx3mm surface mount leadless plastic package. The pin pad plating is Sn or NiPdAu.

Electrical performance table (TA=+25℃, VDD=3.3V)

Parameter Name	Test conditions	Minimum value	Typical values	Maximum value	Unit
RF Frequency Range		0.1 to 6			GHz
insert loss	0.1~2GHz		0.65	1	dB
	2GHz~4GHz		0.85	1.3	dB
	4GHz~6GHz		1	1.5	dB
Isolation	0.1~2GHz		60		dB
	2GHz~4GHz		50		dB
	4GHz~6GHz	35	45		dB
Return loss	open state		20		dB
	Off-state		20		dB
Bias Voltage (VDD)		3		3.3	V
Bias Current (IDD)				1	mA
Input 0.1dB compression point power (P0.1dB)	open state		31		dBm
Input 1dB compression point power (P1dB)	open state		33		dBm
Input third-order intercept point of intersection (IP3)	Pin=10dBm@1MHZ		52		dBm
Rise and fall time	10% to 90% RF output		60		ns
Switching time	50% Vctl to 10%/90% RF output		120		ns
Recommended input power	Passage diameter			31	dBm
	final path			26	dBm

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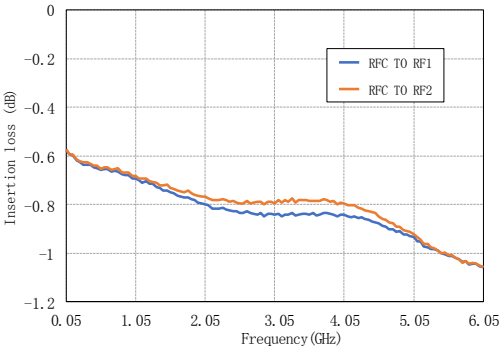
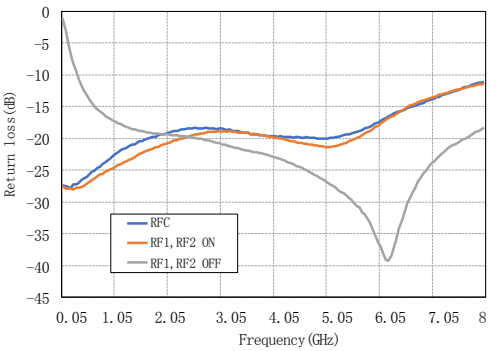
Test Curve

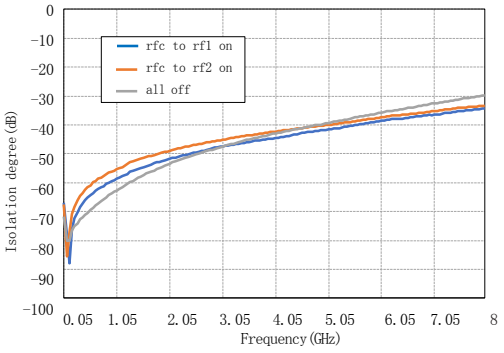
Insertion loss vs. frequency



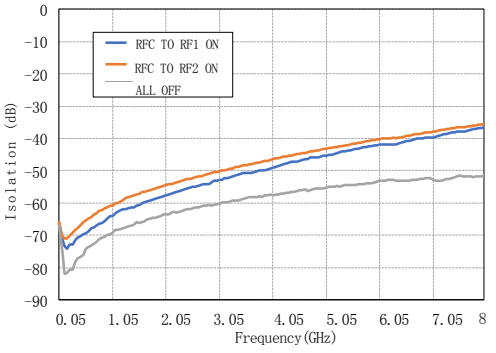
Return loss vs. frequency



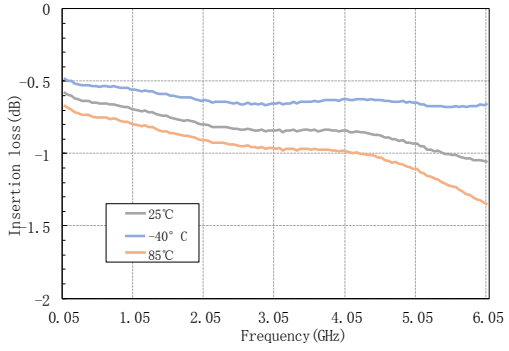
RFC TO RF1/RF2 Isolation VS Frequency



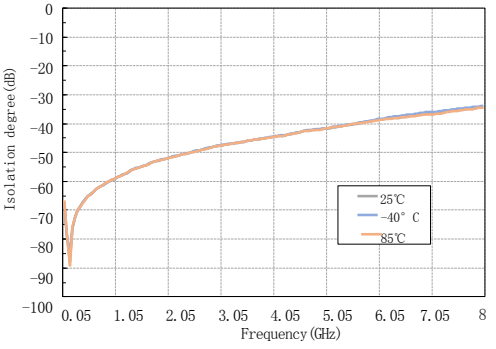
RF1 TO RF2 Isolation VS Frequency



Insertion loss vs. frequency



Isolation vs. frequency



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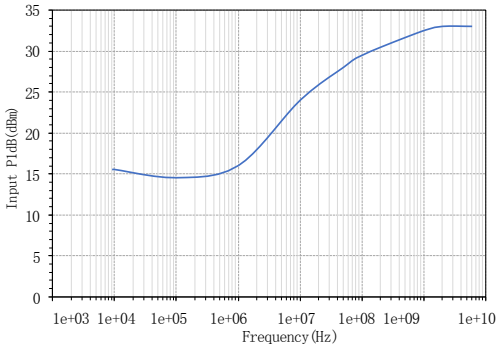
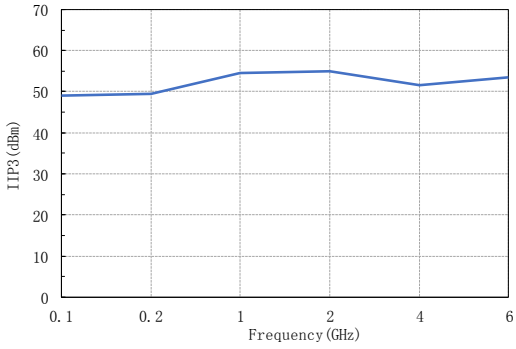
Test Curve

P1dB VS Frequency



IIP3 vs Frequency (Pin=10dBm@1MHZ)



Working parameters

Bias voltage VDD	3V to 3.3V
Control voltage EN, VCTL	0V～0.3V (Low) 3V to 3.3V (High)
Operating temperature	-40℃～+85℃

Absolute maximum rating

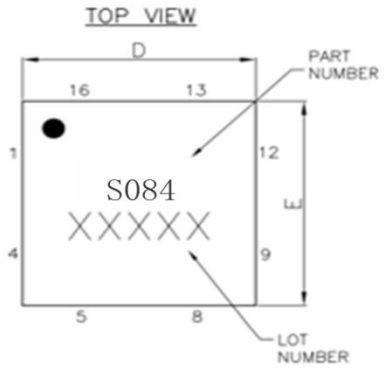
Bias voltage VDD	-0.3V to 3.6V
Control voltage EN, VCTL	-0.5 V to VDD+0.3V
Input power (through-hole)	33dBm
Input power (final diameter)	31dBm
Storage temperature	-65℃～+150℃

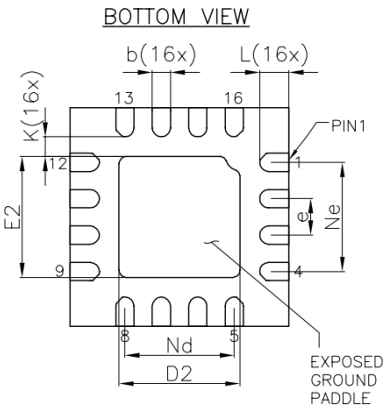
Package Information

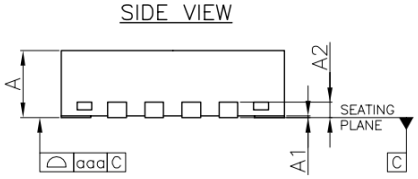
Model	Packaging Materials	Solder plate plating	MSL level [1]	Package identification [2]	Environmental requirements
CWS084SP3	Green resin compounds	Sn or NiPdAu	MSL 3	S084 XXXXX	RoHS compliant

[1] Maximum reflow temperature 260° C
[2] XXXXX is the lot number

Dimension







Description:

1. Unit: mm

2. Lead frame material: copper alloy

3. Package surface warpage: not more than 0.05mm

4. All ground pins should be connected to the PCB RF ground

Dimension Table (unit:mm)			
Symbol	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.20Ref		
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D2	1.51	1.66	1.80
e	0.50BSC		
Ne	1.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	1.51	1.66	1.80
K	0.20	---	---
L	0.30	0.40	0.50
aaa	0.08		

Pin Definition

Pin Number	Function Symbols	Function Description	Pin Number	Function Symbols	Function Description
1	NC	Vacant	9	NC	Vacant
2	GND	RF Ground	10	EN	Enable side
3	RFC	RF input	11	VCTL	Control Port
4	GND	RF Ground	12	VDD	Bias voltage
5	GND	RF Ground	13	NC	Vacant
6	RF1	RF Output	14	GND	RF Ground
7	GND	RF Ground	15	RF2	RF Output
8	NC	Vacant	16	GND	RF Ground

All NC pins are recommended to be connected to RF ground when in use

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Truth Table

Control and bias inputs			Signaling pathway status	
Bias Voltage (VDD)	Enable (EN)	Console (VCTL)	RFC to RF1	RFC to RF2
3.3V	Low	Low	Off	Off
3.3V	Low	High	Off	Off
3.3V	High	Low	On	Off
3.3V	High	High	Off	On

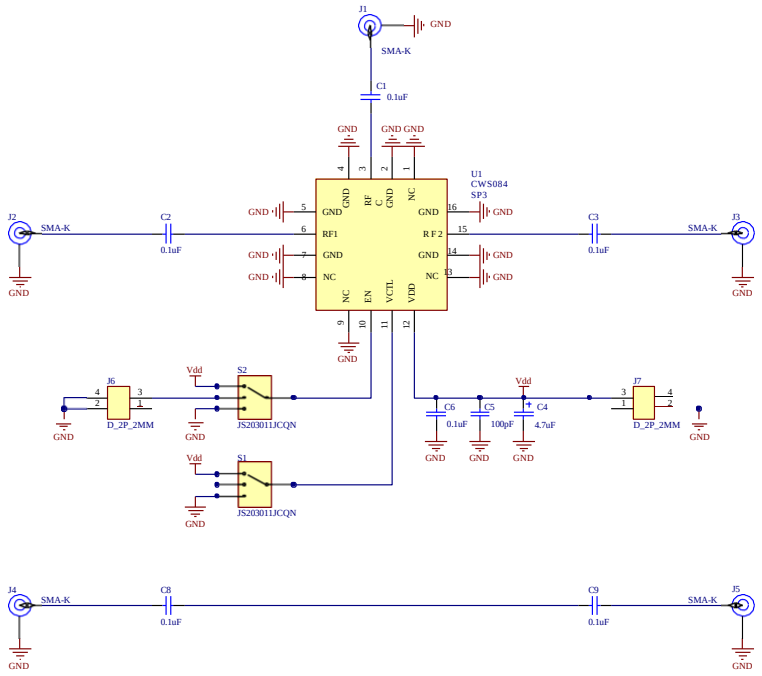
Working Principle

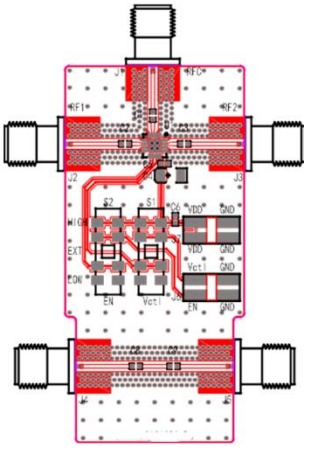
1. This switch requires a supply voltage to be applied to the VDD pin. It is recommended to bypass the capacitor on the power line to minimize RF coupling.
2. Control is provided by two digital control voltages applied to the VCTL pin and the EN pin. It is recommended that a small bypass capacitor be installed on these digital signal lines to improve the isolation of the RF signal.
3. The RF input port (RFC) and the RF output port (RF1 and RF2) are internally matched with 50Ω, so no external matching is required. The RF pins are DC-coupled, and the RF terminals need to be peripherally isolated with capacitors. The design is bi-directional and the inputs and outputs are interchangeable.
4. With a logic level of High at the EN pin, this switch has two modes of operation: On and Off. Depending on the logic level applied to the VCTL pin, one RF output port (e.g., RF1) is set to the on mode, through which an insertion loss path is provided from the input to the output, as the other RF output port (e.g., RF2) is set to the off mode, by which the output is isolated from the input. When the RF output port (RF1 or RF2) is in isolated mode, it is internally terminated to 50 Ω and the port absorbs the applied RF signal.
5. When the EN terminal is at a logic level of Low, EN sets the switch to the off mode. In the off mode, both output ports are isolated from the inputs and the RFC port is open for reflection.

Recommended power supply sequence

1. GND is energized.
2. VDD is energized no earlier than VCTL and EN is energized.
3. Turn on the RF input.

Evaluation Boards





Designator	Description
c1, c2, c3, c8, c9	0.1uF Ceramic Capacitor 0402
C4	4.7uF Tantalum Capacitor 3216
C5	100pF Ceramic Capacitor 0402
C6	0.1uF Ceramic Capacitor 0402
j1, j2, j3, j4, j5	SMA PCB connector
J6, J7	4Pin DC pins
S1, S2	Toggle Switch
U1	CWS084SP3
J1, J2, J3, J4, J5 recommended to use Nanjing Aowen D550B12E01-048 type SMA Connectors	

Circuit board material: Rogers 4350B

The circuit board of the device application should be designed in accordance with the RF circuit design method, the signal line is designed according to 50Ω impedance, while the grounding pin of the package shell is grounded nearby (similar to the figure), connecting the top and bottom ground should have enough grounding holes.

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